IS43R32400D

4Mx32
128Mb DDR SDRAM

SEPTEMBER 2011

FEATURES

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/ received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs and centre-aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data Mask for write data. DM masks write data at both rising and falling edges of data strobe
- Burst Length: 2, 4 and 8
- Burst Type: Sequential and Interleave mode
- Programmable CAS latency: 2, 2.5, 3 and 4
- Auto Refresh and Self Refresh Modes
- Auto Precharge
- VDD and VDDQ: 2.5V ± 0.2V (-5, -6)
- VDD and VDDQ: 2.5V ± 0.125V (-4)
- SSTL_2 compatible I/O

OPTIONS

- Configuration(s): 4M x32
- Package(s):
  144 Ball BGA (x32)
- Lead-free package available
- Temperature Range:
  Commercial (0°C to +70°C)
  Industrial (-40°C to +85°C)

DEVICE OVERVIEW

ISSI's 128-Mbit DDR SDRAM achieves high speed data transfer using pipeline architecture and two data word accesses per clock cycle. The 134,217,728-bit memory array is internally organized as four banks of 32Mb to allow concurrent operations. The pipeline allows Read and Write burst accesses to be virtually continuous, with the option to concatenate or truncate the bursts. The programmable features of burst length, burst sequence and CAS latency enable further advantages. The device is available in 32-bit data word size Input data is registered on the I/O pins on both edges of Data Strobe signal(s), while output data is referenced to both edges of Data Strobe and both edges of CLK. Commands are registered on the positive edges of CLK.

An Auto Refresh mode is provided, along with a Self Refresh mode. All I/Os are SSTL_2 compatible.

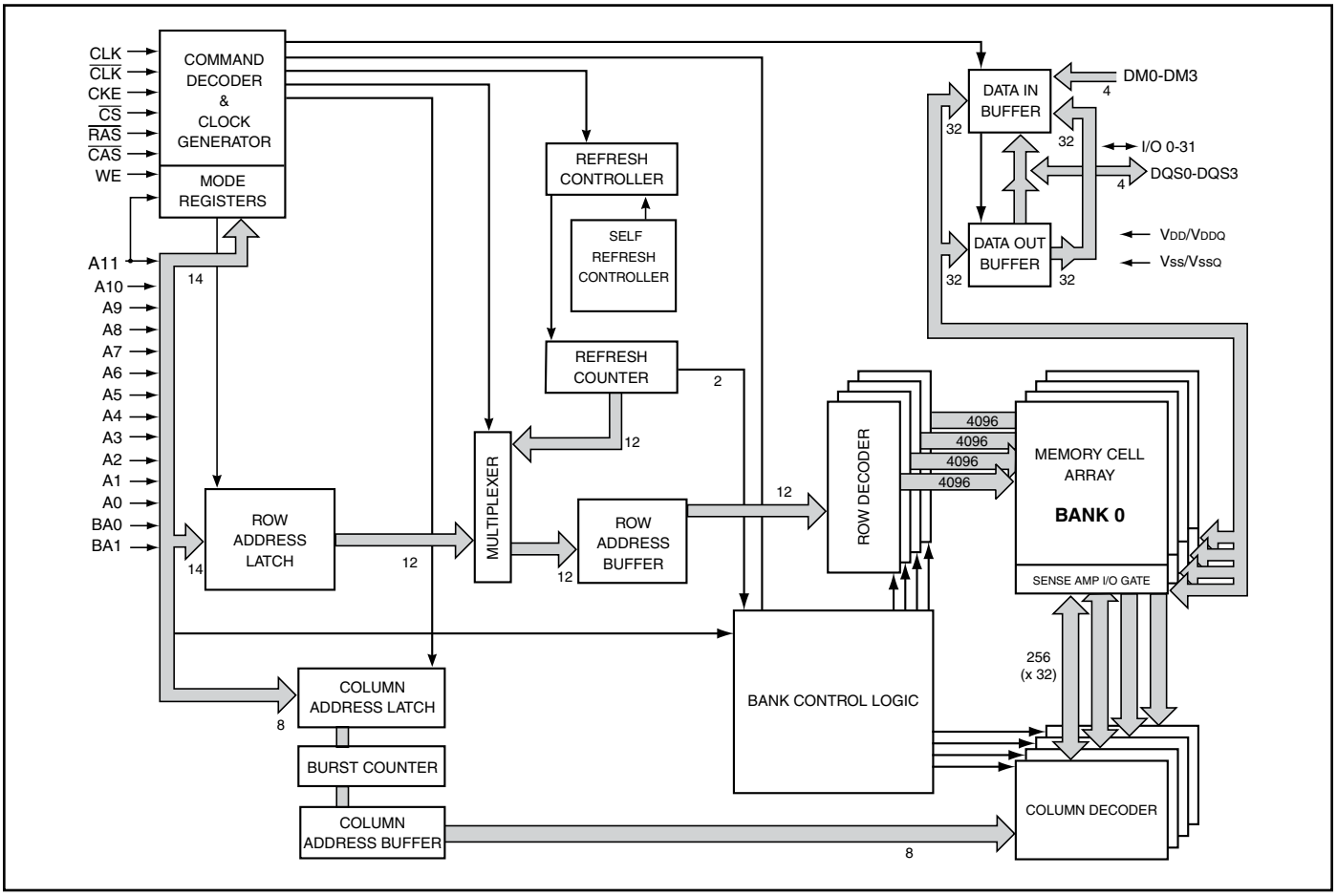
ADDRESS TABLE

Parameter	4M x 32
Configuration	1M x 32 x 4 banks
Bank Address Pins	BA0, BA1
Autoprecharge Pins	A8/AP
Row Addresses	4K(A0 – A11)
Column Address	256(A0 – A7)
Refresh Count	4K / 32ms

KEY TIMING PARAMETERS

Speed Grade	-4	-5	-6	Units
F_{CK} Max CL = 4	250	200	166	MHz
F_{CK} Max CL = 3	200	200	166	MHz
F_{CK} Max CL = 2.5	–	166	166	MHz
F_{CK} Max CL = 2	–	133	133	MHz

FUNCTIONAL BLOCK DIAGRAM (x32)

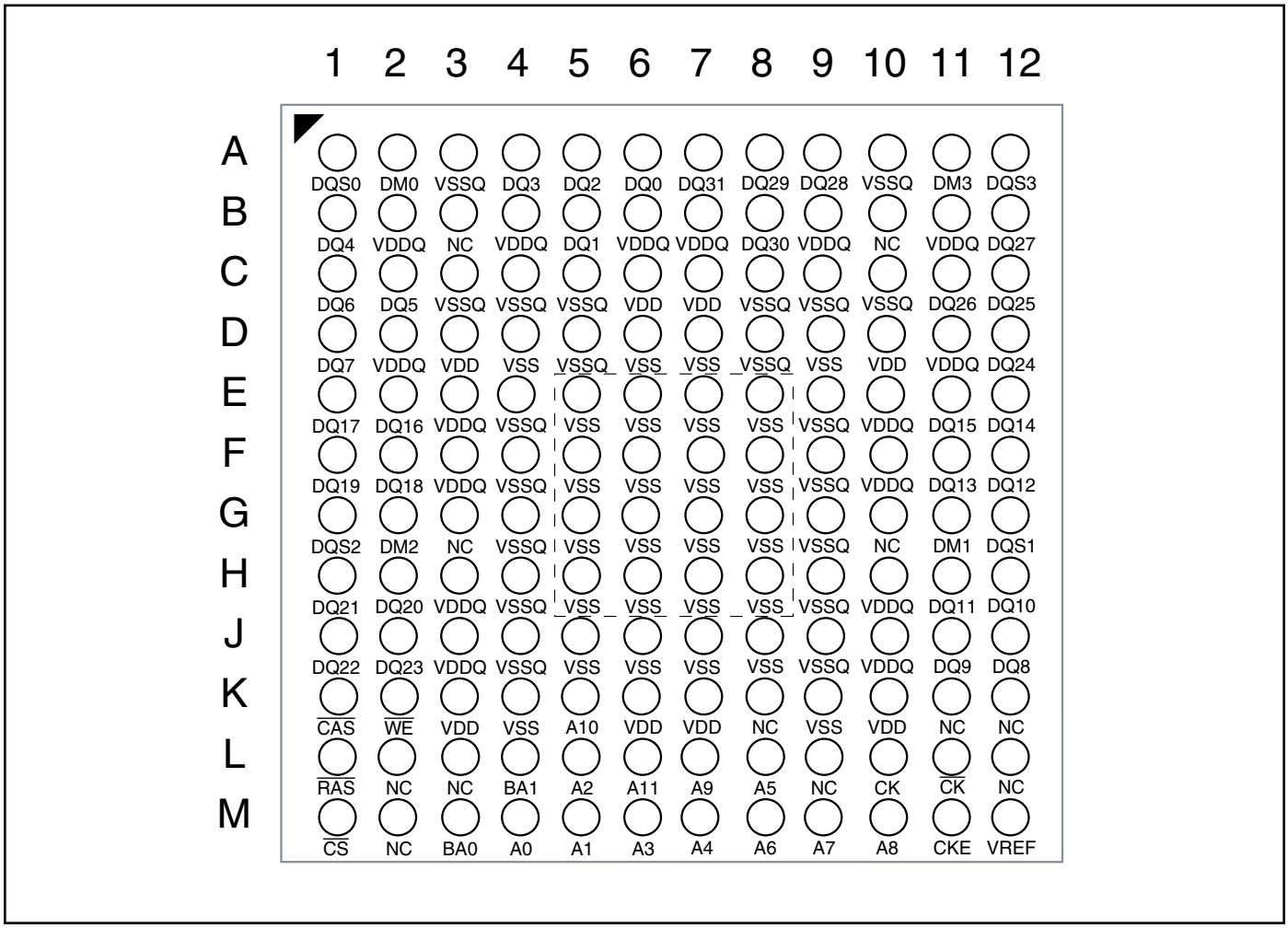


PIN CONFIGURATION

Package Code B: 144-ball FBGA (top view)

(12mm x 12mm Body, 0.8mm Ball Pitch)

Top View (Balls seen through the package)



Note: Vss balls inside the dotted box are optional for purposes of thermal dissipation.

PIN DESCRIPTION: for x32

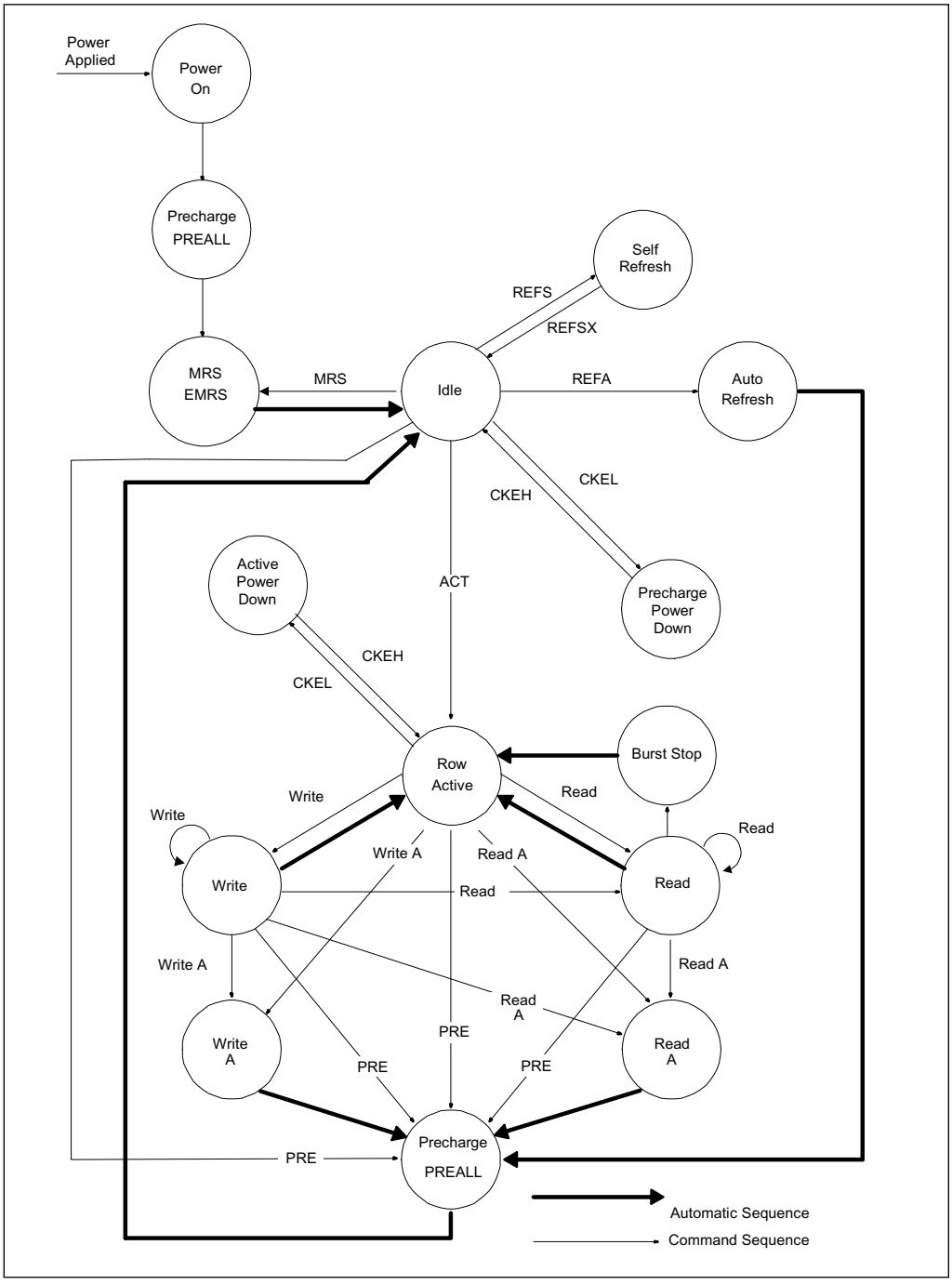
A0-A11	Row Address Input
A0-A7	Column Address Input
BA0, BA1	Bank Select Address
DQ0 – DQ31	Data I/O
CK, $\overline{CK}$	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe Command
$\overline{RAS}$	Row Address Strobe Command

$\overline{WE}$	Write Enable
DM0-DM3	Data Write Mask
DQS0-UDQS	Data Strobe
VDD	Power
VDDQ	Power Supply for I/O Pins
VREF	Reference voltage for SSTL_2
VSS	Ground
VSSQ	Ground for I/O Pins
NC	No Connection

PIN FUNCTIONAL DESCRIPTIONS

Symbol	Type	Description
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{CK}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select: CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	$\overline{WE}$ Input Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM: DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
BA0, BA1	Input	Input Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [11:0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ: DQ0-DQ31	I/O	Data Bus: Input / Output
DQS: DQS0-DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
NC	--	No Connect: Should be left unconnected.
VREF	Supply	SSTL_2 reference voltage
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground
VDD	Supply	Power Supply
VSS	Supply	Ground

SIMPLIFIED STATE DIAGRAM



PREALL = Precharge All Banks

CKEL = Enter Power Down

MRS = Mode Register Set

CKEH = Exit Power Down

EMRS = Extended Mode Register Set

ACT = Active

REFS = Enter Self Refresh

Write A = Write with Autoprecharge

REFSX = Exit Self Refresh

Read A = Read with Autoprecharge

REFA = Auto Refresh

PRE = Precharge

FUNCTIONAL DESCRIPTION

The DDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. The 128 Mb devices contains: 134,217,728 bits.

The DDR SDRAM uses double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation

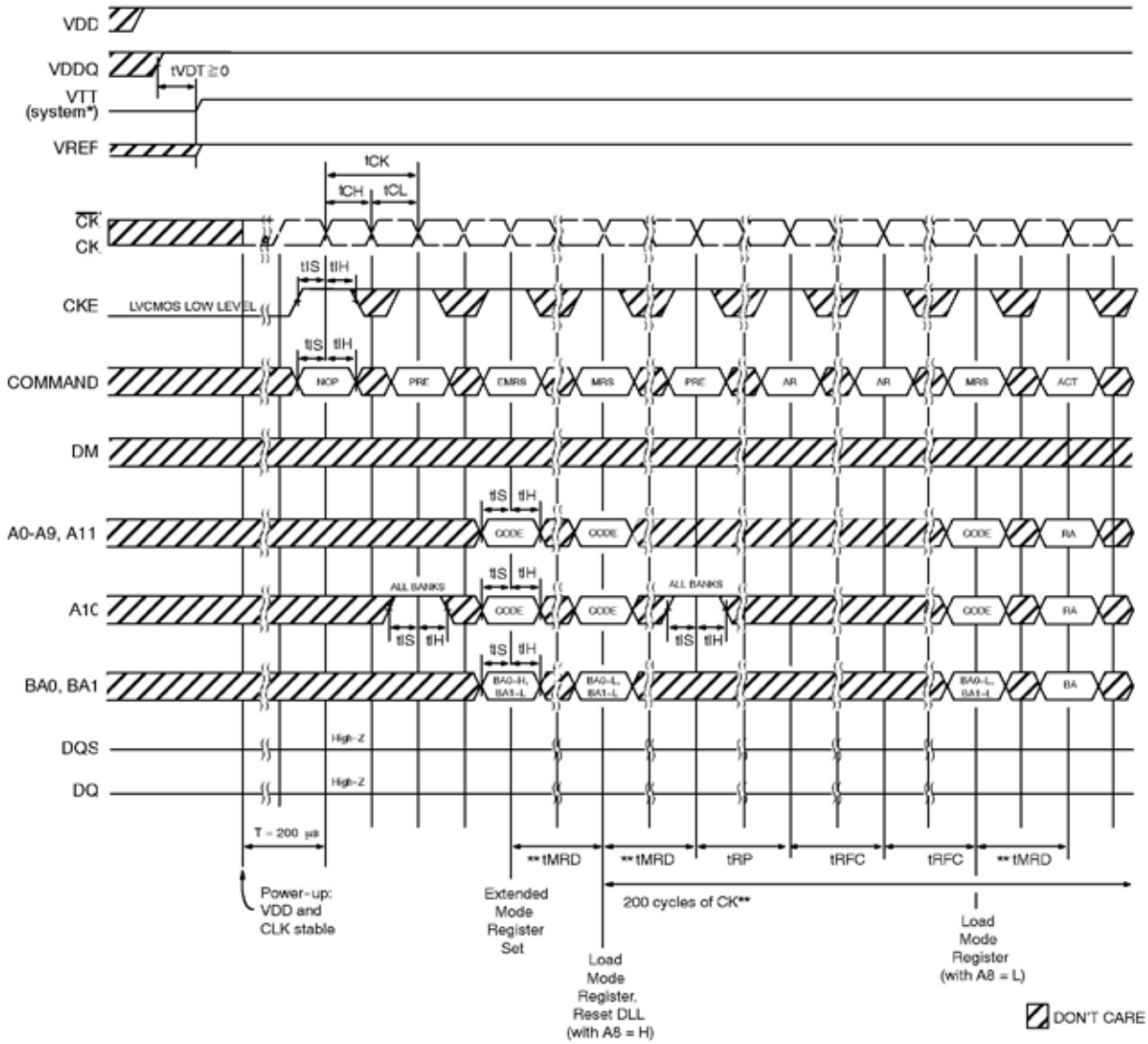
INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below. The Initialization Flow diagram and the Initialization Flow sequence are shown in the following figures.

The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Step 1 through 13.

- Step1: Apply VDD before or at the same time as VDDQ
- Step 2: CKE must maintain LVCMOS Low until VREF is stable. Apply VDDQ before applying VTT and VREF
- Step 3: There must be at least 200 µs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus and CKE should be brought HIGH.
- Step 4: Issue a PRECHARGE ALL command.
- Step 5: Provide NOPs or DESELECT commands for at least tRP time.
- Step 6: Issue EMRS command
- Step 7: Issue MRS command, load the base mode register and to reset the DLL. Set the desired operating modes.
- Step 8: Provide NOPs or DESELECT commands for at least tMRD time.
- Step 9: Issue a PRECHARGE ALL command
- Step 10: Issue 2 or more AUTO REFRESH cycles
- Step 11: Issue MRS command with the reset DLL bit deactivated to program operating parameters without resetting the DLL
- Step 12: Provide NOP or DESELECT commands for at least tMRD time.
- Step 13: The DRAM has been properly initialized and is ready for any valid command.

Initialization Waveform Sequence

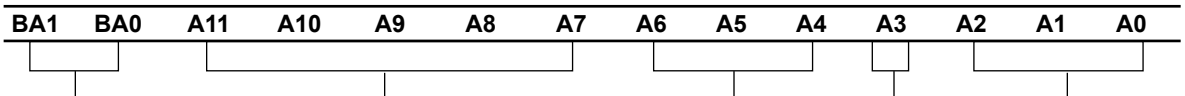


Notes:
* = VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch--up.
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied
The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

MODE REGISTER (MR) DEFINITION

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the definition of a burst length, a burst type, and a CAS latency. The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device goes into Deep Power-Down mode, or the device loses power. Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency, and A8 DLL reset. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility. The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result

MODE REGISTER DEFINITION



A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A11	A10	A9	A8	A7	DLL
0	0	0	0	0	Normal operation
0	0	0	1	0	Reset DLL

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Program Extended Mode Register
1	0	Reserved
1	1	Reserved

Notes:
1. An = most significant address bit for this device.
2. A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.

BURST LENGTH

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being set and the burst order as in Burst Definition. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
			A 0		
2			0	0-1	0-1
			1	1-0	1-0
		A 1	A 0		
		0	0	0-1-2-3	0-1-2-3
4		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A 2	A 1	A 0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
8	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:
1. For a burst length of two, A1-A7 selects the two data element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A7 selects the four data element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A7 selects the eight data element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1-A7 when the burst length is set to two, by A2-A7 when the burst length is set to 4, by A3-A7 when the burst length is set to 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.

The programmed burst length applies to both read and write bursts.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address.

READ LATENCY

The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data.

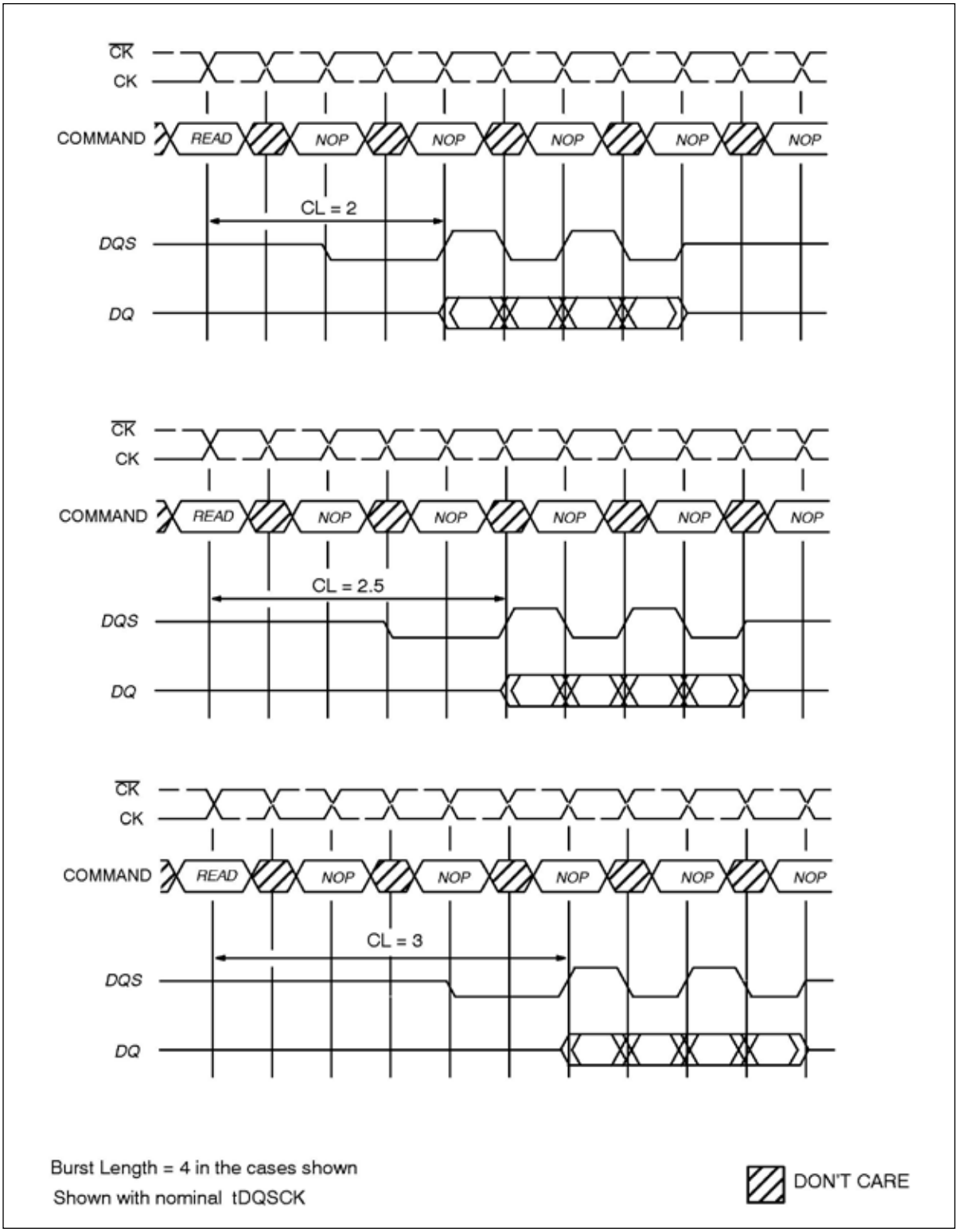
If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2tCK + tAC. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + tCK + tAC.

OPERATING MODE

The normal operating mode is selected by issuing a Mode Register Set command with bits A7 to A11 each set to zero, and bits A0 to A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9 to A11 each set to zero, bit A8 set to one, and bits A0 to A6 set to the desired values. A Mode Register Set command issued to reset the DLL must always be followed by a Mode Register Set command to select normal operating mode (i.e., with A8=0).

All other combinations of values for A7 to A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

CAS LATENCIES



EXTENDED MODE REGISTER (EMR) DEFINITION

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, and output drive strength selection. The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=0 and BA0=1) and will retain the stored information until it is reprogrammed, or the device loses power. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

DLL Enable/Disable

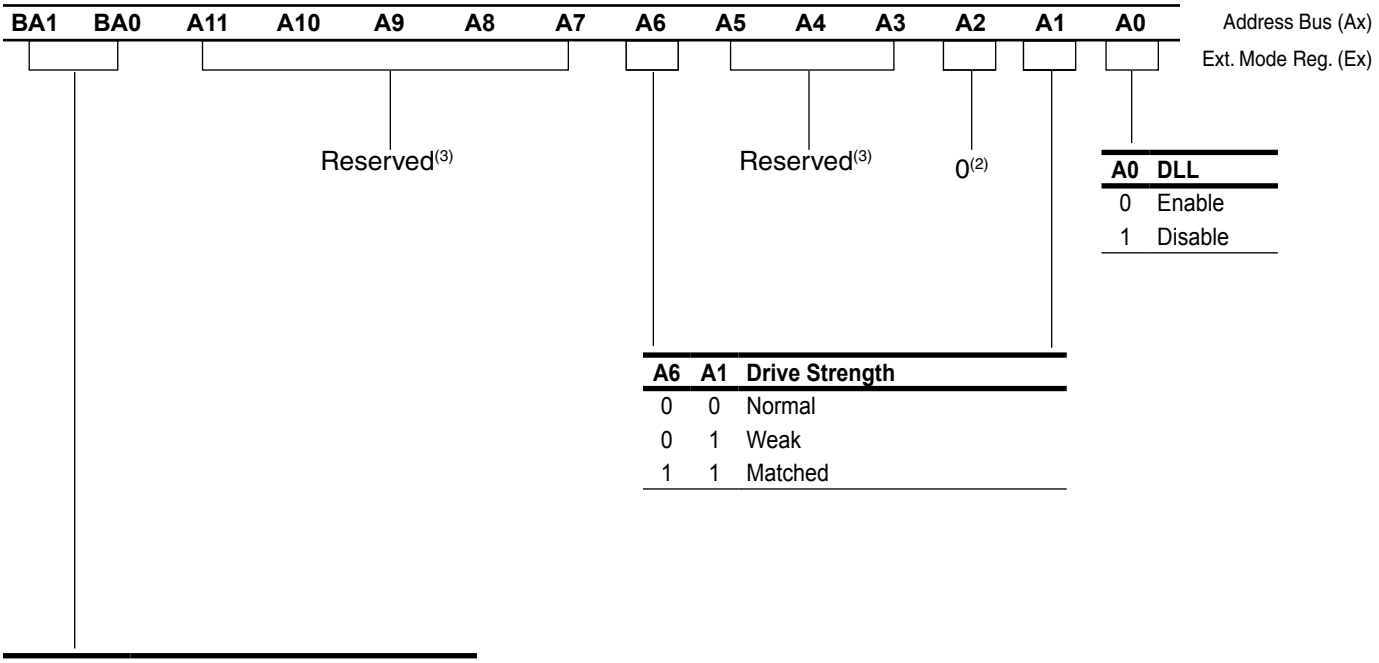
The DLL must be enabled for normal operation. DLL enable is required during power--up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles must occur before any executable command can be issued.

OUTPUT DRIVE STRENGTH (DS)

The normal drive strength for all outputs is specified to be SSTL_2, Class II. This DRAM also supports a weak driver strength option, intended for lighter load and/or point--to--point environments.

EXTENDED MODE REGISTER DEFINITION

Extended Mode Register Definition



A0	DLL
0	Enable
1	Disable

A6	A1	Drive Strength
0	0	Normal
0	1	Weak
1	1	Matched

BA1	BA0	Mode Register Definition
0	0	Program Mode Register
0	1	Program Extended Mode Register
1	0	Reserved
1	1	Reserved

NOTES:
1. MSB depends on DDR SDRAM density.
2. A2 must be 0 to provide compatibility with early DDR devices
3. A logic 0 should be programmed to all unused/undefined address bits to ensure future compatibility

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_{IN}, V_{OUT}	-1.0 ~ 3.6	V
Voltage on VDD & VDDQ supply relative to VSS	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5	W
Short circuit current	I_{OS}	50	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

AC/DC Electrical Characteristics and Operating Conditions

Recommended operating conditions (Voltage referenced to VSS=0V, TA=0 to 70°C for Commercial. TA = -40°C to +85°C for Industrial)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (for device with a nominal VDD of 2.5V for -5, -6)	V_{DD}	2.3	2.7	V	
Supply voltage (for device with a nominal VDD of 2.5V for -4)	V_{DD}	2.375	2.625	V	
I/O Supply voltage (for device with a nominal VDD of 2.5V for -5, -6)	V_{DDQ}	2.3	2.7	V	
I/O Supply voltage (for device with a nominal VDD of 2.5V for -4)	V_{DDQ}	2.375	2.625	V	
I/O Reference voltage	V_{REF}	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage (system)	V_{TT}	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	$V_{IH(DC)}$	VREF+0.15	VDDQ+0.3	V	
Input logic low voltage	$V_{IL(DC)}$	-0.3	VREF-0.15	V	
Input Voltage Level, CLK and CLK inputs	$V_{IN(DC)}$	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CLK and CLK inputs	$V_{ID(DC)}$	0.36	VDDQ+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	V_I(Ratio)	0.71	1.4	–	4
Input leakage current	I_L	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strength driver) ; VOUT = VTT + 0.84V	I_{OH}	-16.8	–	mA	
Output Low Current (Normal strength driver) ; VOUT = VTT - 0.84V	I_{OL}	16.8	–	mA	
Output High Current (Half strength driver); VOUT = VTT + 0.45V	I_{OHR}	-9	–	mA	
Output Low Current (Half strength driver); VOUT = VTT - 0.45V	I_{OLR}	9	–	mA	
Ambient Operating Temperature					
Commercial	T_A	0	+70	°C	
Industrial	T_A	-40	+85	°C	

Note :
1. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CLK and the input level on CLK.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

CAPACITANCE CHARACTERISTICS

(V_{DD} = V_{DDQ} = 2.5V ± 0.2V (-5, -6), V_{DD} = V_{DDQ} = 2.5V ± 0.125V (-4), Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Units
			Min	Max	
CI(A)	Input Capacitance, address pin	VI=1.25v	1.3	3	pF
CI(C)	Input Capacitance, control pin	f=100MHz	1.3	3	pF
CI(K)	Input Capacitance, CLK pin	VI=25mVrms	1.3	3	pF
CI/O	I/O Capacitance, I/O, DQS, DM pin		2	5	pF

IDD Specification Parameters and Test Conditions

(V_{DD} = V_{DDQ} = 2.5V ± 0.2V (-5, -6), V_{DD} = V_{DDQ} = 2.5V ± 0.125V (-4), Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/ Test Condition	-4	-5	-6	Units
IDD0	Operating current for one bank active-precharge; tRC = tRC(min); tCK = tCK(min); DQ, DM and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles; CS = high between valid commands.	170	140	120	mA
IDD1	Operating current for one bank operation; one bank open, BL = 4, tRC = tRC(min), tCK = tCK(min), Iout=0mA, Address and control inputs changing once per clock cycle.	160	130	110	mA
IDD2P	Precharge power-down standby current; all banks idle; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	3	3	3	mA
IDD2F	Precharge floating standby current; CS VIH(min); all banks idle; CKE VIH(min); tCK = tCK(min); address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS and DM	115	95	80	mA
IDD3P	Active power-down standby current; one bank active; power-down mode; CKE VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS and DM	50	40	35	mA
IDD3N	Active standby current; CS VIH(min); CKE VIH(min); one bank active; tRC = tRAS(max); tCK = tCK(min); DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	160	130	110	mA
IDD4R	Operating current for burst read; burst length = 2; reads; continuous burst; one bank active; address and control inputs changing once per clock cycle; tCK = tCK(min); 50% of data changing on every transfer; IOUT = 0mA	215	180	150	mA
IDD4W	Operating current for burst write; burst length = 2; writes; continuous burst; one bank active address and control inputs changing once per clock cycle; tCK = tCK(min); DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every transfer	165	135	115	mA
IDD5	Auto refresh current; tRC = tRFC(min);	225	180	155	mA
IDD6	Self refresh current; CKE 0.2V;	3	3	3	mA
IDD7	Operating current for four bank operation; four bank interleaving READs (BL=4) with auto precharge; tRC = tRC(min), tCK = tCK(min); Address and control inputs change only during ACTIVE, READ, or WRITE commands	425	350	295	mA

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = 2.5V ± 0.125V@-4)

PARAMETER	SYMBOL	-4		UNITS
		MIN	MAX	
DQ output access time for CLK,/CLK	tAC	-0.7	0.7	ns
DQS output access time for CLK,/CLK	tDQSCK	-0.6	0.6	ns
CLK high-level width	tCH	0.45	0.55	tCK
CLK low-level width	tCL	0.45	0.55	tCK
CLK half period	tHP	min (tCL,tCH)	–	ns
CLK cycle time CL=4	tCK(4)	4	8	ns
CL=3	tCK(3)	5	8	ns
CL=2.5	tCK(2.5)	–	–	ns
CL=2	tCK(2)	–	–	ns
DQ and DM input hold time	tDH	0.4	–	ns
DQ and DM input setup time	tDS	0.4	–	ns
Control & Address input pulse width (for each input)	tIPW	2.2	–	ns
DQ and DM input pulse width (for each input)	tDIPW	1.75	–	ns
DQ & DQS high-impedance time from CLK,/CLK	tHZ	–	0.7	ns
DQ & DQS low--impedance time from CLK,/CLK	tLZ	-0.7	–	ns
DQS--DQ Skew, DQS to last DQ valid, per group, per access	tDQSQ	–	0.4	ns
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	–	ns
Data Hold Skew Factor	tQHS	–	0.5	ns
Write command to first DQS latching transition	tDQSS	0.72	1.28	tCK
DQS input high pulse width	tDQSH	0.35	–	tCK
DQS input low pulse width	tDQSL	0.35	–	tCK
DQS falling edge to CLK setup time	tDSS	0.2	–	tCK
DQS falling edge hold time from CLK	tDSH	0.2	–	tCK
MODE REGISTER SET command cycle time	tMRD	2	–	tCK
Write preamble setup time	tWPRES	0.25	–	tCK
Write postamble	tWPST	0.4	0.6	tCK
Write preamble	tWPRE	0.25	–	tCK
Address and Control input hold time (fast slew rate)	tIHF	0.6	–	ns
Address and Control input setup time (fast slew rate)	tISF	0.6	–	ns
Address and Control input hold time (slow slew rate)	tIH	0.7	––	ns
Address and Control input setup time (slow slew rate)	tIS	0.7	–	ns
Read preamble	tRPRE	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	tCK
ACTIVE to PRECHARGE command	tRAS	40	70,000	ns

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = 2.5V ± 0.125V@-4)

PARAMETER	SYMBOL	-4		UNITS
		MIN	MAX	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	55	–	ns
Auto Refresh to Active/Auto	tRFC	70	–	ns
ACTIVE to READ or WRITE delay	tRCD	15	–	ns
PRECHARGE command period	tRP	15	–	ns
Active to Autoprecharge Delay	tRAP	15	–	ns
ACTIVE bank A to ACTIVE bank B command	tRRD	10	–	ns
Write recovery time	tWR	15	–	ns
Auto Precharge write recovery + precharge time	tDAL	tWR+tRP	–	tCK
Internal Write to Read Command Delay	tWTR	2	–	tCK
Exit self refresh to non-READ	tXSNR	70	–	ns
Exit self refresh to READ command	tXSRD	200	–	tCK
Average Periodic Refresh Interval	tREFI	–	7.8	µs

AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = 2.5V ± 0.2V@-5, -6)

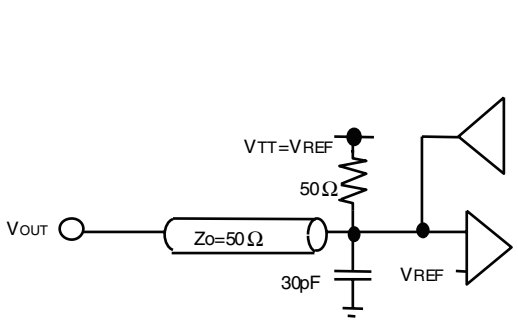
PARAMETER	SYMBOL	-5		-6		UNITS
		MIN	MAX	MIN	MAX	
DQ output access time for CLK,/CLK	tAC	-0.7	0.7	-0.7	0.7	ns
DQS output access time for CLK,/CLK	tDQSCK	-0.6	0.6	-0.6	0.6	ns
CLK high-level width	tCH	0.45	0.55	0.45	0.55	tCK
CLK low-level width	tCL	0.45	0.55	0.45	0.55	tCK
CLK half period	tHP	min (tCL,tCH)	–	min (tCL,tCH)	–	ns
CLK cycle time CL=4	tCK(4)	5	8	6	12	ns
CL=3	tCK(3)	5	8	6	12	ns
CL=2.5	tCK(2.5)	6	12	6	12	ns
CL=2	tCK(2)	7.5	12	7.5	12	ns
DQ and DM input hold time	tDH	0.4	–	0.45	–	ns
DQ and DM input setup time	tDS	0.4	–	0.45	–	ns
Control & Address input pulse width (for each input)	tIPW	2.2	–	2.2	–	ns
DQ and DM input pulse width (for each input)	tDIPW	1.75	–	1.75	–	ns
DQ & DQS high-impedance time from CLK,/CLK	tHZ	–	0.7	–	0.7	ns
DQ & DQS low--impedance time from CLK,/CLK	tLZ	-0.7	–	-0.7	–	ns
DQS--DQ Skew, DQS to last DQ valid, per group, per access	tDQSQ	–	0.4	–	0.45	ns
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	–	tHP-tQHS	–	ns
Data Hold Skew Factor	tQHS	–	0.5	–	0.55	ns
Write command to first DQS latching transition	tDQSS	0.72	1.28	0.75	1.25	tCK
DQS input high pulse width	tDQSH	0.35	–	0.35	–	tCK
DQS input low pulse width	tDQSL	0.35	–	0.35	–	tCK
DQS falling edge to CLK setup time	tDSS	0.2	–	0.2	–	tCK
DQS falling edge hold time from CLK	tDSH	0.2	–	0.2	–	tCK
MODE REGISTER SET command cycle time	tMRD	2	–	2	–	tCK
Write preamble setup time	tWPRES	0.25	–	0.25	–	tCK
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK
Write preamble	tWPRE	0.25	–	0.25	–	tCK
Address and Control input hold time (fast slew rate)	tIHF	0.6	–	0.75	–	ns
Address and Control input setup time (fast slew rate)	tISF	0.6	–	0.75	–	ns
Address and Control input hold time (slow slew rate)	tIH	0.7	–	0.8	-–	ns
Address and Control input setup time (slow slew rate)	tIS	0.7	–	0.8	–	ns
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK
ACTIVE to PRECHARGE command	tRAS	40	70,000	42	120,000	ns

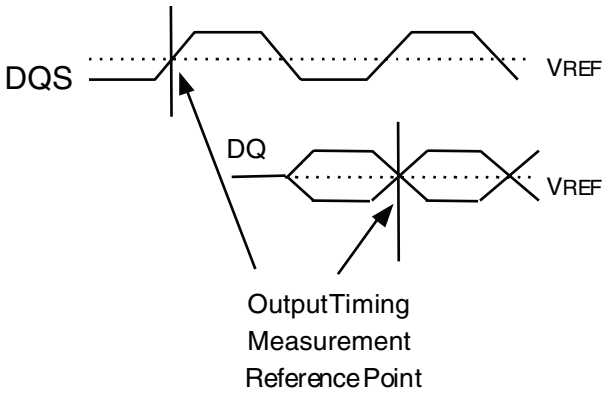
AC TIMING REQUIREMENTS

Absolute Specifications (VDD, VDDQ = 2.5V ± 0.2 V@-5, -6)

PARAMETER	SYMBOL	-5		-6		UNITS
		MIN	MAX	MIN	MAX	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	55	–	60	–	ns
Auto Refresh to Active/Auto	tRFC	70	–	72	–	ns
ACTIVE to READ or WRITE delay	tRCD	15	–	18	–	ns
PRECHARGE command period	tRP	15	–	18	–	ns
Active to Autoprecharge Delay	tRAP	0.5	–	18	–	ns
ACTIVE bank A to ACTIVE bank B command	tRRD	10	–	12	–	ns
Write recovery time	tWR	15	–	15	–	ns
Auto Precharge write recovery + precharge time	tDAL	tWR+tRP	–	tWR+tRP	–	tCK
Internal Write to Read Command Delay	tWTR	2	–	2	–	tCK
Exit self refresh to non-READ	tXSNR	70	–	70	–	ns
Exit self refresh to READ command	tXSRD	200	–	200	–	tCK
Average Periodic Refresh Interval	tREFI	–	7.8	–	7.8	µs

Output Load Condition





Notes

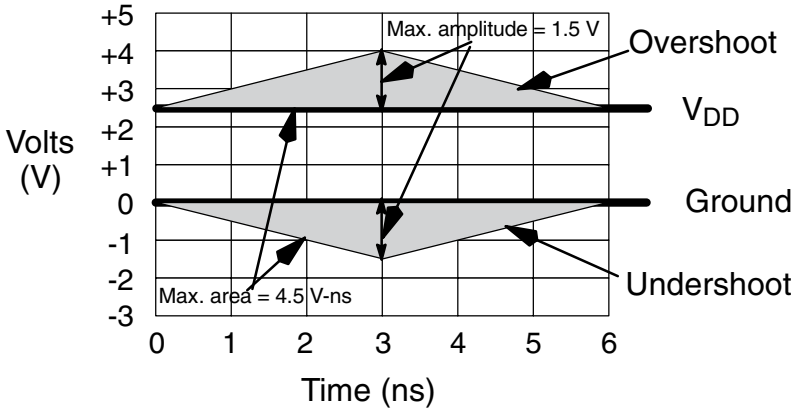
1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized.
11. This parameter is sampled. VddQ = 2.5V+0.2V, Vdd = 2.5V + 0.2V , f = 100 MHz, T_A = 25°C, VOUT(DC) = VddQ/2, VOUT(PEAK TO PEAK) = 25mV. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE< 0.3VddQ is recognized as LOW.
14. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.
19. For command/address and CK & /CK slew rate > 1.0V/ns.
20. Min (tCL,tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.

OUTPUT SLEW RATE CHARACTERISTICS

Slew Rate Characteristic	Typical Range (V/ns)	Min (V/ns)	Max (V/ns)
Pullup Slew Rate	1.2-2.5	0.7	5.0
Pulldown Slew Rate	1.2-2.5	0.7	5.0

AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR ADDRESS AND CONTROL PINS

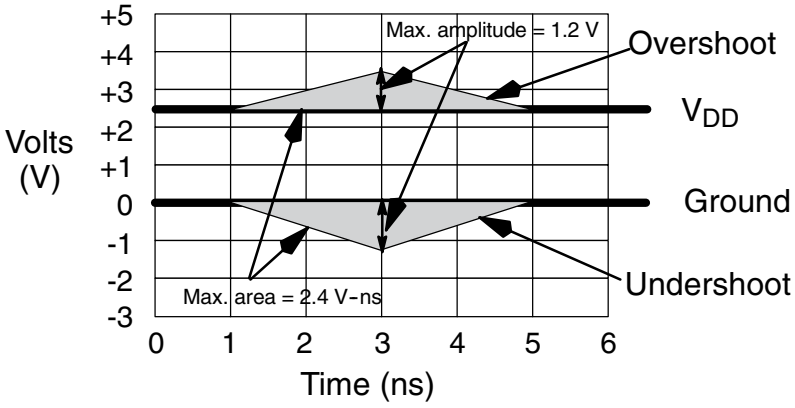
Parameter	Max	Units
Peak amplitude allowed for overshoot	1.5	V
Peak amplitude allowed for undershoot	1.5	V
Area between the overshoot signal and VDD must be less than or equal to (see figure below)	4.5	V-ns
Area between the undershoot signal and GND must be less than or equal to (see figure below)	4.5	V-ns



Address and Control AC Overshoot and Undershoot Definition

OVERSHOOT/UNDERSHOOT SPECIFICATION FOR DATA, STROBE, AND MASK PINS

Parameter	Max	Units
Peak amplitude allowed for overshoot	1.2	V
Peak amplitude allowed for undershoot	1.2	V
Area between the overshoot signal and VDD must be less than or equal to (see figure below)	2.4	V-ns
Area between the undershoot signal and GND must be less than or equal to (see figure below)	2.4	V-ns



DQ/DM/DQS AC Overshoot and Undershoot Definition

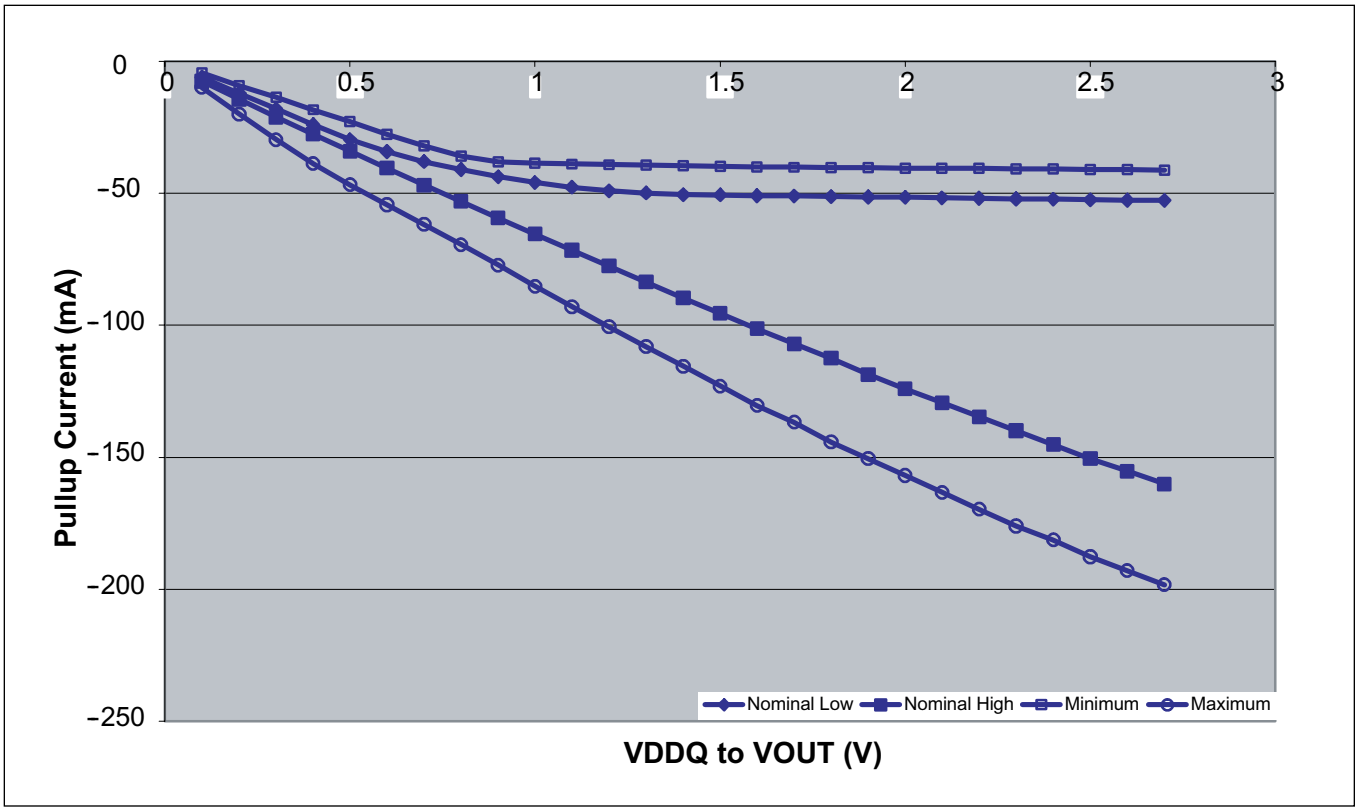
DRIVER CHARACTERISTICS

DDR SDRAM output driver characteristics are defined for full and weak drive strength operation as selected in the Extended Mode Register bit A1. The table below shows the data in a tabular format suitable for input into simulation tools. The following figures show the driver strength characteristics graphically.

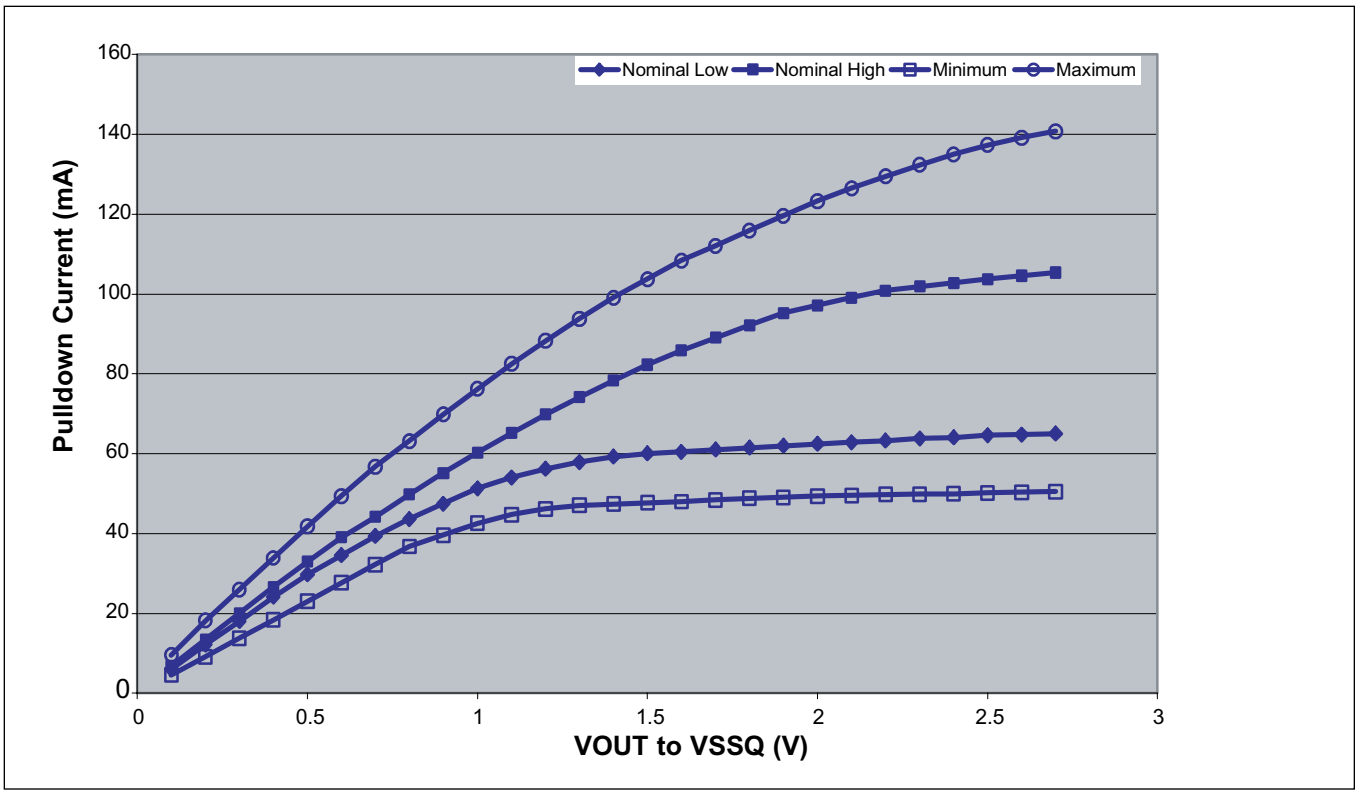
Full Strength Driver Characteristics

Voltage (V)	Pull Down Current (mA)				Pull Up Current (mA)			
	Nominal Low	Nominal High	Min.	Max.	Nominal Low	Nominal High	Min.	Max.
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	10.0
0.2	12.2	13.5	9.2	18.2	12.2	14.5	-9.2	20.0
0.3	18.1	20.1	13.8	26.0	18.1	21.2	13.8	29.8
0.4	24.1	26.6	18.4	33.9	24.0	27.7	18.4	38.8
0.5	29.8	33.0	23.0	41.8	29.8	34.1	23.0	46.8
0.6	34.6	39.1	27.7	49.4	34.3	40.5	27.7	54.4
0.7	39.4	44.2	32.2	56.8	38.1	46.9	32.2	61.8
0.8	43.7	49.8	36.8	63.2	41.1	53.1	36.0	69.5
0.9	47.5	55.2	39.6	69.9	43.8	59.4	38.2	77.3
1.0	51.3	60.3	42.6	76.3	46.0	65.5	38.7	85.2
1.1	54.1	65.2	44.8	82.5	47.8	71.6	39.0	93.0
1.2	56.2	69.9	46.2	88.3	49.2	77.6	39.2	100.6
1.3	57.9	74.2	47.1	93.8	50.0	83.6	39.4	108.1
1.4	59.3	78.4	47.4	99.1	50.5	89.7	39.6	115.5
1.5	60.1	82.3	47.7	103.8	50.7	95.5	39.9	123.0
1.6	60.5	85.9	48.0	108.4	51.0	101.3	40.1	130.4
1.7	61.0	89.1	48.4	112.1	51.1	107.1	40.2	136.7
1.8	61.5	92.2	48.9	115.9	51.3	112.4	40.3	144.2
1.9	62.0	95.3	49.1	119.6	51.5	118.7	40.4	150.5
2.0	62.5	97.2	49.4	123.3	51.6	124.0	40.5	156.9
2.1	62.9	99.1	49.6	126.5	51.8	129.3	40.6	163.2
2.2	63.3	100.9	49.8	129.5	52.0	134.6	40.7	169.6
2.3	63.8	101.9	49.9	132.4	52.2	139.9	40.8	176.0
2.4	64.1	102.8	50.0	135.0	52.3	145.2	40.9	181.3
2.5	64.6	103.8	50.2	137.3	52.5	150.5	41.0	187.6
2.6	64.8	104.6	50.4	139.2	52.7	155.3	41.1	192.9
2.7	65.0	105.4	50.5	140.8	52.8	160.1	41.2	198.2

Pullup characteristics for Full Strength Output Driver



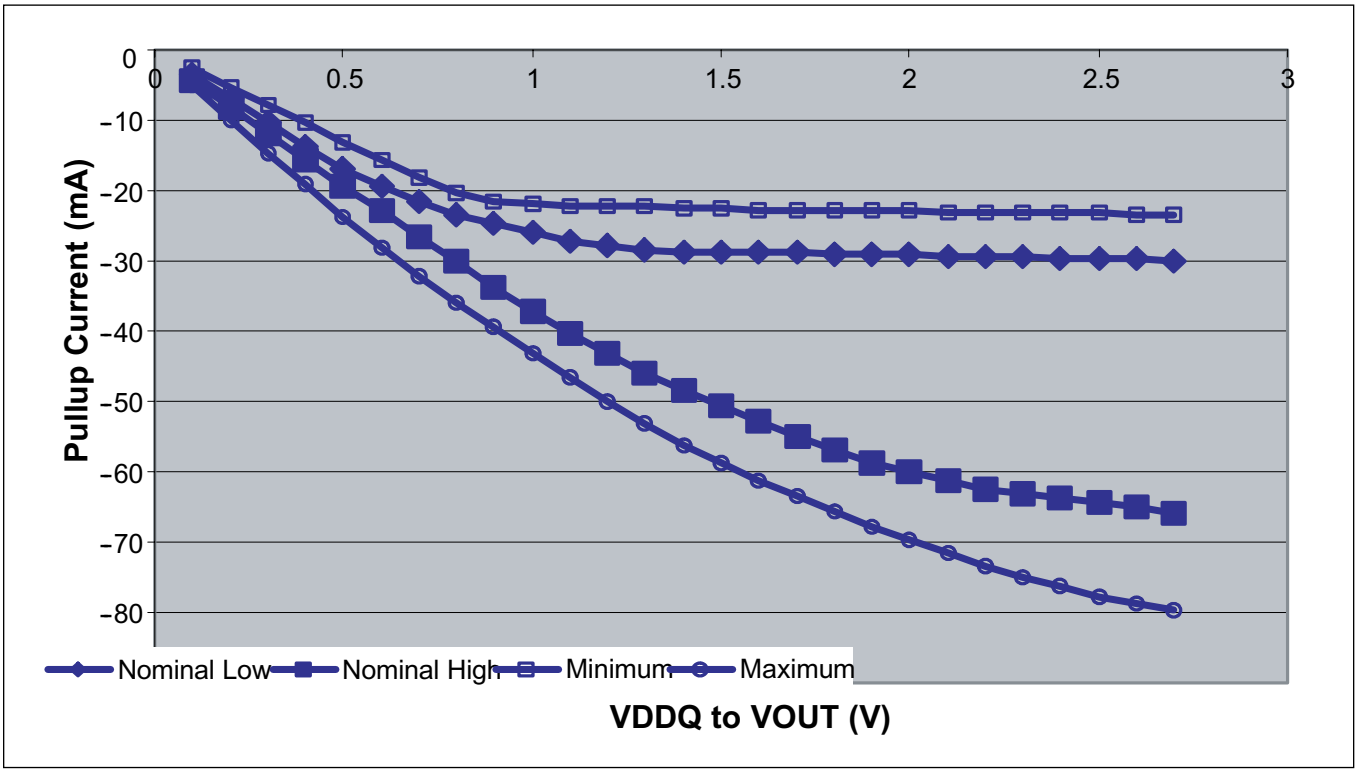
Pulldown characteristics for Full Strength Output Driver



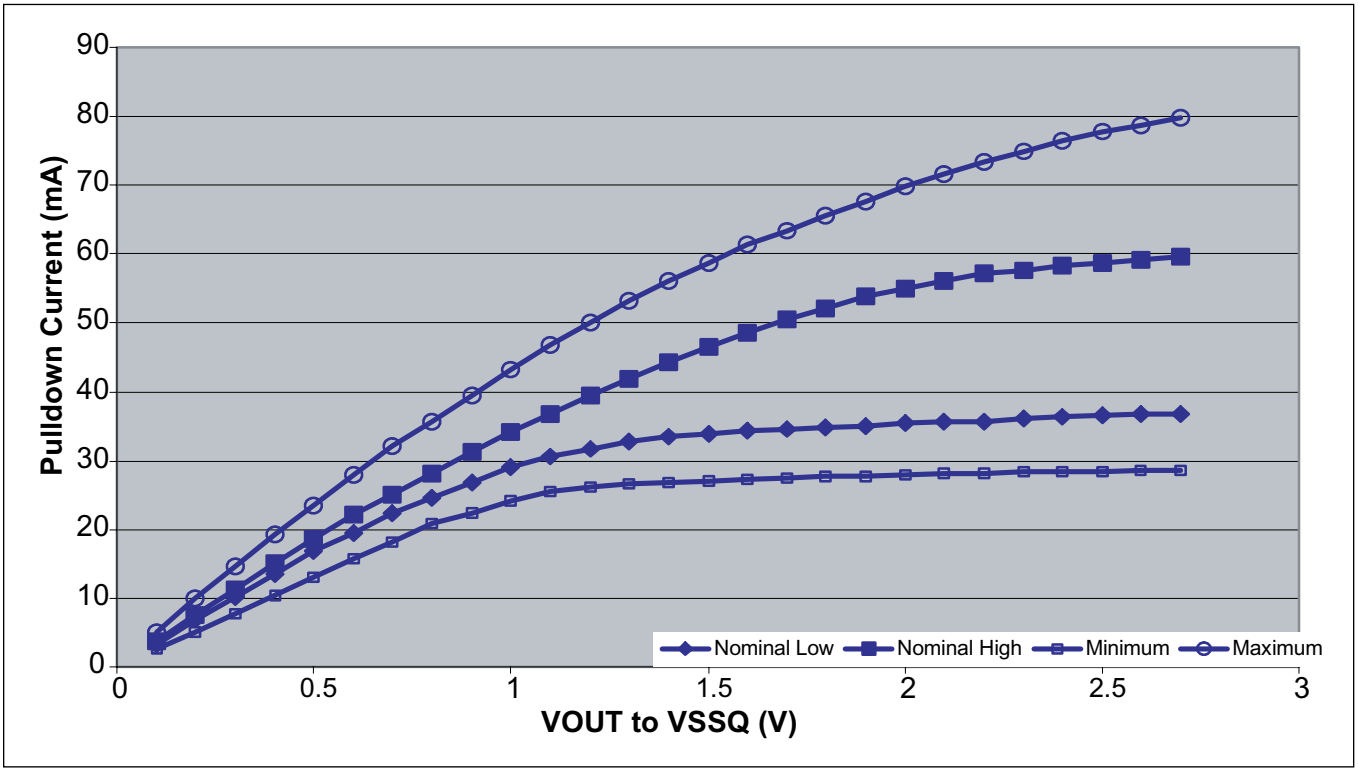
Weak Driver Characteristics

Voltage (V)	Pull Down Current (mA)				Pull Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5	-3.5	-4.3	-2.6	-5
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	10.3	-12	-7.8	14.6
0.4	13.6	15.1	10.4	19.2	13.6	15.7	10.4	19.2
0.5	16.9	18.7	13	23.6	16.9	19.3	-13	23.6
0.6	19.6	22.1	15.7	28	19.4	22.9	15.7	-28
0.7	22.3	25	18.2	32.2	21.5	26.5	18.2	32.2
0.8	24.7	28.2	20.8	35.8	23.3	30.1	20.4	35.8
0.9	26.9	31.3	22.4	39.5	24.8	33.6	21.6	39.5
1	29	34.1	24.1	43.2	-26	37.1	21.9	43.2
1.1	30.6	36.9	25.4	46.7	27.1	40.3	22.1	46.7
1.2	31.8	39.5	26.2	50	27.8	43.1	22.2	50.0
1.3	32.8	42	26.6	53.1	28.3	45.8	22.3	53.1
1.4	33.5	44.4	26.8	56.1	28.6	48.4	22.4	56.1
1.5	34	46.6	27	58.7	28.7	50.7	22.6	58.7
1.6	34.3	48.6	27.2	61.4	28.9	52.9	22.7	61.4
1.7	34.5	50.5	27.4	63.5	28.9	-55	22.7	63.5
1.8	34.8	52.2	27.7	65.6	-29	56.8	22.8	65.6
1.9	35.1	53.9	27.8	67.7	29.2	58.7	22.9	67.7
2	35.4	55	28	69.8	29.2	-60	22.9	69.8
2.1	35.6	56.1	28.1	71.6	29.3	61.2	-23	71.6
2.2	35.8	57.1	28.2	73.3	29.5	62.4	-23	73.3
2.3	36.1	57.7	28.3	74.9	29.5	63.1	23.1	74.9
2.4	36.3	58.2	28.3	76.4	29.6	63.8	23.2	76.4
2.5	36.5	58.7	28.4	77.7	29.7	64.4	23.2	77.7
2.6	36.7	59.2	28.5	78.8	29.8	65.1	23.3	78.8
2.7	36.8	59.6	28.6	79.7	29.9	65.8	23.3	79.7

Pullup Characteristics for Weak Output Driver



Pulldown Characteristics for Weak Output Driver



COMMANDS TRUTH TABLES

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and CK going low). Truth Table shows basic timing parameters for all commands.

Truth Tables for Commands provide a quick reference of available commands. Table "Current State" provides the current state / next state information. This is followed by a detailed description of each command.

TRUTH TABLE - Commands

NAME (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7, 12
MODE REGISTER SET	L	L	L	L	Op-Code	2

TRUTH TABLE - DM Operations

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0--BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0--BA1 are reserved; A0-A11 provide the op--code to be written to the selected Mode Register.
3. BA0--BA1 provide bank address and A0-A11 provide row address.
4. BA0--BA1 provide bank address; A0-A7 provide column address; AP HIGH enables the auto precharge feature (nonpersistent), AP LOW disables the auto precharge feature.
5. AP LOW: BA0--BA1 determine which bank is precharged. AP HIGH: all banks are precharged and BA0--BA1 are ”Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are ”Don’t Care” except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data, provided coincident with the corresponding data.
11. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
12. VREF must be maintained during Self Refresh operation.

TRUTH TABLE - CKE

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power-Down	X	Maintain Power-Down	
L	L	Self Refresh	X	Maintain Self Refresh	7
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
L	H	Self Refresh	DESELECT or NOP	Exit Self Refresh	5, 7
H	L	All Banks Idle	DESELECT or NOP	Precharge Power- Down Entry	
H	L	Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See next Truth Table		

NOTE:
1. CKEn is the logic state of CKE at clock edge n; CKEn--1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying any executable command, for the DLL to lock.
6. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
7. VREF must be maintained during Self Refresh operation.

TRUTH TABLE - Current State Bank n -- Command to Bank n

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start precharge)	8, 11

NOTE:

1. This table applies when CKEn--1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table is bank--specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the "row active" state.
   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRFC is met, the DDR SDRAM will be in the "all banks idle" state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the DDR SDRAM will be in the "all banks idle" state.
   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank--specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank--specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank--specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,
13. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

TRUTH TABLE - CURRENT STATE BANK n - COMMAND TO BANK m

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start WRITE burst)	3a, 7, 9
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	3a, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	3a, 7
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn--1 was HIGH and CKEn is HIGH and after tXSNR or tXSRD has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled and has not yet terminated or been terminated.
   Read with Auto-Precharge Enabled: See following text, notes 3a, 3b, and 3c:
   Write with Auto-Precharge Enabled: See following text, notes 3a, 3b, and 3c:

3a. For devices which do not support the optional “concurrent auto precharge” feature, the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins.During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

3b. For devices which do support the optional “concurrent auto precharge” feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided.)
3c. The minimum delay from a read or write command with auto precharge enable, to a command to a different bank, is summarized below, for both cases of “concurrent auto precharge,” supported or not:
4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of data output, otherwise a Burst Terminate must be used to the READ prior to asserting a WRITE command..
10. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

OPERATION

DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the DDR SDRAM.

The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION

The NO OPERATION (NOP) command is used to perform a NOP to a DDR SDRAM that is selected ($\overline{CS}$ = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The Mode Register and the Extended Mode Register are loaded via the address inputs. See "Mode Register" and the "Extended Mode Register" descriptions for further details.

The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

Before any READ or WRITE commands can be issued to a bank in the DDR SDRAM, a row in that bank must be opened. This is accomplished by the ACTIVE command: BA0 and BA1 select the bank, and the address inputs select the row to be activated. More than one bank can be active at anytime.

Once a row is open, a READ or WRITE command could be issued to that row, subject to the tRCD specification.

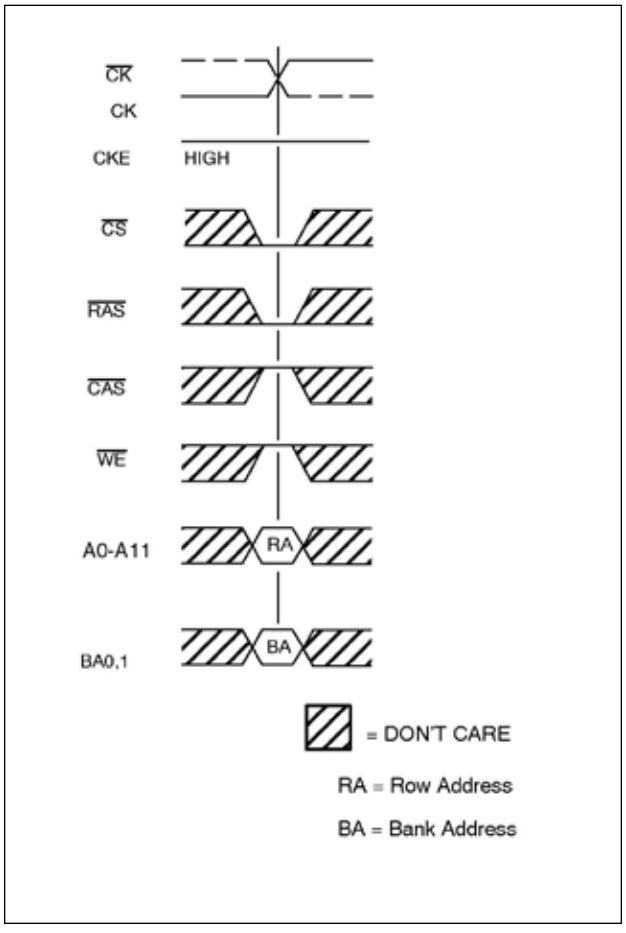
A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive ACTIVE commands on the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by tRRD. Bank Activation Command Cycle shows the tRCD and tRRD definition.

The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

A PRECHARGE command (or READ or WRITE command with Auto Precharge) must be issued before opening a different row in the same bank.

Bank Activation Command Cycle



READ

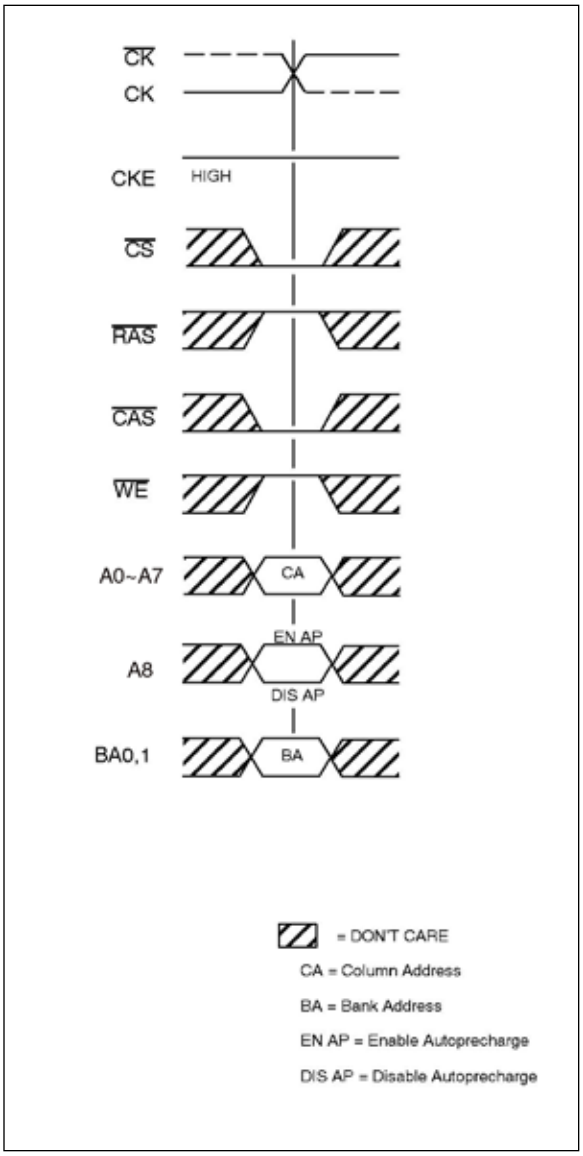
The READ command is used to initiate a burst read access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A8 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the read burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

The basic Read timing parameters for DQs are shown in Figure Basic Read Timing Parameters they apply to all Read operations.

During Read bursts, DQS is driven by the DDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in Figure Read Burst Showing CAS Latency with a CAS latency of 2 and 3.

Upon completion of a read burst, assuming no other READ command has been initiated, the DQs will go to High-Z.

READ Command



READ to READ

Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).

A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses within a page or pages can be performed as shown in Figure Random Read Bursts.

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure Read to Write for the case of nominal tDQSS.

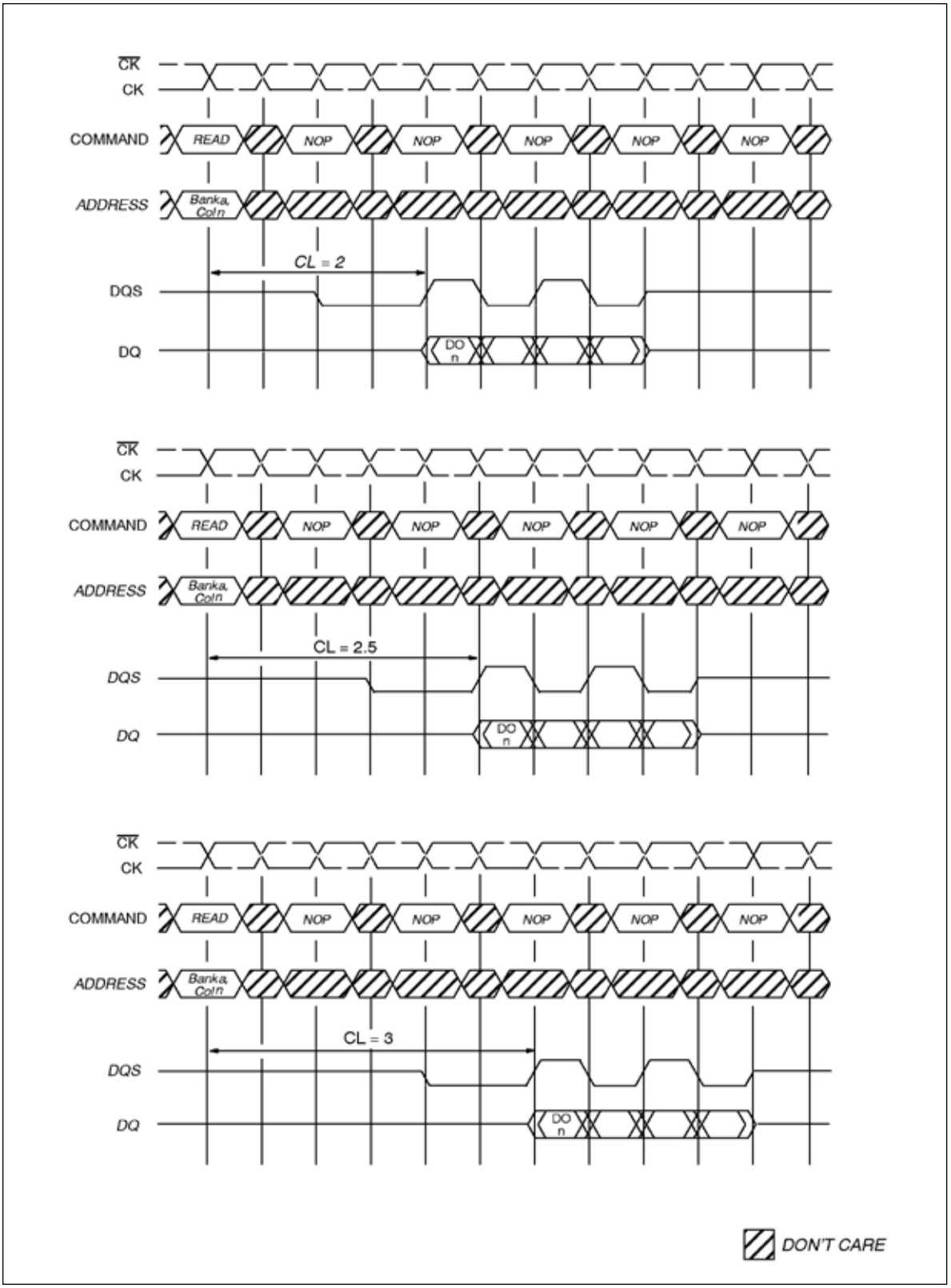
READ to PRECHARGE

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs.

Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.

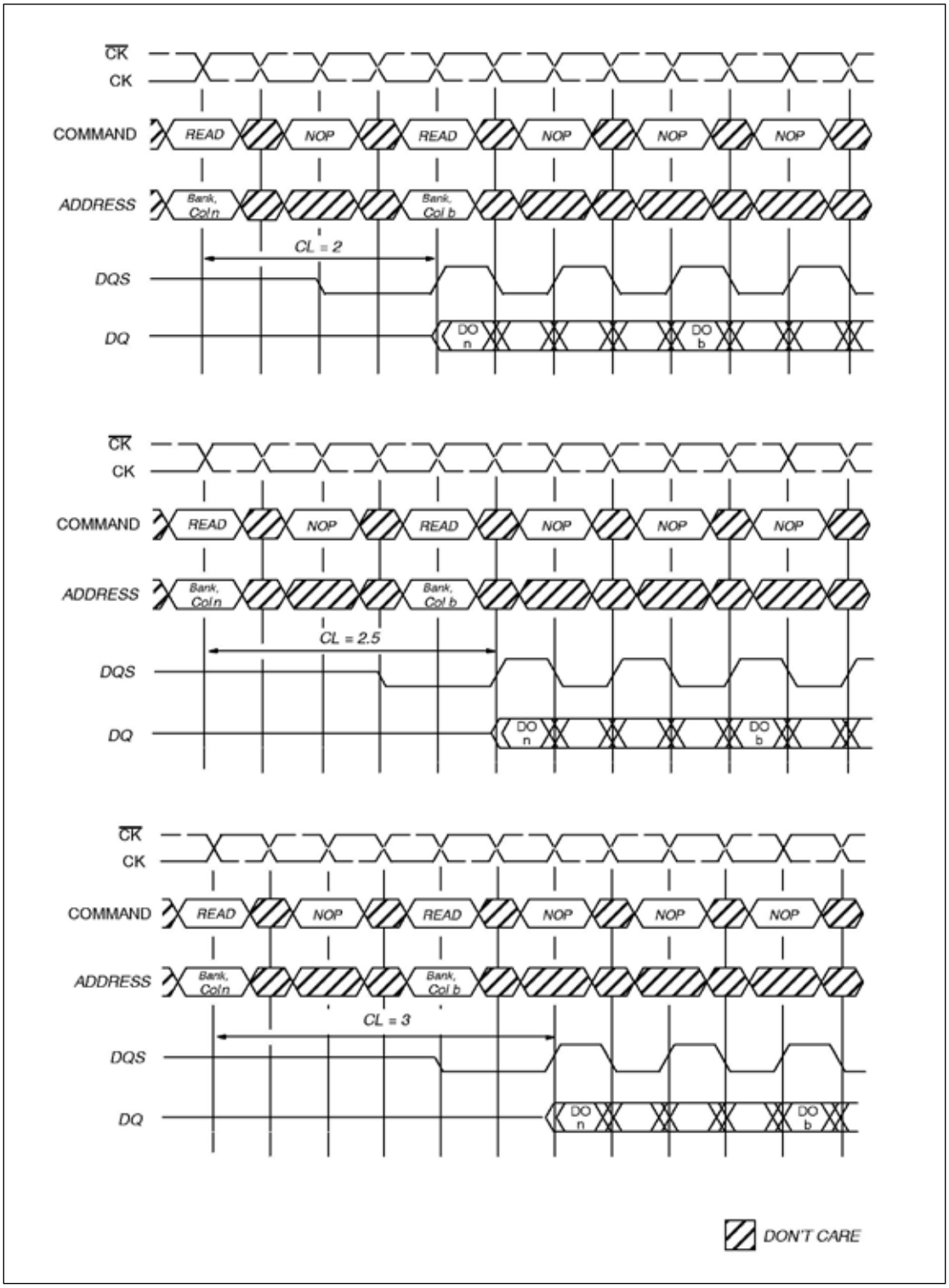
In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

Read Burst Showing CAS Latency



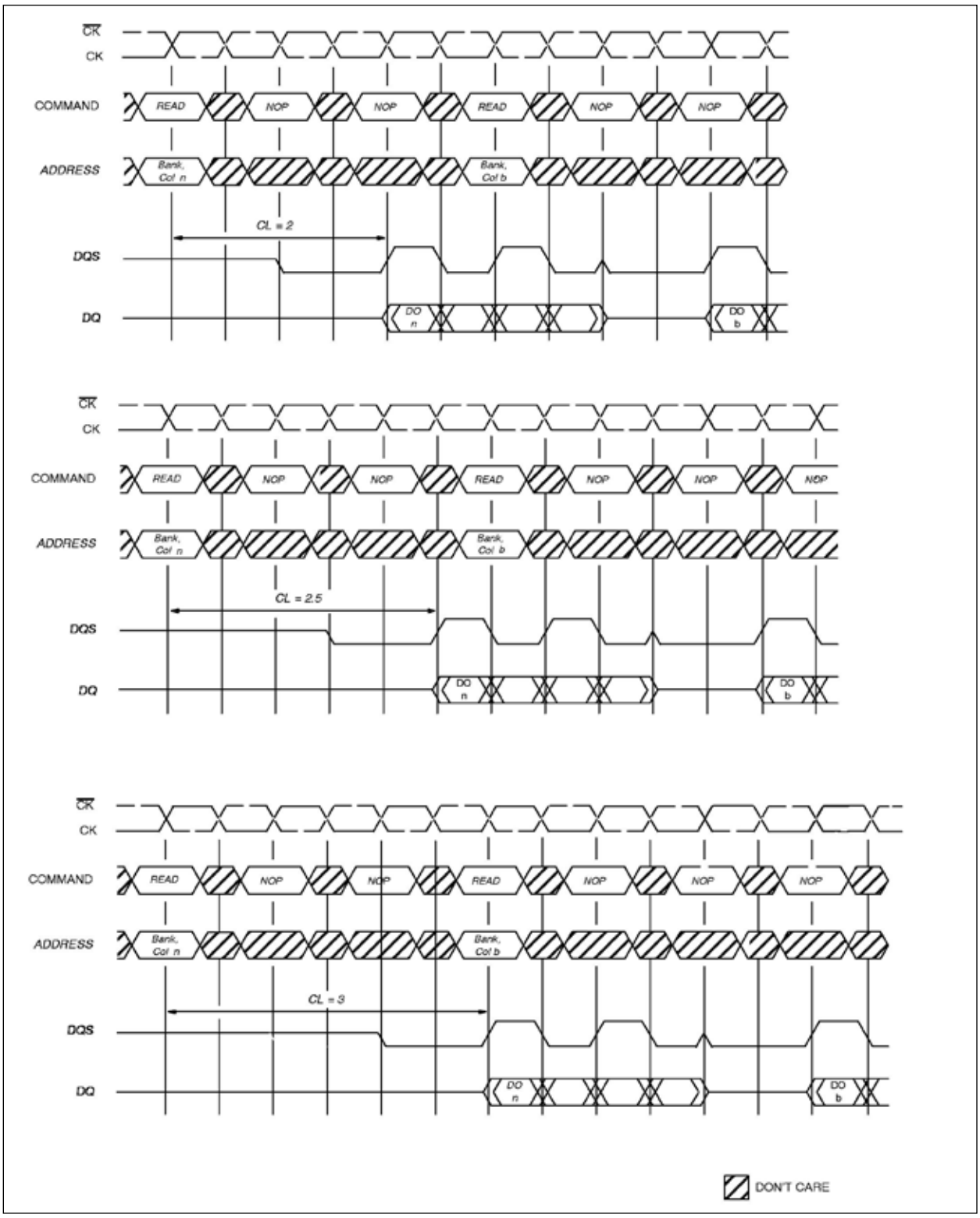
Notes:
DO n = Data Out from column n
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n

Consecutive Read Bursts



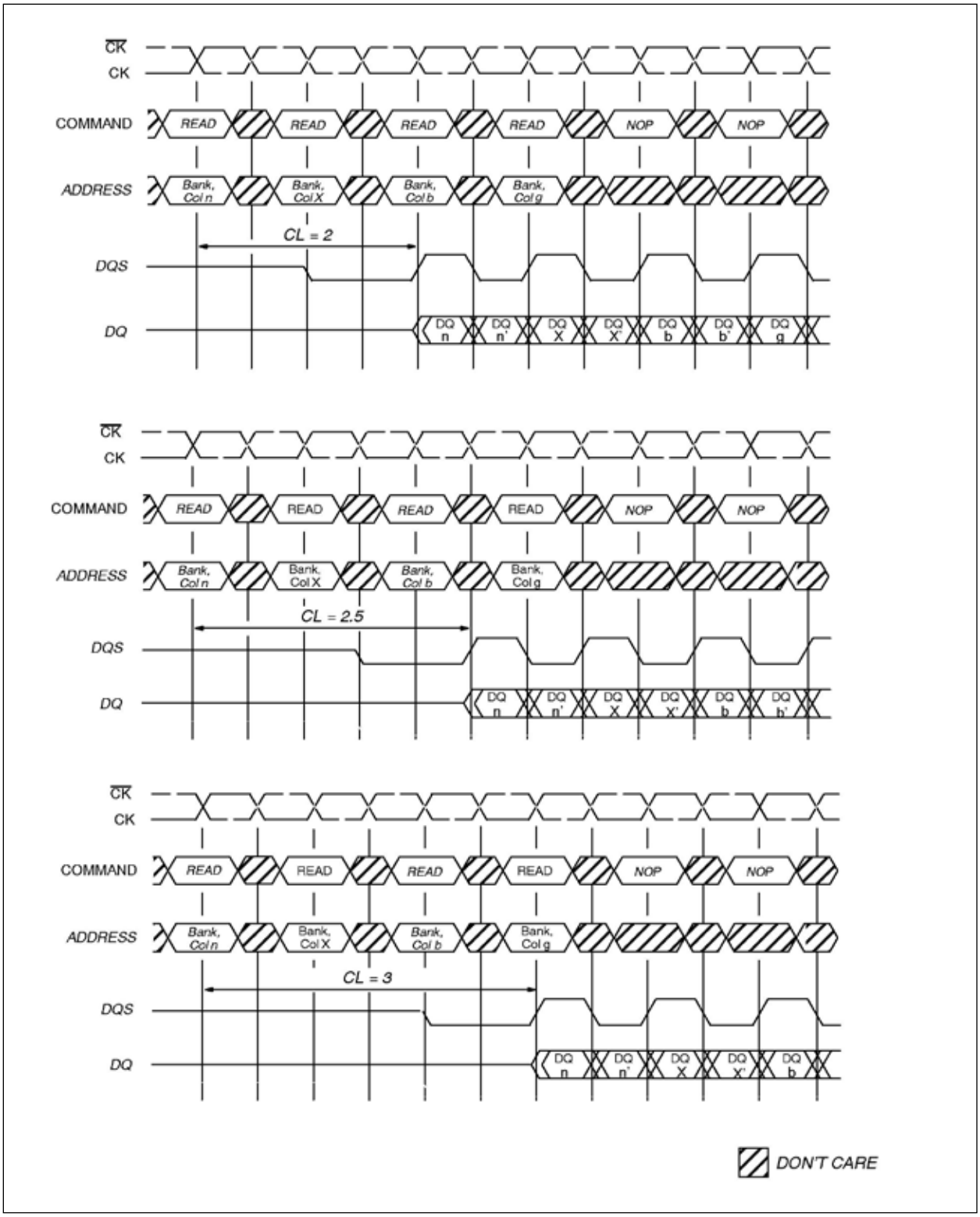
Notes:
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b
Read commands shown must be to the same device

Non-Consecutive Read Bursts



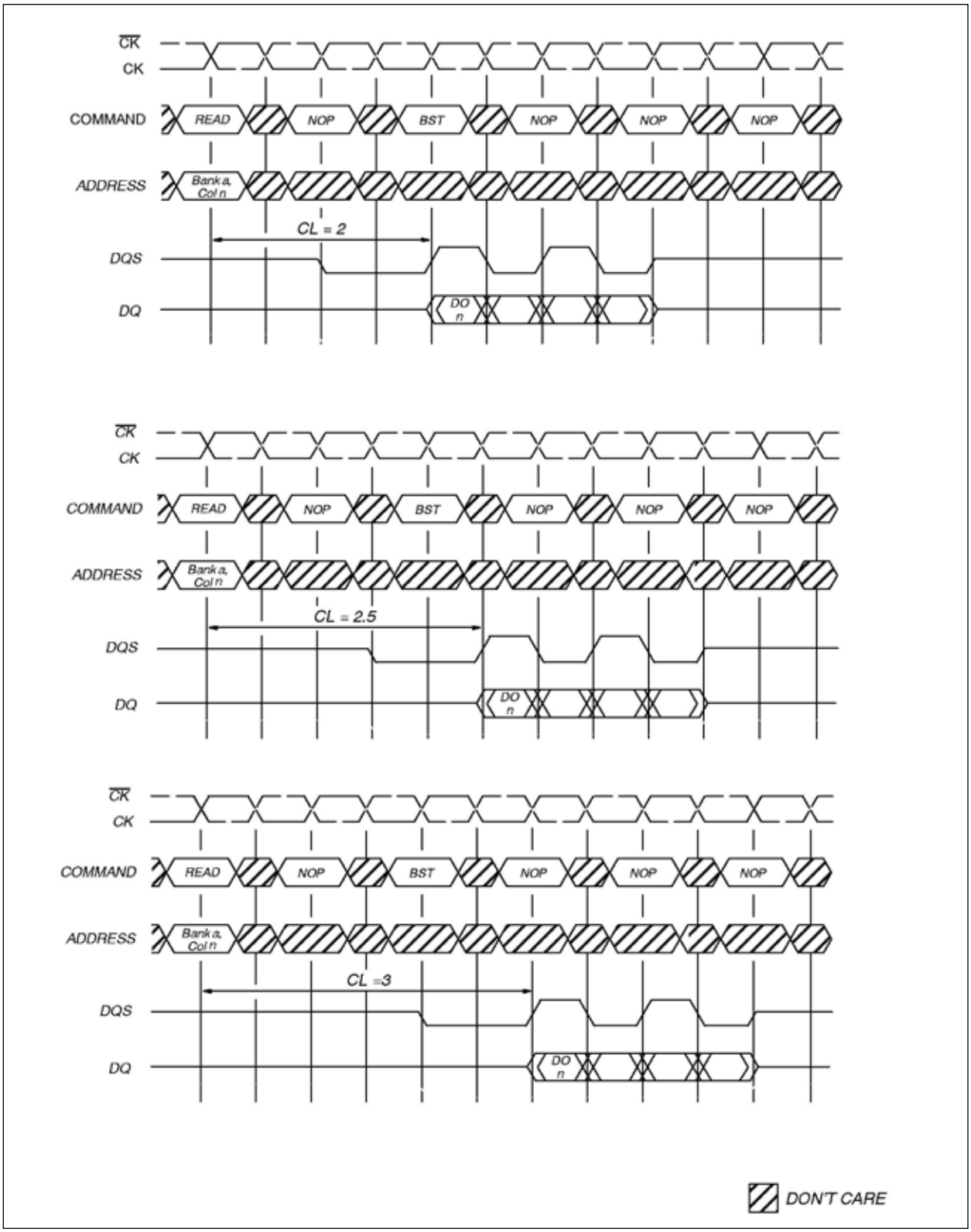
Notes:
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO b)

Random Read Bursts



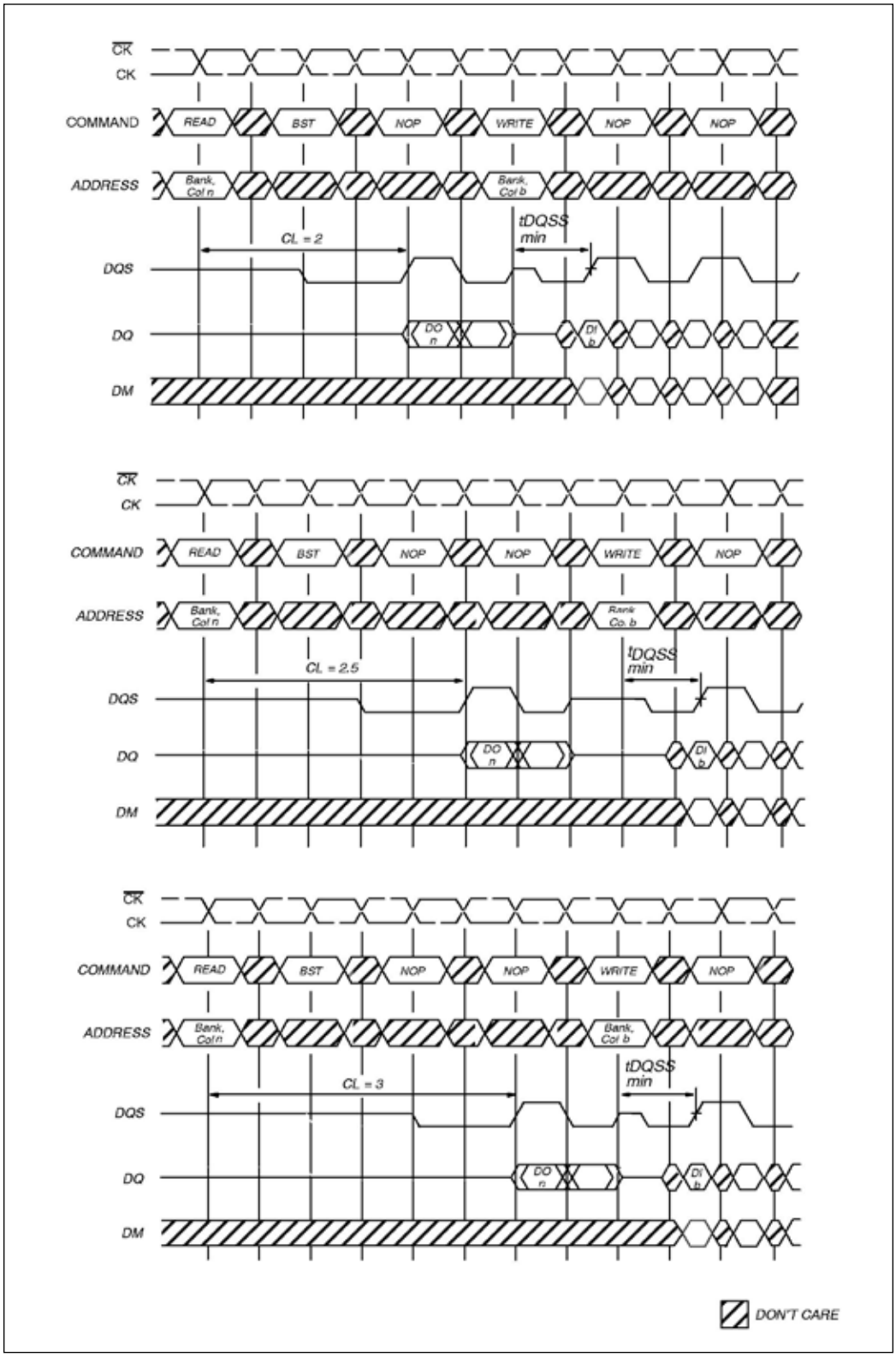
Notes:
DO n, etc. = Data Out from column n, etc.
n' , etc. = the next Data Out following DO n, etc. according to the programmed burst order
Burst Length = 2, 4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted,
Reads are to active rows in any banks

Terminating a Read Burst



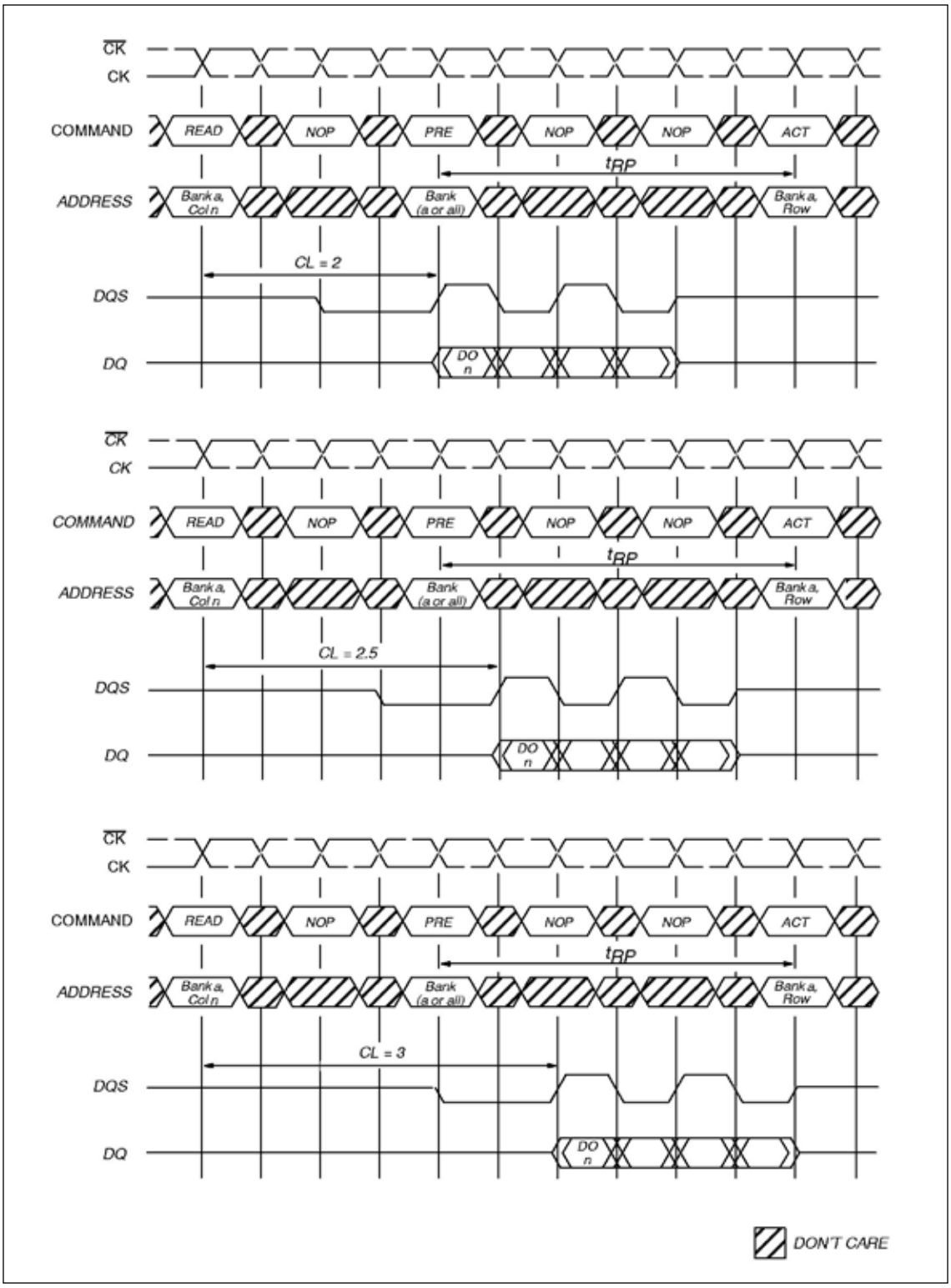
Notes:
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

Read To Write



Notes:
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)
1 subsequent element of Data Out appears in the programmed order following DO n
Data In elements are applied following DI b in the programmed order

Read To Precharge



Notes:
DO n = Data Out from column n
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
3 subsequent elements of Data Out appear in the programmed order following DO n
Precharge may be applied at (BL/2) tCK after the READ command.
Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
The Active command may be applied if tRC has been met.

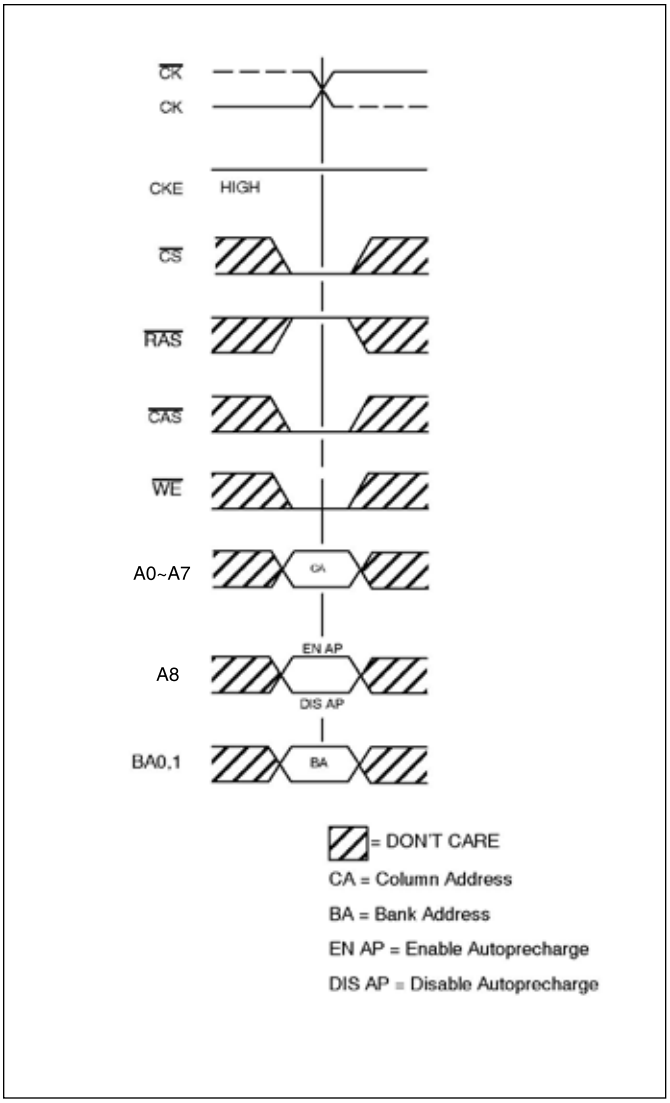
WRITE

The WRITE command is used to initiate a burst write access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A8 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the write burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

Basic Write timing parameters for DQs are shown in Figure Basic Write Timing Parameters; they apply to all Write operations.

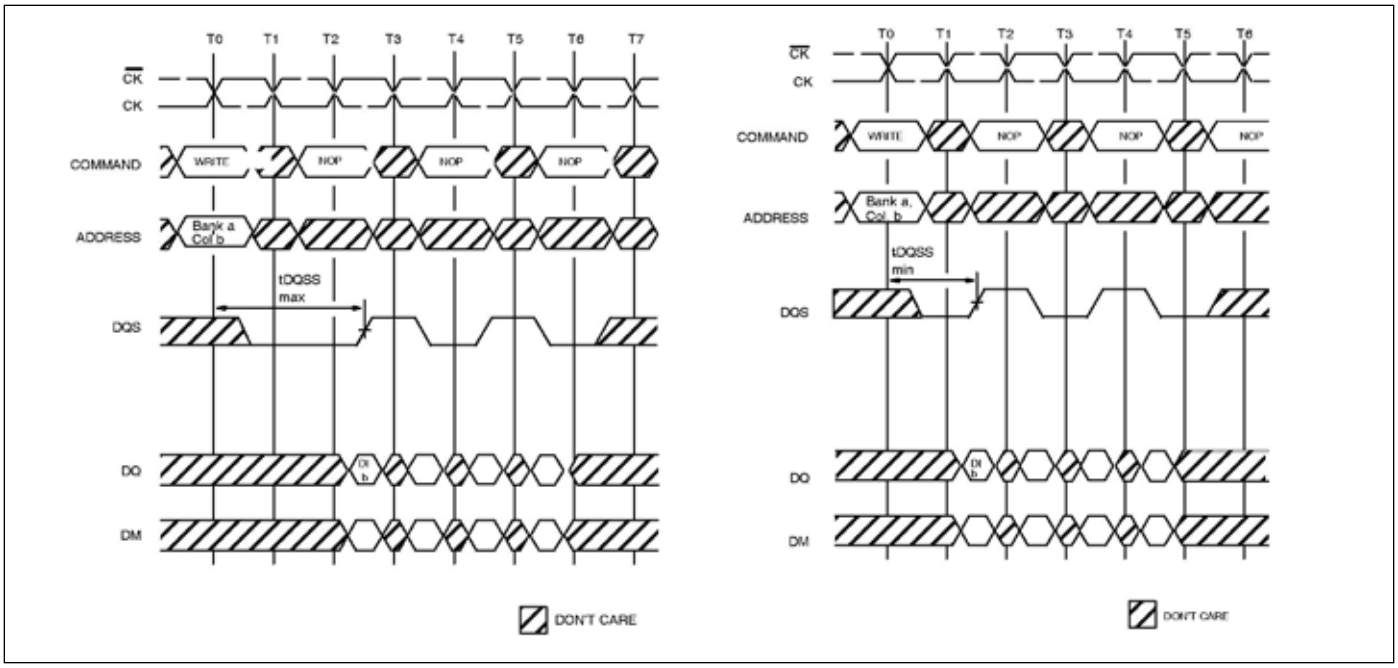
Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.

WRITE command



During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range - from 75% to 125% of a clock cycle. The figure below shows the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain high-Z and any additional input data will be ignored.

Write Burst (min. and max. tDQSS)



Notes:
DI b = Data in for column b
3 subsequent elements of Data IN are applied in the programmed order following Di b
A non--interrupted burst of 4 is shown
AP is LOW with the WRITE command (AUTO PRECHARGE disabled)

WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.

The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.

WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, tWTR should be met as shown in Non-interrupting Write to Read.

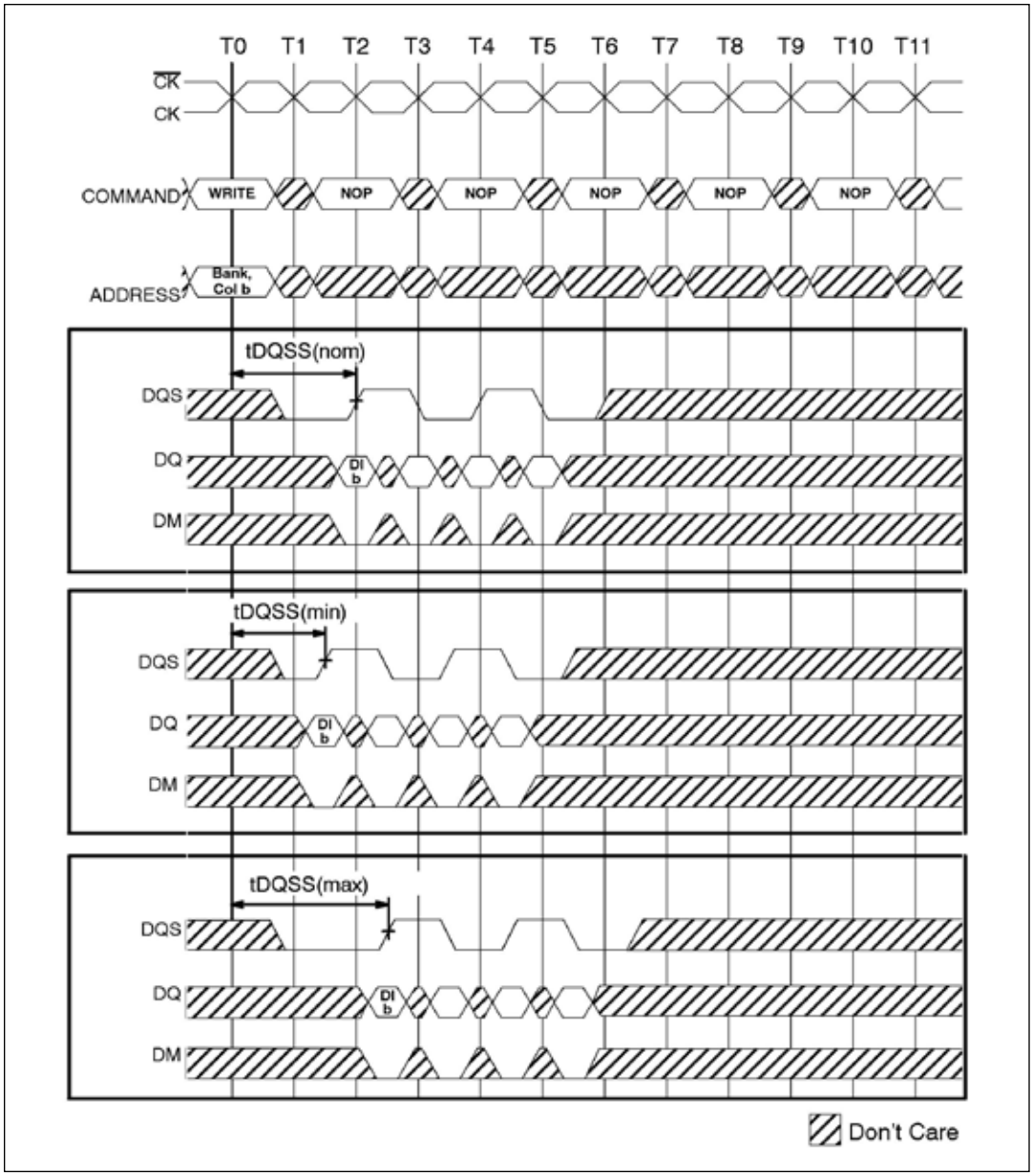
Data for any Write burst may be truncated by a subsequent READ command as shown in Figure Interrupting Write to Read. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

WRITE to PRECHARGE:

Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met. Data for any WRITE burst may be truncated by a subsequent PRECHARGE command.

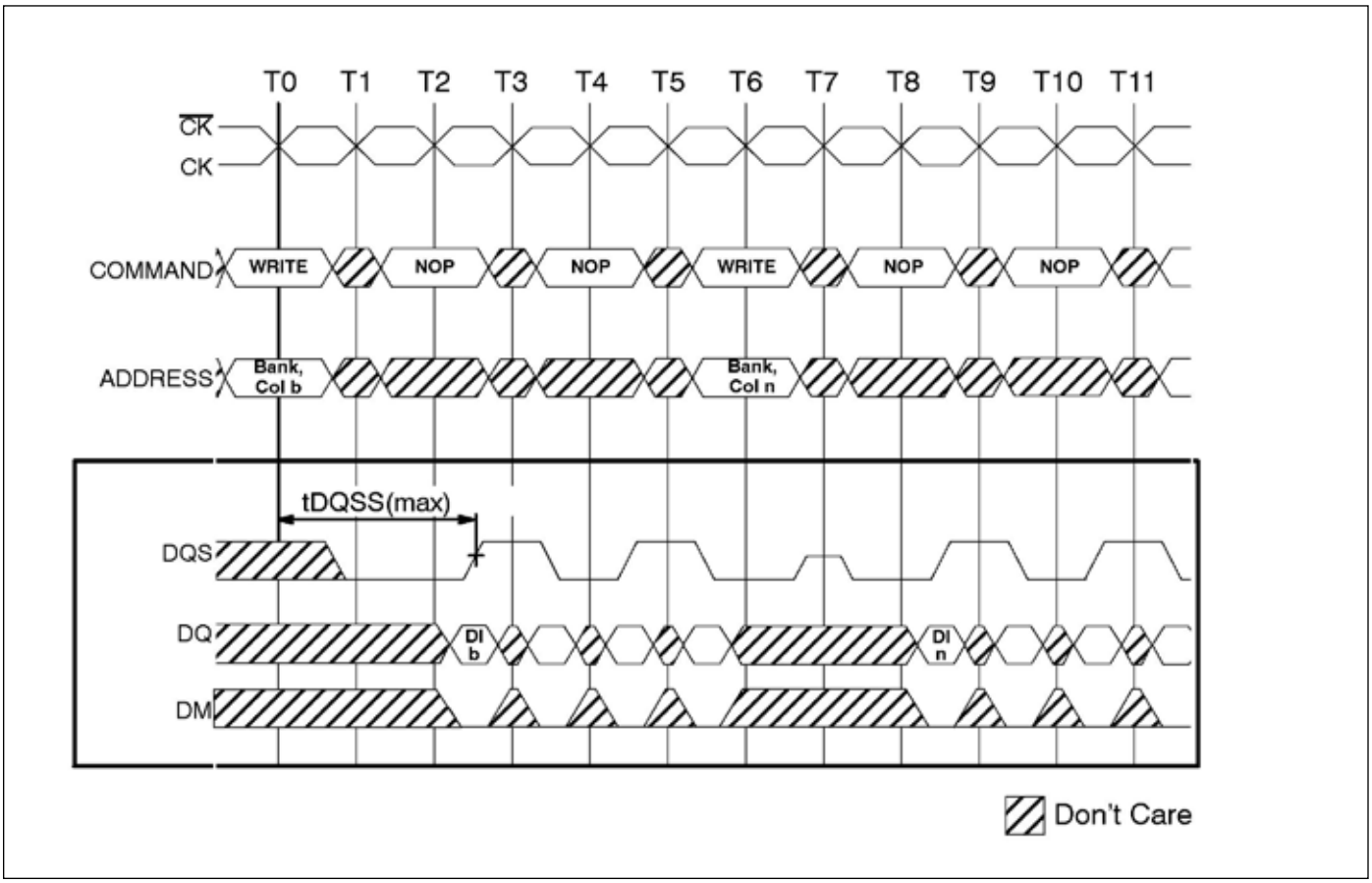
Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

Write Bursts



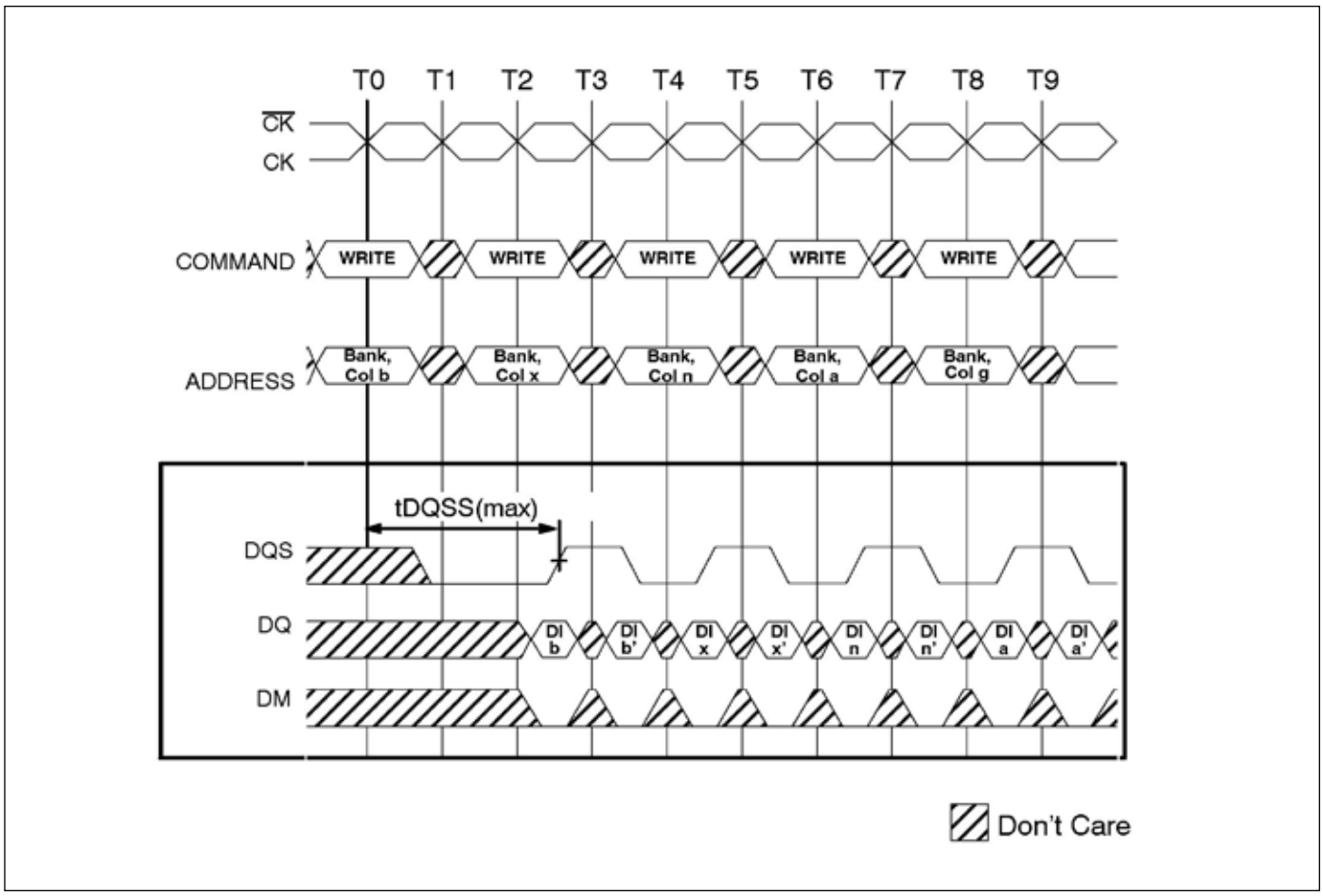
Notes:
DI b = Data In for column b
Three elements of data are applied in the programmed order following DI
A noninterrupted burst of 4 is shown
AP is low with the WRITE command (autoprecharge is disabled)
DM: DM0~DM3, DQ: DQ0~DQ31, DQS: DQS0~DQS3.

Non-Consecutive Write Bursts



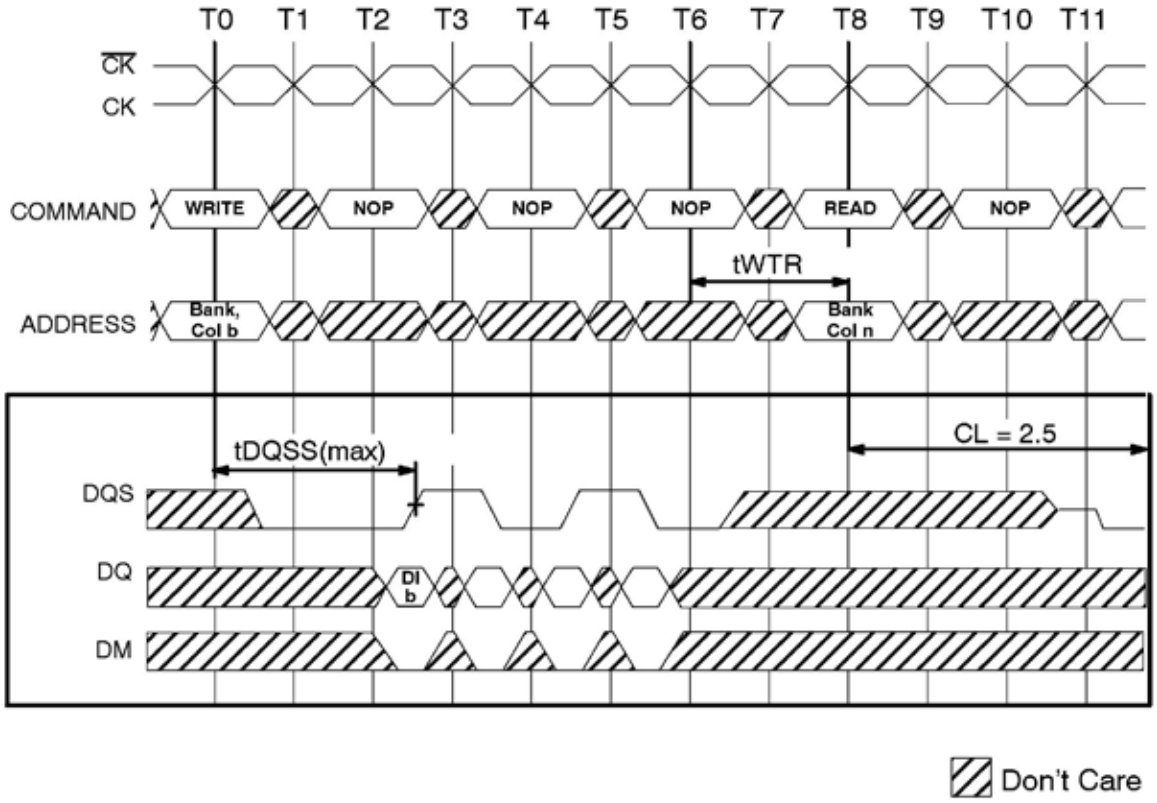
Notes:
DI b, etc. = Data In for column b, etc.
Three subsequent elements of Data In are applied in the programmed order following DI b
Three subsequent elements of Data In are applied in the programmed order following DI n
Noninterrupted bursts of 4 are shown
Each WRITE command may be to any bank and may be to the same or different devices

Random Write Cycles



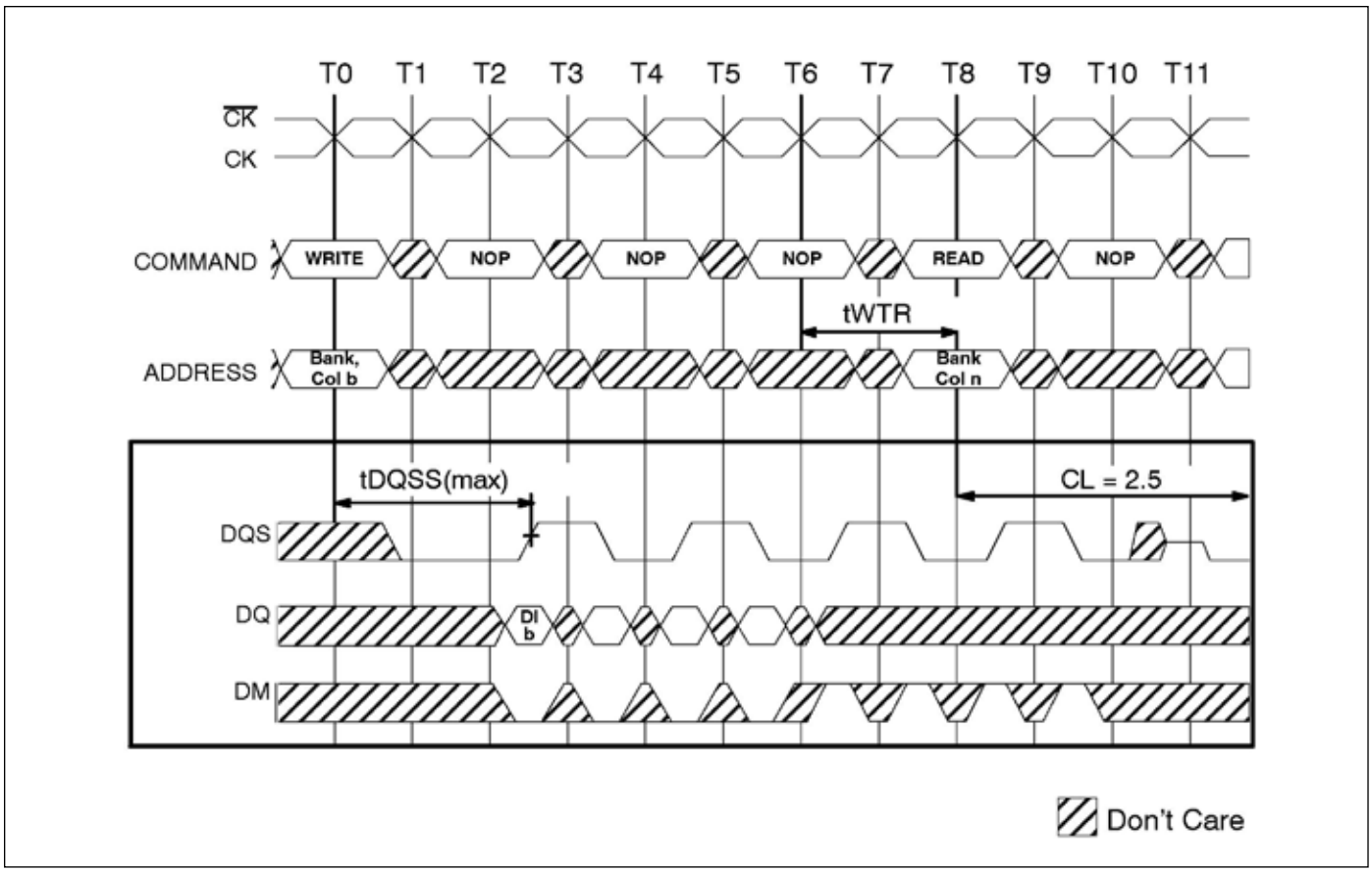
Notes:
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order.
Programmed Burst Length = 2, 4, or 8 in cases shown.
If burst of 4 or 8, the burst would be truncated.
Each WRITE command may be to any bank and may be to the same or different devices.

Non-Interrupting Write to Read



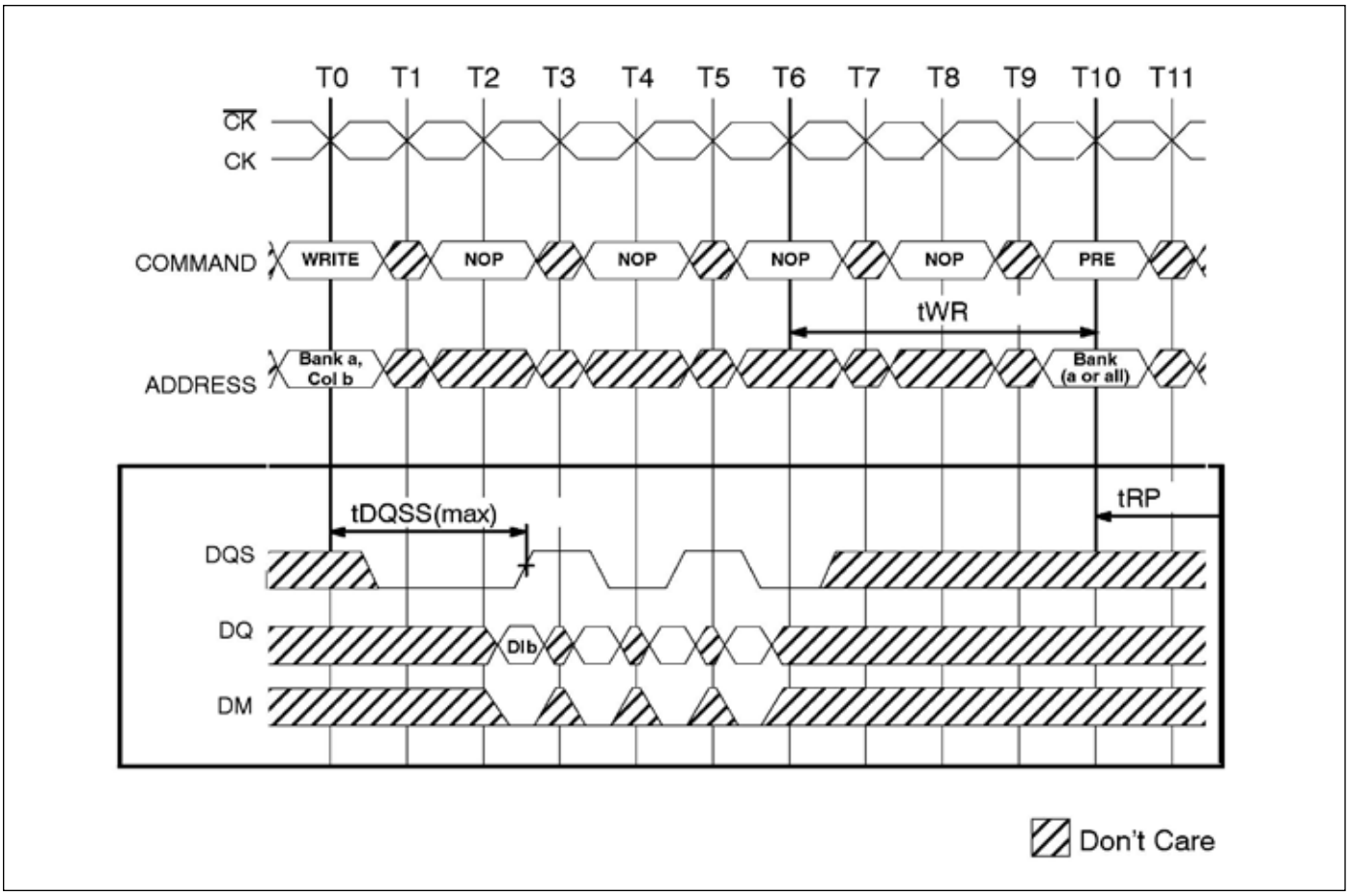
Notes:
DI b = Data In for column b
Three subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
tWTR is referenced from the first positive CK edge after the last Data In pair
AP is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank

Interrupting Write to Read



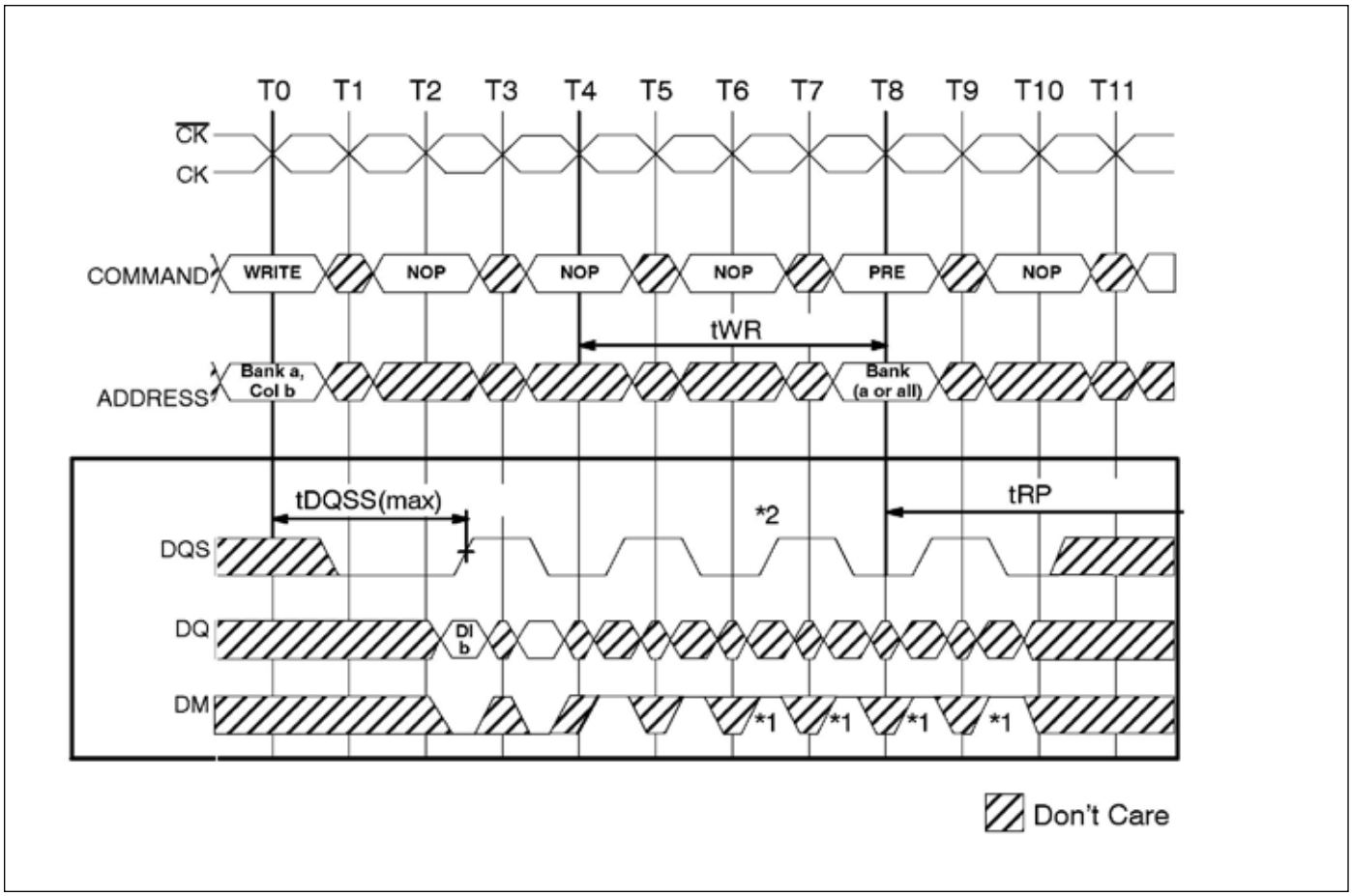
Notes:
DI b = Data In for column b
An interrupted burst of 8 is shown, 4 data elements are written
Three subsequent elements of Data In are applied in the programmed order following DI b
tWTR is referenced from the first positive CK edge after the last Data In pair
AP is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ and WRITE commands are to the same device but not necessarily to the same bank

Non-Interrupting Write to Precharge



Notes:
DI b = Data In for column b
Three subsequent elements of Data In are applied in the programmed order following DI b
A non-interrupted burst of 4 is shown
tWR is referenced from the first positive CK edge after the last Data In pair
AP is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Interrupting Write to Precharge



Notes:
DI b = Data In for column b
An interrupted burst of 4 or 8 is shown, 2 data elements are written
tWR is referenced from the first positive CK edge after the last desired Data In pair
AP is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued.

Input A8 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”.

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A8 = High, to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

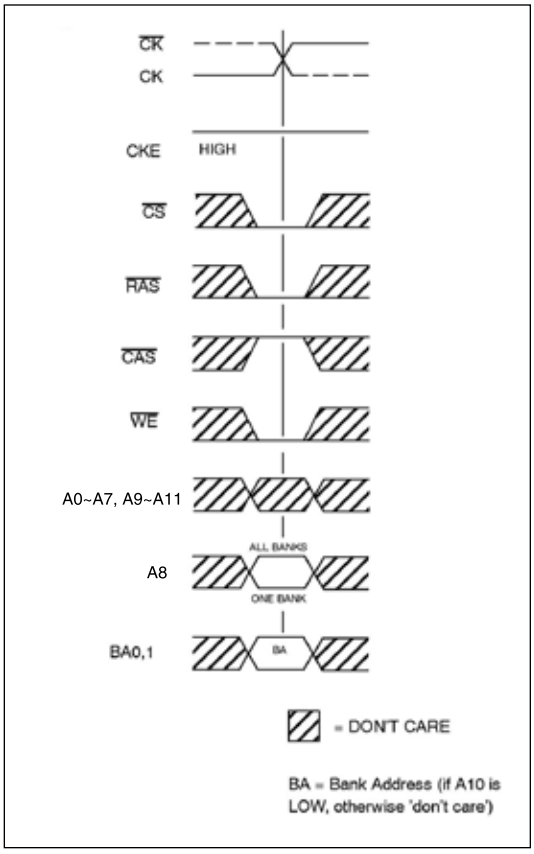
Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharging time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this specification.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with Auto Precharge disabled).

The most recently registered READ command prior to the BURST TERMINATE command will be truncated. Note that the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

PRECHARGE command



REFRESH REQUIREMENTS

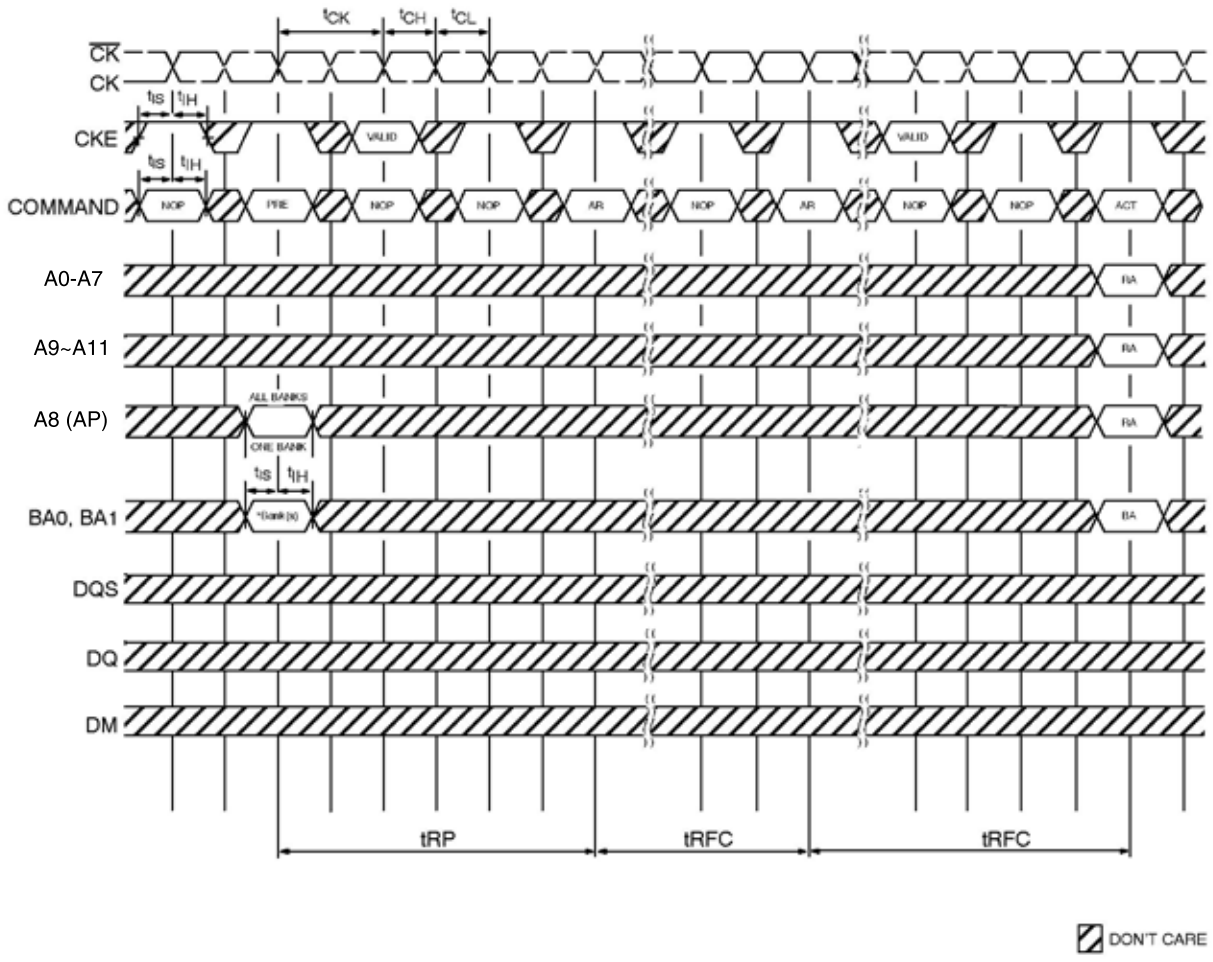
DDR SDRAM devices require a refresh of all rows in any 32ms. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 32ms interval defines the average refresh interval (tREFI), which is a guideline to controllers for distributed refresh timing.

AUTO REFRESH

AUTO REFRESH command is used during normal operation of the DDR SDRAM. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. The DDR SDRAM requires AUTO REFRESH commands at an average periodic interval of tREFI.

AUTO REFRESH command



Notes:
* = ”Don’t Care”, if AP is HIGH at this point; AP must be HIGH if more than one bank is active (i.e., must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC.
DM, DQ and DQS signals are all ”Don’t Care”/High--Z for operations shown

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR SDRAM retains data without external clocking. The DDR SDRAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is LOW. Input signals except CKE are “Don’t Care” during Self Refresh. The user may halt the external clock one clock after the SELF REFRESH command is registered.

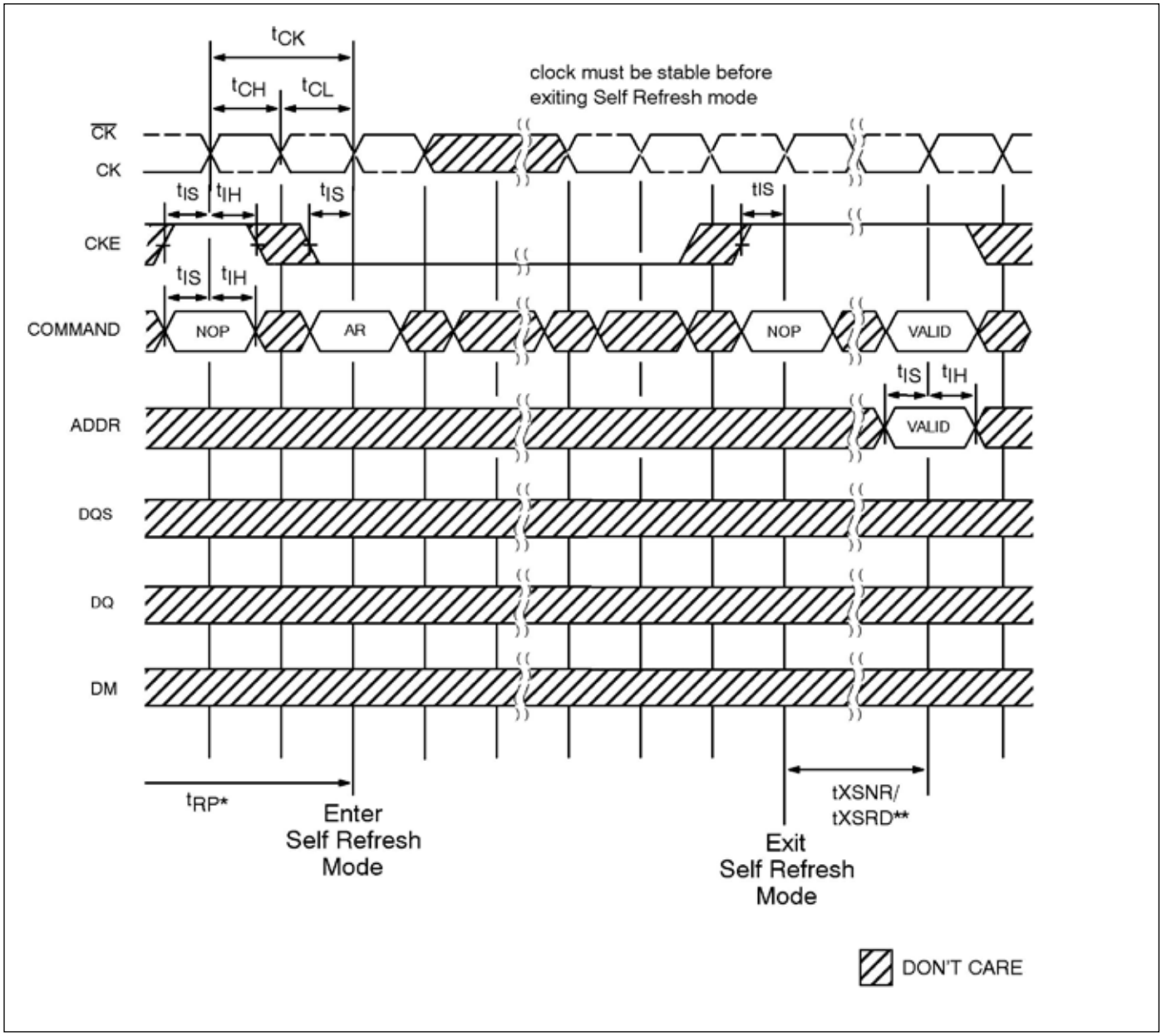
Once the command is registered, CKE must be held low to keep the device in Self Refresh mode.

The clock is internally disabled during Self Refresh operation to save power. The minimum time that the device must remain in Self Refresh mode is tRFC.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back High. Once Self Refresh Exit is registered, a delay of at least tXS must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh an extra AUTO REFRESH command is recommended.

SELF REFRESH command



Notes:
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non--READ command can be applied, and tXSRD (200 cycles of CK) is required before a READ command can be applied.

POWER-DOWN

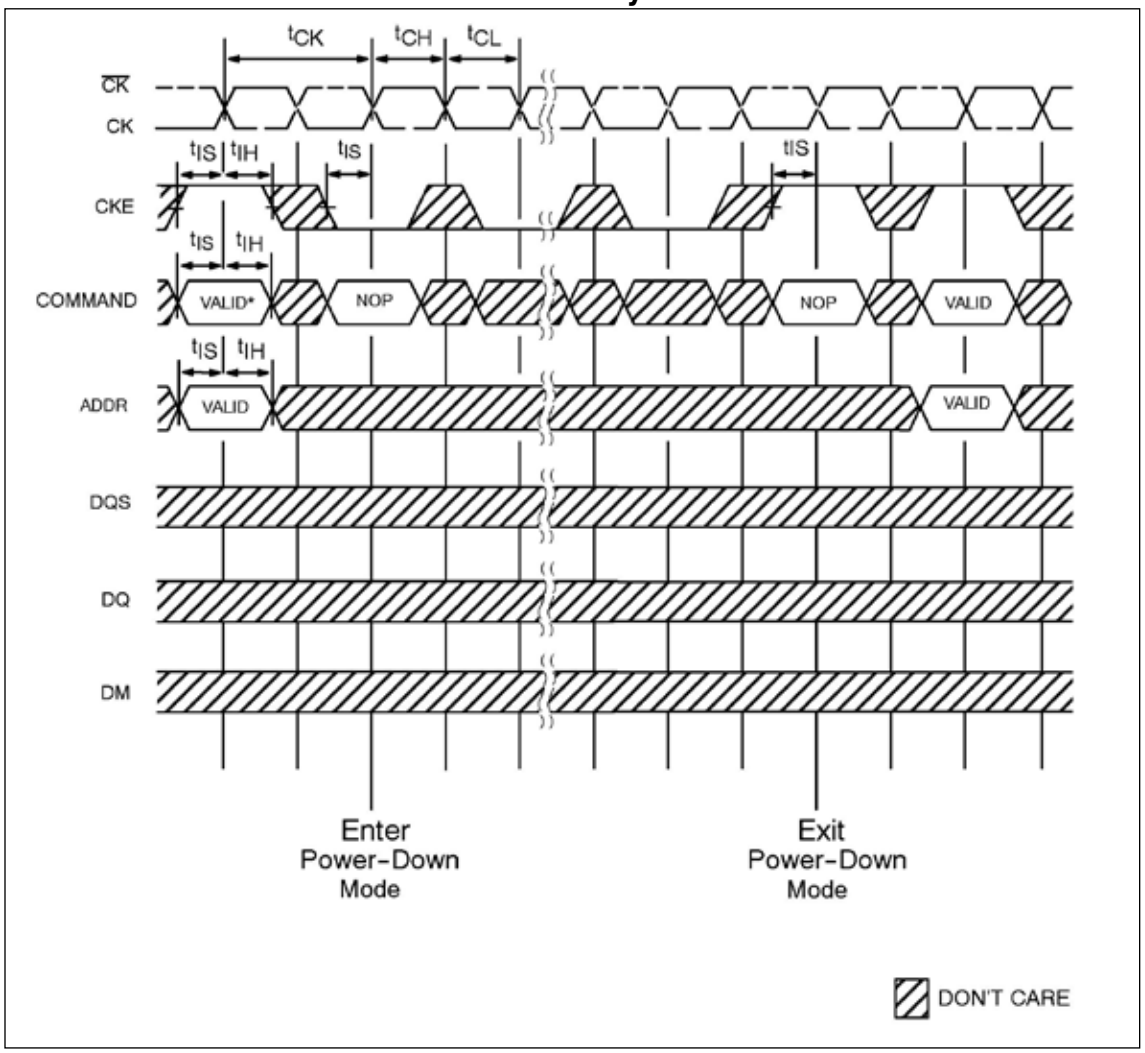
Power-down is entered when CKE is registered Low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

For maximum power savings, the user has the option of disabling the DLL prior to entering power--down. In that case, the DLL must be enabled after exiting power--down, and 200 clock cycles must occur before a READ command can be issued. However, power--down duration is limited by the refresh requirements of the device, so in most applications, the self--refresh mode is preferred over the DLL--disabled power--down mode.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. In power-down mode, CKE LOW must be maintained, and all other input signals are “Don’t Care”. The minimum power-down duration is specified by tCKE. However, power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered High (along with a NOP or DESELECT command). A valid command may be applied tXP after exit from power-down.

Power-Down Entry and Exit



Notes:

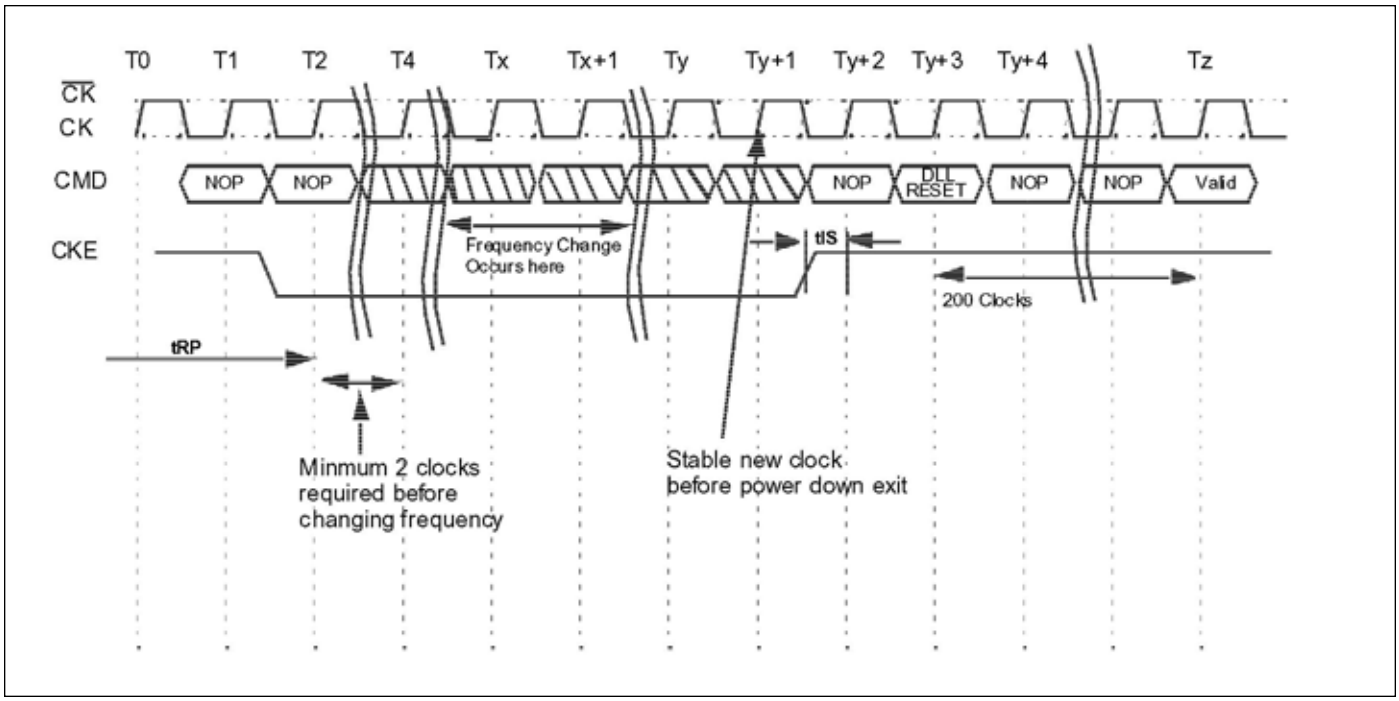
No column accesses are allowed to be in progress at the time Power--Down is entered

* = If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power--Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power--Down mode shown is Active Power Down.

Input Clock Frequency Change during Precharge Power Down

The DDR SDRAM input clock frequency can be changed under following condition: DDR SDRAM must be in precharged power down mode with CKE at logic LOW level. After a minimum of 2 clocks after CKE goes LOW, the clock frequency may change to any frequency between minimum and maximum operating frequency specified for the particular speed grade. During an input clock frequency change, CKE must be held LOW. Once the input clock frequency is changed, a stable clock must be provided to DRAM before precharge power down mode may be exited. The DLL must be RESET via EMRS after precharge power down exit. An additional MRS command may need to be issued to appropriately set CL etc.. After the DLL relock time, the DRAM is ready to operate with new clock frequency.

Clock Frequency Change in Precharge Power Down Mode



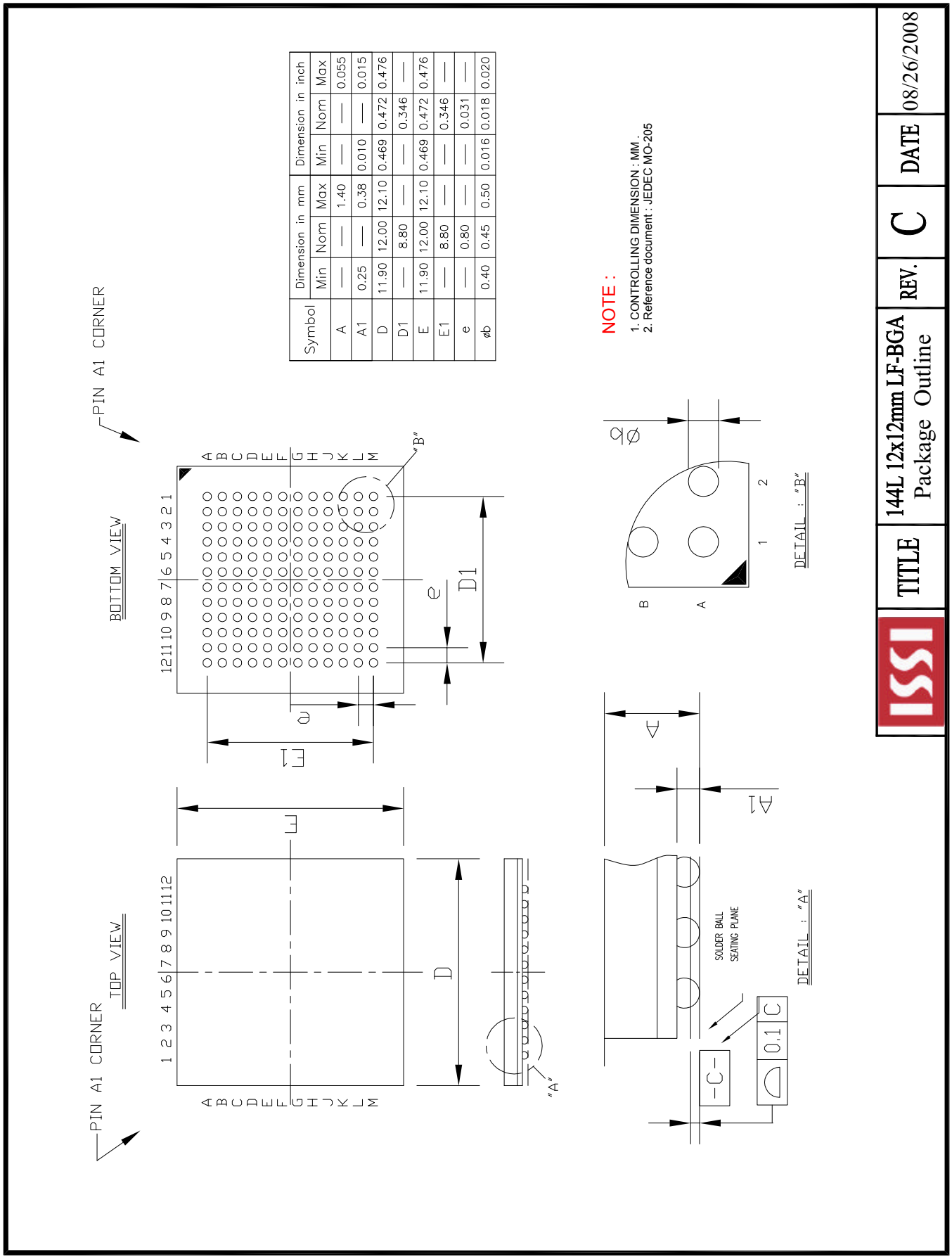
ORDERING INFORMATION - VDD = 2.5V

Commercial Range: 0°C to +70°C

Frequency	Speed (ns)	Order Part No.	Package
250 MHz	4	IS43R32400D-4BL	144-ball FBGA, Lead-free
200 MHz	5	IS43R32400D-5BL	144-ball FBGA, Lead-free
166 MHz	6	IS43R32400D-6BL	144-ball FBGA, Lead-free

Industrial Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
250 MHz	4	IS43R32400D-4BLI	144-ball FBGA, Lead-free
200 MHz	5	IS43R32400D-5BLI	144-ball FBGA, Lead-free
166 MHz	6	IS43R32400D-6BLI	144-ball FBGA, Lead-free



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.40	—	—	0.055
A1	0.25	—	0.38	0.010	—	0.015
D	11.90	12.00	12.10	0.469	0.472	0.476
D1	—	8.80	—	—	0.346	—
E	11.90	12.00	12.10	0.469	0.472	0.476
E1	—	8.80	—	—	0.346	—
e	—	0.80	—	—	0.031	—
øb	0.40	0.45	0.50	0.016	0.018	0.020

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