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by PZTA63T1/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PZTA63T1,T3
PZTA64T1,T3

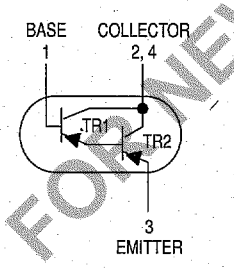
Advance Information

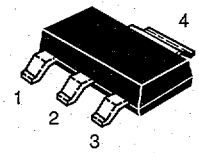
PNP Small-Signal Darlington Transistors

This family of PNP small-signal darlington transistors is designed for use in preamplifiers input applications or wherever it is necessary to have a high input impedance. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

- NPN Complements are PZTA13 and PZTA14
- High f_T; 125 MHz Minimum
- The SOT-223 Package can be Soldered Using Wave or Reflow.
- SOT-223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Available in 12 mm Tape and Reel
  T1 Configuration — 7 Inch Reel; 1000 Units
  T3 Configuration — 13 Inch Reel; 4000 Units

SOT-223 PACKAGE
PNP SILICON
TRANSISTORS
SURFACE MOUNT





CASE 318E-04, STYLE 1
TO-261AA

MAXIMUM RATINGS			
Rating	**Symbol**	**Value**	**Unit**
Collector-Emitter Voltage	V_{CES}	−30	Vdc
Collector-Base Voltage	V_{CBO}	−30	Vdc
Emitter-Base Voltage	V_{EBO}	−10	Vdc
Total Power Dissipation up to T_A = 25°C*	P_{tot}*	1.5	Watts
Collector Current	I_C	−500	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	150	°C
DEVICE MARKING			
PZTA63 P2U PZTA64 P2V			
THERMAL CHARACTERISTICS			
Thermal Resistance from Junction to Ambient*	$R_{\theta JA}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	**Symbol**	**Min**	**Max**	**Unit**
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = −100 μAdc, V_{BE} = 0)	$V_{(BR)CES}$	−30	—	Vdc
Collector-Base Breakdown Voltage (I_C = −100 nA, I_E = 0)	$V_{(BR)CBO}$	−30	—	Vdc
Emitter-Base Breakdown Voltage (I_E = −100 nA, I_C = 0)	$V_{(BR)EBO}$	−10	—	Vdc

* Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 in^2.

(continued)

Thermal Clad is a registered trademark of the Bergquist Company

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)					
Characteristic		**Symbol**	**Min**	**Max**	**Unit**
OFF CHARACTERISTICS — continued					
Emitter-Base Cutoff Current (V_{BE} = – 10 Vdc, I_C = 0)		I_{EBO}	—	– 0.1	µAdc
Collector-Base Cutoff Current (V_{CB} = – 30 Vdc, I_E = 0)		I_{CBO}	—	– 0.1	µAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = – 10 mAdc, V_{CE} = – 5.0 Vdc)	PZTA63		5,000	—	
	PZTA64		10,000	—	
(I_C = – 100 mAdc, V_{CE} = – 5.0 Vdc)	PZTA63		10,000	—	
	PZTA64		20,000	—	
Collector-Emitter Saturation Voltage (I_C = – 100 mAdc, I_B = – 0.1 mAdc)		$V_{CE(sat)}$	—	– 1.5	Vdc
Base-Emitter On-Voltage (V_{CE} = – 5.0 Vdc, I_C = – 100 mAdc)		$V_{BE(on)}$	—	– 2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = – 10 mAdc, V_{CE} = – 5.0 Vdc, f = 100 MHz)		f_T	125	—	MHz

SOT-223 POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the collector pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows.

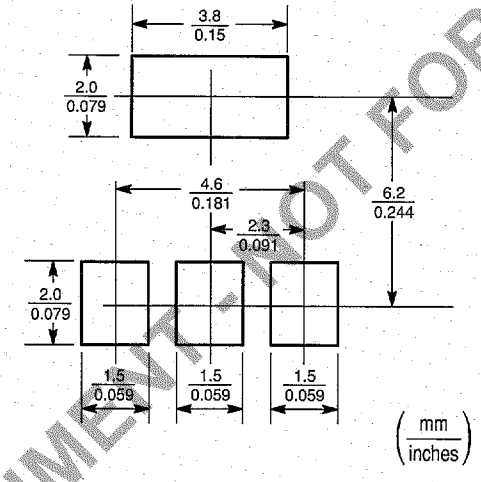
$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 1.5 watts.

$$P_D = \frac{150°C - 25°C}{83.3°C/W} = 1.5 \text{ watts}$$

The 83.3°C/W assumes the recommended collector pad area of 965 mil^2 on a glass epoxy printed circuit board to achieve a power dissipation of 1.5 watts. If space is at a premium, a more realistic approach is to use the device at a P_D of 800 milliwatts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad. Using a board material such as Thermal Clad™, an aluminum core board, the power dissipation can be doubled using the same footprint.

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS



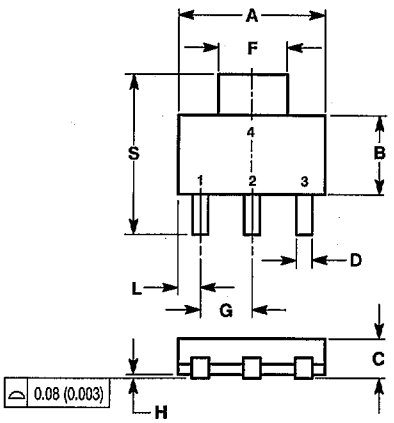
MOUNTING PRECAUTIONS

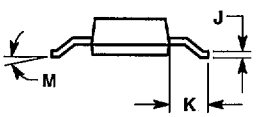
The melting temperature of solder is higher than the rated temperature of the device and the entire device is heated to a high temperature; therefore failure to complete soldering within a short time at a low temperature can adversely affect the following characteristics: heat resistance and humidity resistance which could result in device failure. Therefore the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device
- The delta temperature between the preheat and soldering should be 100°C or less*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference in temperatures of the case and the leads shall be Δ10°C or less.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for three minutes or more. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

*Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

OUTLINE DIMENSIONS





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.30	6.70	0.249	0.263
B	3.30	3.70	0.130	0.145
C	1.50	1.75	0.060	0.068
D	0.60	0.89	0.024	0.035
F	2.90	3.20	0.115	0.126
G	2.20	2.40	0.087	0.094
H	0.020	0.100	0.0008	0.0040
J	0.24	0.35	0.009	0.014
K	1.50	2.00	0.060	0.078
L	0.85	1.05	0.033	0.041
M	0°	10°	0°	10°
S	6.70	7.30	0.264	0.287

CASE 318E-04
TO-261AA

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USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
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