PRO-LINX™ GS7005
Complete Serial Digital Video Receiver

DATA SHEET

GS7005

FEATURES

- **SMPTE 259M-C compliant**
- **fully integrated 270 Mb/s SDI receiver**
- **integrated cable equalization (100m Belden 8281 typical)**
- **low power consumption (750mW typical)**
- **operates from 0°C to 85°C**
- **small footprint with minimal external components**
- **Lock and Carrier Detect output indications**
- **H timing signal output**
- **SMPTE descrambler and NRZI decoder may be disabled for DVB - ASI applications**
- **ease of design use and adjustment free operation**

APPLICATIONS

Limited space, low power SMPTE 259M-C or generic 270Mb/s serial to parallel interfaces; DVB-ASI 270Mb/s receive interface; broadcast quality uncompressed video interface for industrial and professional video equipment such as video editing workstations.

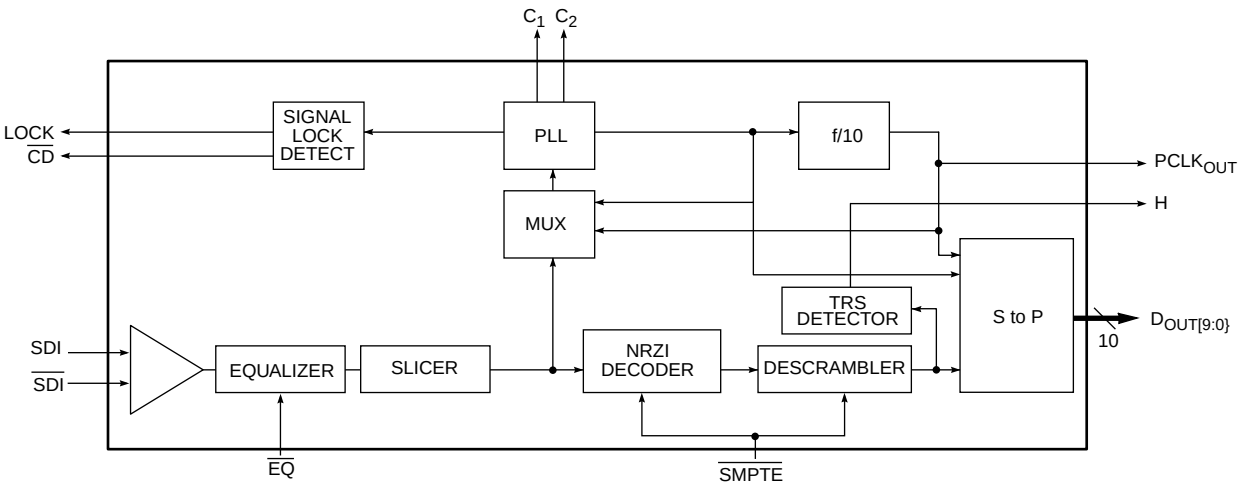
DESCRIPTION

The GS7005 is a BiCMOS integrated circuit capable of operating as a complete 270Mb/s Serial Digital Video receiver. The GS7005 provides a complete serial digital video receive solution while consuming only 750mW.

The serial data input accepts SMPTE 259M-C compliant signals. An on-chip by-passable equalizer typically provides 100m of co-axial cable equalization. The clock recovery is performed on chip with minimal external components. The incoming serial data is decoded using an NRZI decoder and SMPTE descrambler to provide SMPTE 125M compliant 27Mb/s parallel data outputs and clock.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS7005 - CQT	52 pin MQFP	0°C to 85°C
GS7005 - CTT	52 pin MQFP Tape	0°C to 85°C



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	5.5V
Input Voltage Range (any input)	GND < V_{IN} < V_{CC}
DC Input Current (any one input)	10mA
Power Dissipation (V_{CC} = 5.25V)	1W
Maximum Die Temperature	125°C
Operating Temperature Range	0°C <= T_A <= 85°C
Storage Temperature Range	-65°C <= T_S <= 150°C
Lead Temperature (soldering 10s)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C, unless otherwise specified.
Serial data rate = 270Mb/s, Parallel Data Rate = 27Mb/s, f_{PCLK} = 27MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Positive Supply Voltage	V_{CC}	Operating range	4.75	5.00	5.25	V		6
Power Consumption	P	V_{CC} = 5.25V	-	750	-	mW		5
Supply Current	I_{CC}	V_{CC} = 5.25V	-	140	-	mA		1
Logic Inputs - Low	V_{IL}	V_{CC} = 5.25V	-	-	0.8	V		6
Logic Inputs - High	V_{IH}	V_{CC} = 4.75V	2	-	-	V		6
Logic Outputs - Low	V_{OL}	V_{CC} = 5.25V	-	-	0.5	V		1
Logic Outputs - High	V_{OH}	V_{CC} = 4.75V	2.4	-	-	V		1

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C, unless otherwise specified in 'conditions'
Serial data rate = 270Mb/s, Parallel Data Rate = 27Mb/s, f_{PCLK} = 27MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Parallel Data - Rise/Fall Time	t_{R/F_DOUT}	C_L = 20pF	1.0	-	6.0	ns	1	4, 7
PCLK Rising Edge to $D_{OUT(N)}$ Centre	t_D		-	-	±5	ns	2, 3	4, 7
PCLK Rise/Fall Time	$t_{R/F\_PCLKOUT}$	C_L = 20pF	0.5	-	3.0	ns	1	4, 7
Input Return Loss	$LOSS_{IN}$	75Ω match 5MHz to 270MHz	-	17	-	dB		7
Asynchronous Lock Time	t_{LOCK_ASYNC}		-	-	250	ms	4	1
Synchronous Lock Time	t_{LOCK_SYNC}		-	-	10	µs	5	1
Input Jitter Tolerance	t_{J_SI}	Pathological Input	-	0.35	-	U.I.	6	7
Output PCLK Jitter	$t_{J\_PCLKOUT}$	Pseudorandom Input	-	800	-	ps p-p		1
		Pathological Input	-	1000	-	ps p-p	6	7
Error Free Cable Length		Pseudorandom Input	-	100	-	m		7
		Pathological Input	75	100	-	m	6, 7	1

NOTES

1. Rise/Fall time is defined as the time for the signal to rise from 20% to 80% of the specified p-p value, or to fall from 80% to 20% of the specified value.
2. Refer also to Figure 10.
3. This is the time difference between the rising edge of $PCLK_{OUT}$ and the centre of the bit period.
4. This is the time delay between a valid serial TRS signal on the input to the moment valid data appears on the parallel outputs.
5. This is the time for the PLL to re-lock when video streams are switched during the vertical blanking interval in accordance with SMPTE RP168-1993. The two streams may be 180° out of phase with respect to one another, but pixel aligned.
6. This pathological pattern is defined in SMPTE RP178-1996, paragraphs 4.1 and 4.3.
7. "Error free" is defined as no single bit errors over a period of 10 minutes, using Belden 8281 Cable and 75Ω connections. The MIN value is fully tested and the TYP value is based on using the EB7005 Evaluation Board.

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

TEST SETUP

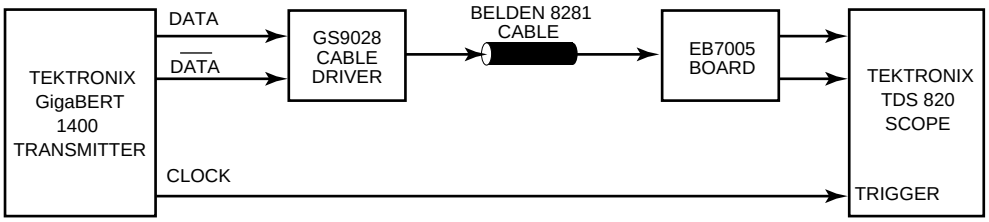


Fig. 1a Test Setup for Jitter Measurements

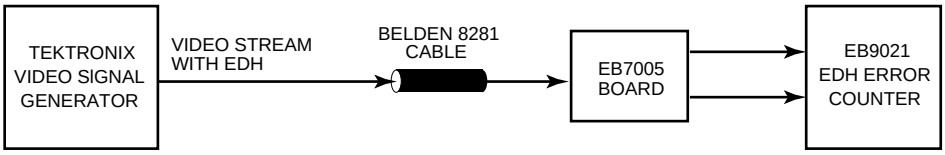


Fig. 1b Test Setup for Error-Free Cable Length

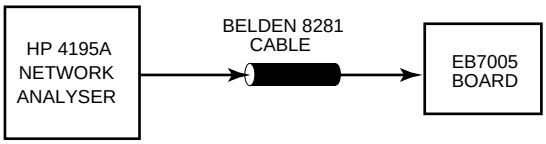
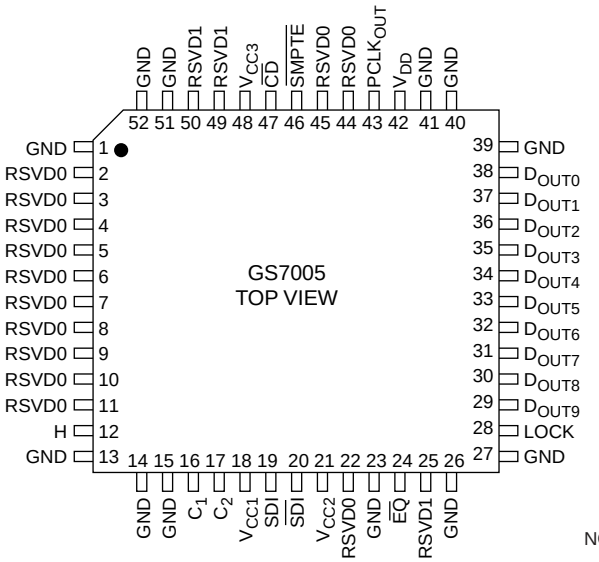


Fig. 1c Test Setup for Return Loss Measurements

PIN CONNECTIONS



NOTE: RSVD = Reserved

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 13, 14, 26, 27, 39, 40, 52	GND	-	Connect to Ground.
2-11, 22, 44, 45	RSVD0	-	Connect to Ground.
12	H	O	H Indication. HIGH after EAV ID and LOW after SAV ID.
15	GND	-	Ground for analog blocks of the device.
16, 17	C_1, C_2	-	External 100nF loop filter capacitor connection.
18	V_{CC1}	-	Power supply for analog blocks of the device.
19, 20	SDI, $\overline{SDI}$	I	Differential Serial Data Input
21	V_{CC2}	-	Power supply for PECL blocks of the device.
23	GND	-	Ground for PECL blocks of the device.
24	$\overline{EQ}$	I	Equalizer Control; LOW = EQ on, HIGH = EQ bypassed.
25, 49, 50	RSVD1	-	Connect to $V_{CC.}$
28	LOCK	O	Signal Lock Indication Output. Goes HIGH approximately 38µs after valid parallel data occurs.
29-38	$D_{OUT[9:0]}$	O	27Mb/s Parallel Data Outputs.
41	GND	-	Ground for CMOS blocks of the device.
42	V_{DD}	-	Power supply for CMOS blocks of the device.
43	$PCLK_{OUT}$	O	27MHz Clock Output.
46	$\overline{SMPTE}$	I	NRZI decoding and descrambling control. LOW = NRZI and SMPTE mode on. HIGH = NRZI and SMPTE mode disabled.
47	$\overline{CD}$	O	Carrier Detect. Active LOW. Goes LOW when carrier is detected and high when carrier is lost.
48	V_{CC3}	-	Power supply for Analog and PECL blocks of the device.
51	GND	-	Ground for analog and PECL blocks of the device.

INPUT / OUTPUT CIRCUITS

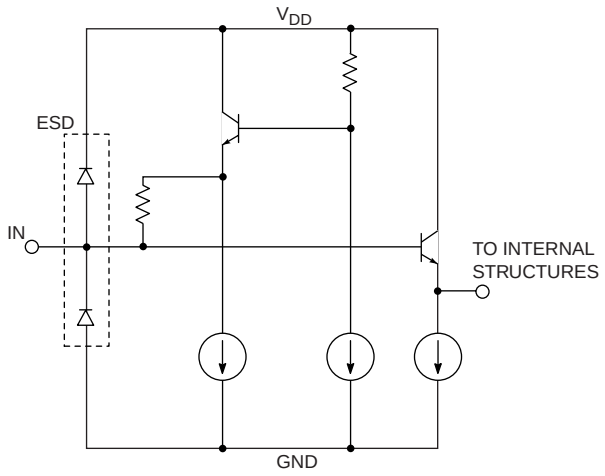


Fig. 2 SDI, $\overline{SDI}$

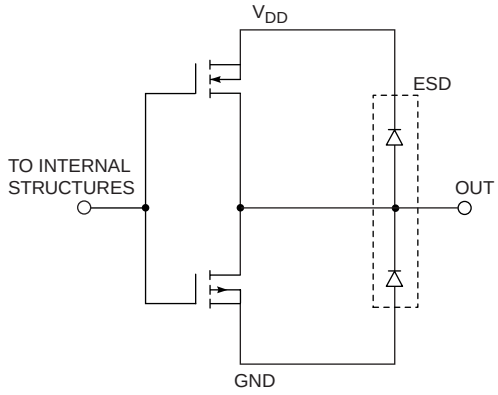


Fig. 3 $D_{OUT[9:0]}$, H, LOCK, $\overline{CD}$, $PCLK_{OUT}$

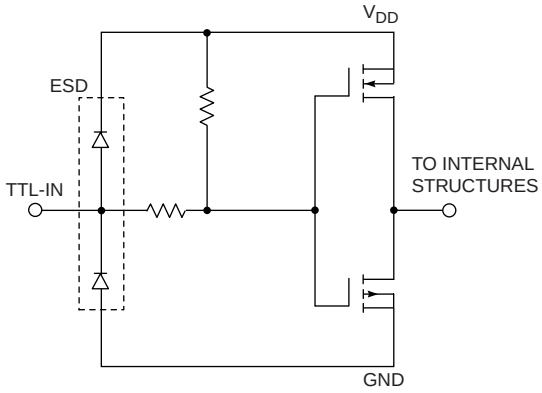


Fig. 4 $\overline{EQ}$, $\overline{SMPTE}$

TYPICAL PERFORMANCE CURVES (V_{CC} = 5V, T_A = 25°C unless otherwise shown)

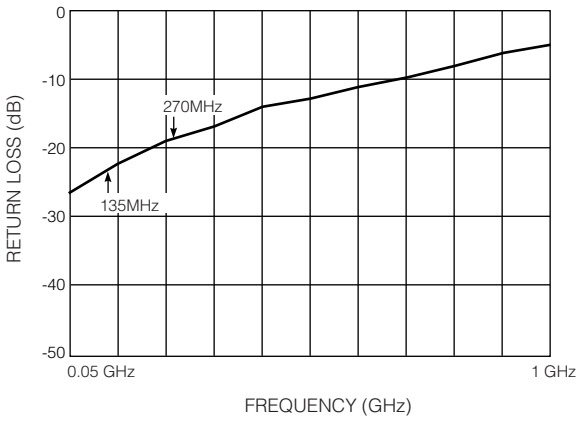


Fig. 5 Input Return Loss

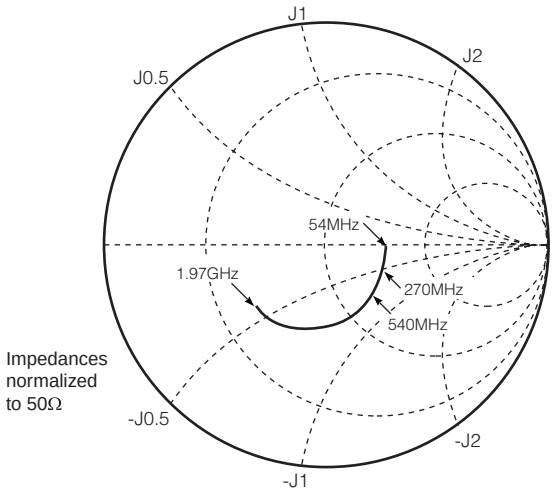


Fig. 7 Input Impedance

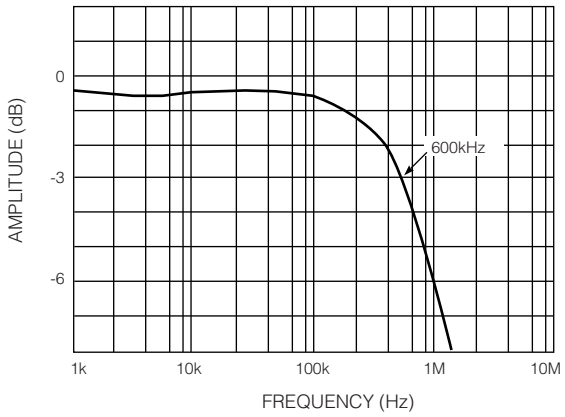


Fig. 6 Loop Bandwidth

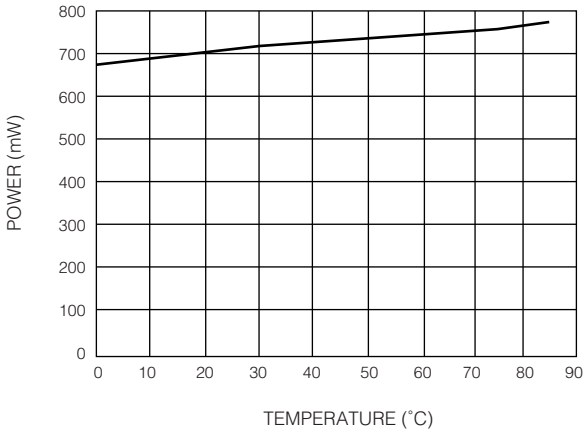


Fig. 8 Power vs. Temperature

RECEIVER OPERATION

$\overline{EQ}$	$\overline{SMPTE}$	GS7005 Operating mode
0	0	SMPTE 259M Receiver (Equalizer ON, SMPTE / NRZI Descrambler enabled).
1	0	SMPTE 259M Receiver with equalizer bypassed.
0	1	Receiver function with equalizer enabled and NRZI and SMPTE Descrambler disabled.
1	1	Receiver function with equalizer bypassed and NRZI and SMPTE Descrambler disabled.

The output of the LOCK pin is logic high approximately 38µs after the receiver has successfully locked to the input serial bit stream. The output H is set low after the SAV ID and is set high after the EAV ID when these sequences are identified in the incoming bit stream.

If external equalization is performed prior to this device, bypass the equalization control function ($\overline{EQ}$) by setting it HIGH.

To turn off the NRZI and SMPTE Descrambler function, set $\overline{SMPTE}$ HIGH. When operating in this mode, the output of $\overline{H}$ is either "1" or "0" (indeterminate).

DIAGRAMS

The figure below shows the timing relationship between the outputs of the GS7005.

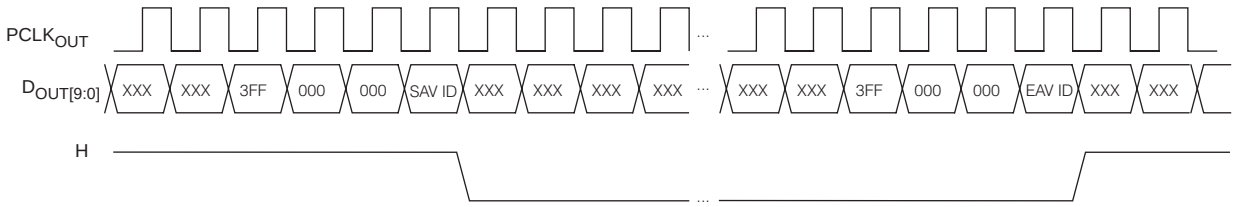


Fig. 9 Timing Diagram for Parallel Outputs, $PCLK_{OUT}$, and H

The figure below shows the relationship between the parallel clock and the parallel data outputs. The rising edge of the parallel clock is within ±5ns of the centre of the data.

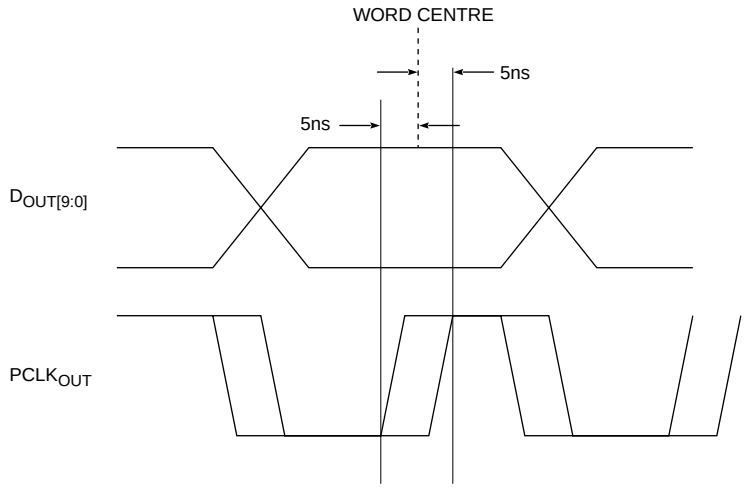


Fig. 10 Parallel Clock Alignment

DETAILED DESCRIPTION

The main functional blocks of the GS7005 are:

1. PECL input buffer
2. Fixed Gain Equalizer
3. Slicer
4. NRZI Decoder & SMPTE Descrambler
5. TRS Detector
6. Signal Lock Detect
7. Serial to Parallel Convertor

Refer to the Functional Block Diagram on the front page of this data sheet.

1. PECL INPUT BUFFER

This differential input buffer features a built-in load termination for the incoming SDI signal. The load is characterized as 75Ω over a wide frequency range and is made up of an internal fixed resistor and current source.

2. FIXED GAIN EQUALIZER

The Fixed Gain Equalizer stage is used to compensate the frequency dependent loss of the SDI signal through co-axial cable. The SDI signal is connected to the input pins (SDI/$\overline{\text{SDI}}$) either differentially or single ended. The input signal passes through a fixed gain equalizing stage whose frequency response closely matches the inverse cable loss characteristic. The equalizer typically provides 100m of coaxial cable equalization. The frequency response is optimized for maximum cable length. For short cable lengths (<10m), bypass the equalizing stage by setting the EQ control pin to a logic HIGH level. If an external equalizer is used, bypass the internal equalizer of the GS7005 to avoid over-equalization (*see Figure 12*).

3. POST EQUALIZATION SLICER

The Post Equalization Slicer stage slices the equalized signal, thereby eliminating any DC offset due to the AC coupling requirement of the SDI signal. Using a differential comparator, the received signal voltage is compared to a midway voltage, known as the baseline or the slicing level. The sliced signal is then applied to the NRZI/SMPTE Decoder/Descrambler and the PLL MUX.

4. NRZI DECODER & SMPTE DESCRAMBLER

To comply with the the ANSI/SMPTE 259M standard, use a scrambled, polarity free NRZI code. The polynomial generator for the scrambler is $G1(X) = X^9+X^4+1$. The NRZI code is produced by a second polynomial, $G2(X) = X+1$. The NRZI Decoder and SMPTE Descrambler blocks within the GS7005 regenerate the original NRZ unscrambled signal by applying the same algorithm to the received signal. For data structures that do not require de-scrambling and NRZI-NRZ conversion, bypass this block by setting the $\overline{\text{SMPTE}}$ pin to logic HIGH.

5. PLL, MUX and f/10

The PLL clock recovery circuitry provides an internal, synchronous 270MHz clock. The 27MHz parallel data clock is derived from the serial clock through a resettable frequency divider. To synchronize the parallel clock signal, set the frequency divider to the initial state at the same time the state machine has detected the Timing Reference Signal (TRS).

The PLL self-centres the VCO to approximately 29MHz when there are no input data transitions. This allows the PLL to lock when a valid signal within the lock range is applied. However, if the GS7005 detects a spurious input with random data transitions, the centering function of the VCO is inhibited. This causes the VCO control voltage to drift to a low clamp level resulting in a VCO frequency of 22MHz. To prevent this “latch-up” condition implementation of a high impedance (1MΩ) bleed resistor across the C1 and C2 (loop filter, pins 16 and 17) is recommended. Due to the large resistance value, the effect on IJT is negligible (*see Figure 11*).

6. TRS DETECTOR

The TRS Detector detects the TRS headers (EAV and SAV). It consists of a word-counter, bit-counter and control state-machine. The bit-counter is reset by either the decoded data or the output of the state-machine. In a normal case, the state-machine output is LOW. The reset of the bit counter is active LOW so that the bit-counter will be started when the data is HIGH. The detection of a valid TRS header is indicated by a level change of the H-signal pin.

7. SIGNAL LOCK DETECT

When there are no input data transitions, the $\overline{\text{CD}}$ pin goes to a HIGH logic level and forces the VCO to the centre frequency as described in section 5, *PLL, MUX, and f/10*. This output can be used to control an external transistor and LED. When there are input data transitions (valid or invalid), the $\overline{\text{CD}}$ pins goes to a LOW logic state.

The locking state of the PLL is indicated by the output LOCK signal being set to a logical HIGH level. This pin however, may have periodic transitions to a LOW logic state of 64µs maximum duration even though the device is properly locked. The parallel data signal integrity is not affected under these conditions. Therefore, the LOCK pin should not be used as a logic control signal if a steady level is required. The output voltage remains in a logic HIGH state for a sufficient period and can be used to drive visual indicators such as LEDs.

8. SERIAL TO PARALLEL CONVERTOR

The final function of the GS7005 is the serial-to-parallel conversion. The output signals of the receiver are ten data signals and one clock signal. The shift register is filled by the serial data and read out at a positive edge of the read-out signal. After parallel read out of the shift register, the parallel data is sampled with the negative edge of the 27MHz clock to achieve synchronization.

APPLICATION CIRCUITS

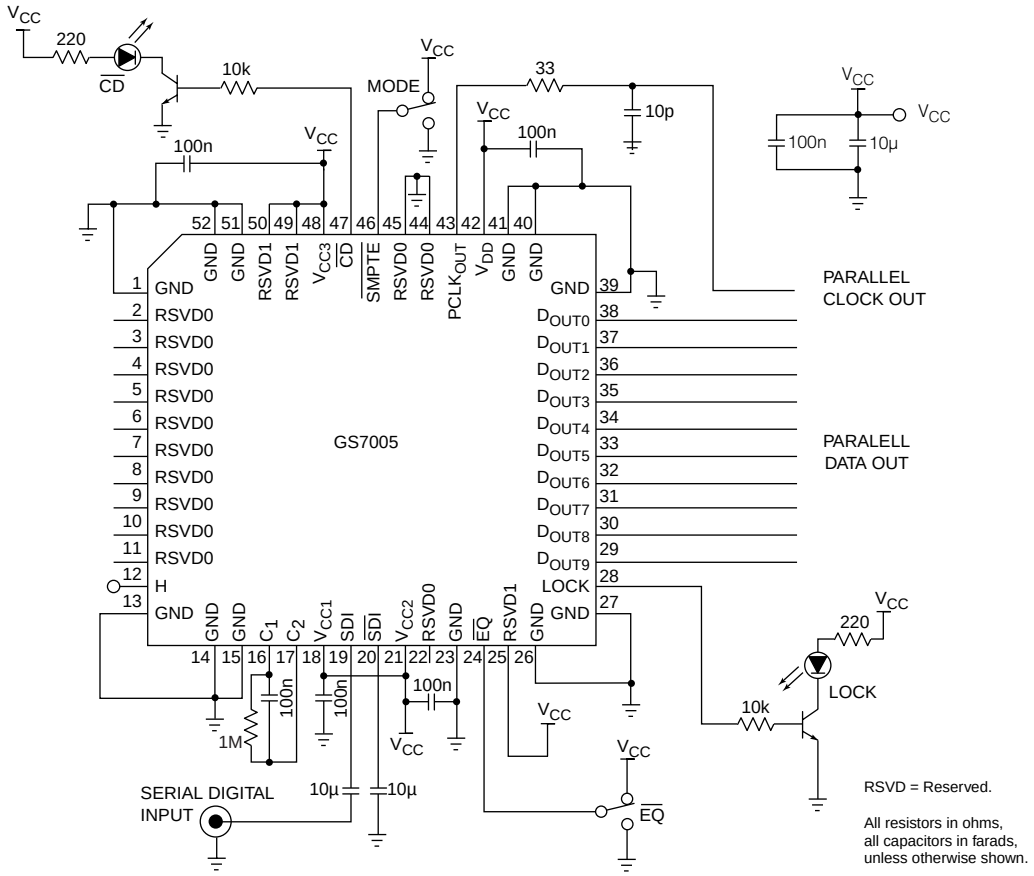


Fig. 11 Application Circuit - Unbalanced Serial Input Operation

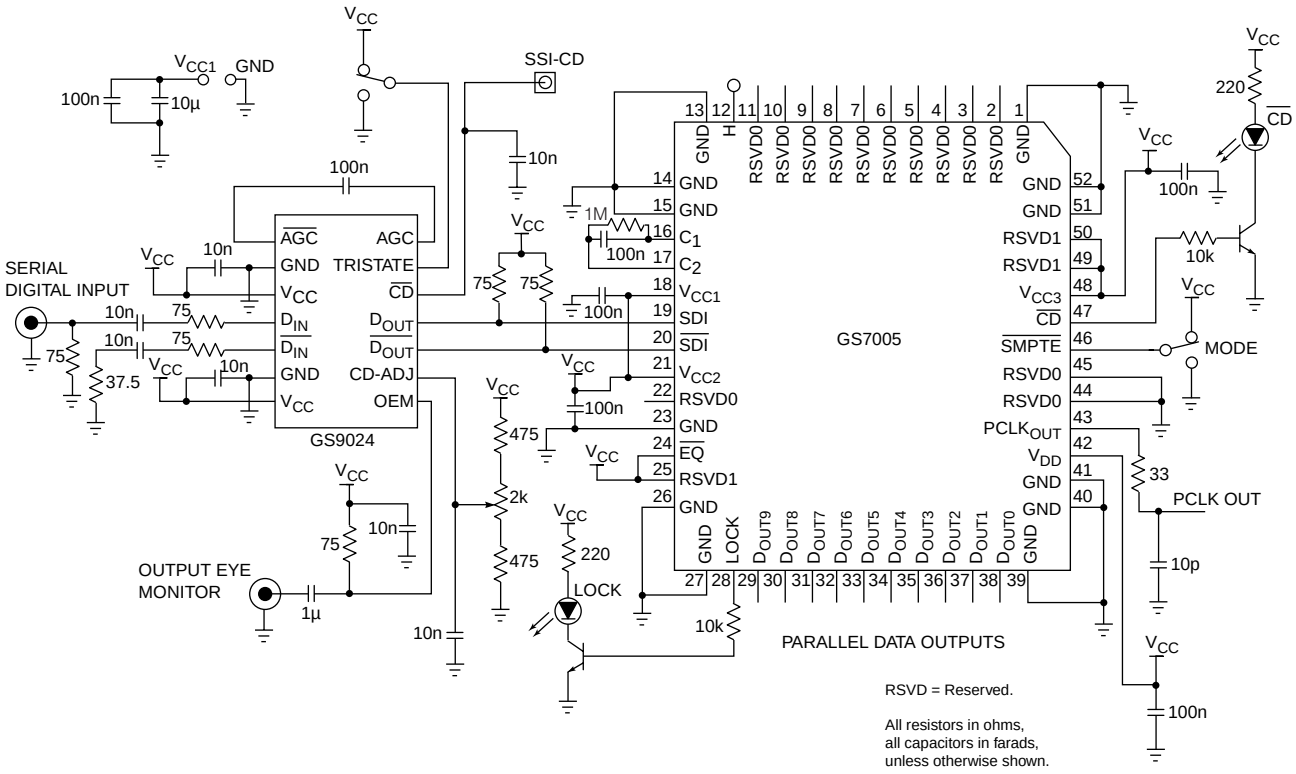
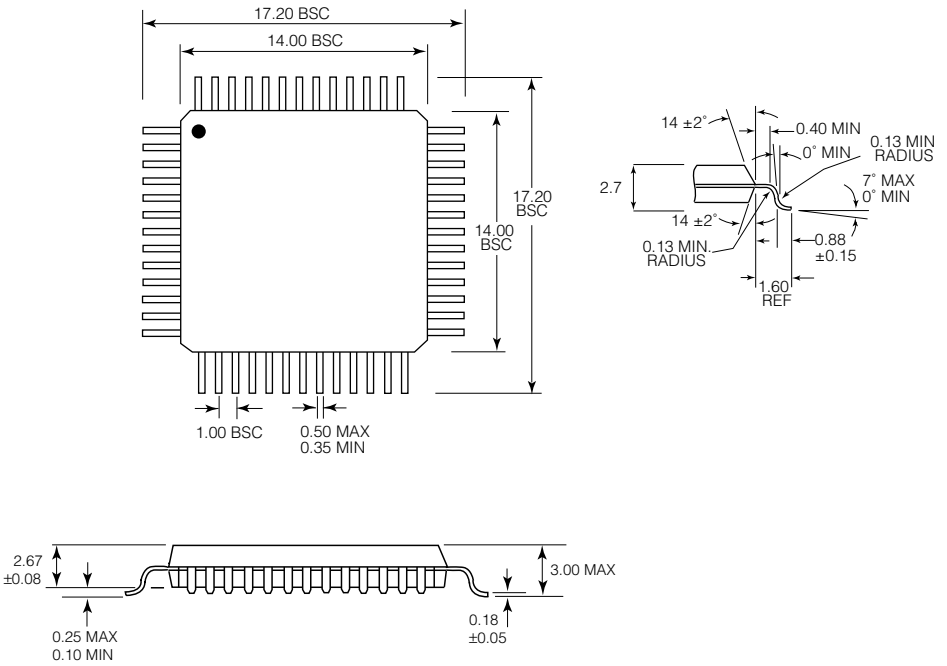


Fig. 12 Typical Application Circuit with External Equalizer

PACKAGE DIMENSIONS



All dimensions are in millimetres.
52 pin MQFP
BSC = Basic or nominal

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

Added label to package dimension drawing to show package thickness and included the third view; Added information to section 5, *PLL, MUX and f/10*; Removed Figures 5 and 6 - "Data to Follow"; Added resistor to Figures 11 and 12; Added to Package Dimensions legend.

For the latest product information, visit www.gennum.com.

GENNUM CORPORATION

MAILING ADDRESS:
P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

SHIPPING ADDRESS:
970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5

GENNUM JAPAN CORPORATION
C-101, Miyamae Village, 2-10-42 Miyamae, Suginami-ku
Tokyo 168-0081, Japan
Tel. +81 (03) 3334-7700 Fax. +81 (03) 3247-8839

GENNUM UK LIMITED
25 Long Garden Walk, Farnham, Surrey, England GU9 7HX
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523