Features

- **High-density, High-performance Electrically-erasable Complex Programmable Logic Device**
  - **44-pin, 32 I/O CPLD**
  - **7.5 ns Maximum Pin-to-pin Delay**
  - **Registered Operation Up to 125 MHz**
  - **Fully Connected Input and Feedback Logic Array**
  - **Backward Compatibility with ATF1500/L Software and Hardware**
- **Flexible Logic Macrocell**
  - **D/T/Latch Configurable Flip-flops**
  - **Global and Individual Register Control Signals**
  - **Global and Individual Output Enable**
  - **Programmable Output Slew Rate**
- **Advanced Power Management Features**
  - **Automatic 3 mA Standby (ATF1500AL)**
  - **Pin-controlled 10 mA Standby Mode**
  - **Programmable Pin-keeper Inputs and I/Os**
- **Available in Commercial and Industrial Temperature Ranges**
- **Available in 44-lead PLCC and TQFP Packages**
- **Advanced Flash Technology**
  - **100% Tested**
  - **Completely Reprogrammable**
  - **100 Program/Erase Cycles**
  - **20 Year Data Retention**
  - **2000V ESD Protection**
  - **200 mA Latch-up Immunity**
- **Supported by Popular third-arty Tools**
- **Security Fuse Feature**
- **Pin-compatible with the Most Commonly Used Devices**
- **Green (Pb/Halide-fee/RoHS Compliant) Package Options**

Description

The ATF1500A is a high-performance, high-density complex PLD. Built on an advanced Flash technology, it has maximum pin-to-pin delays of 7.5 ns and supports sequential logic operation at speeds up to 125 MHz. With 32 logic macrocells and up to 36 inputs, it easily integrates logic from several TTL, SSI, MSI and classic PLDs. The ATF1500A's global input and feedback architecture simplifies logic placement and eliminates pinout changes due to design changes.

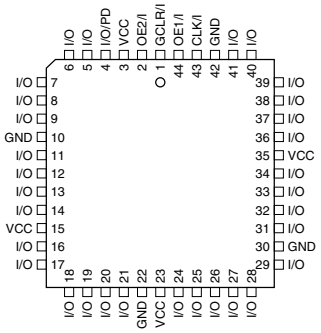
(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bi-directional Buffers
GCLR	Register Reset (active low)
OE1, OE2	Output Enable (active low)
VCC	+5V Supply
PD	Power-down (active high)

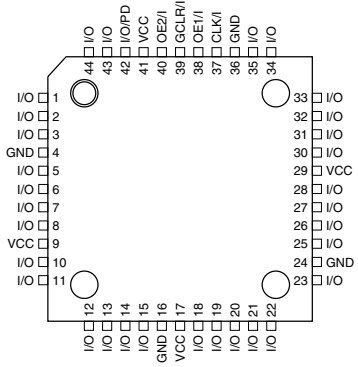
PLCC

Top View



TQFP

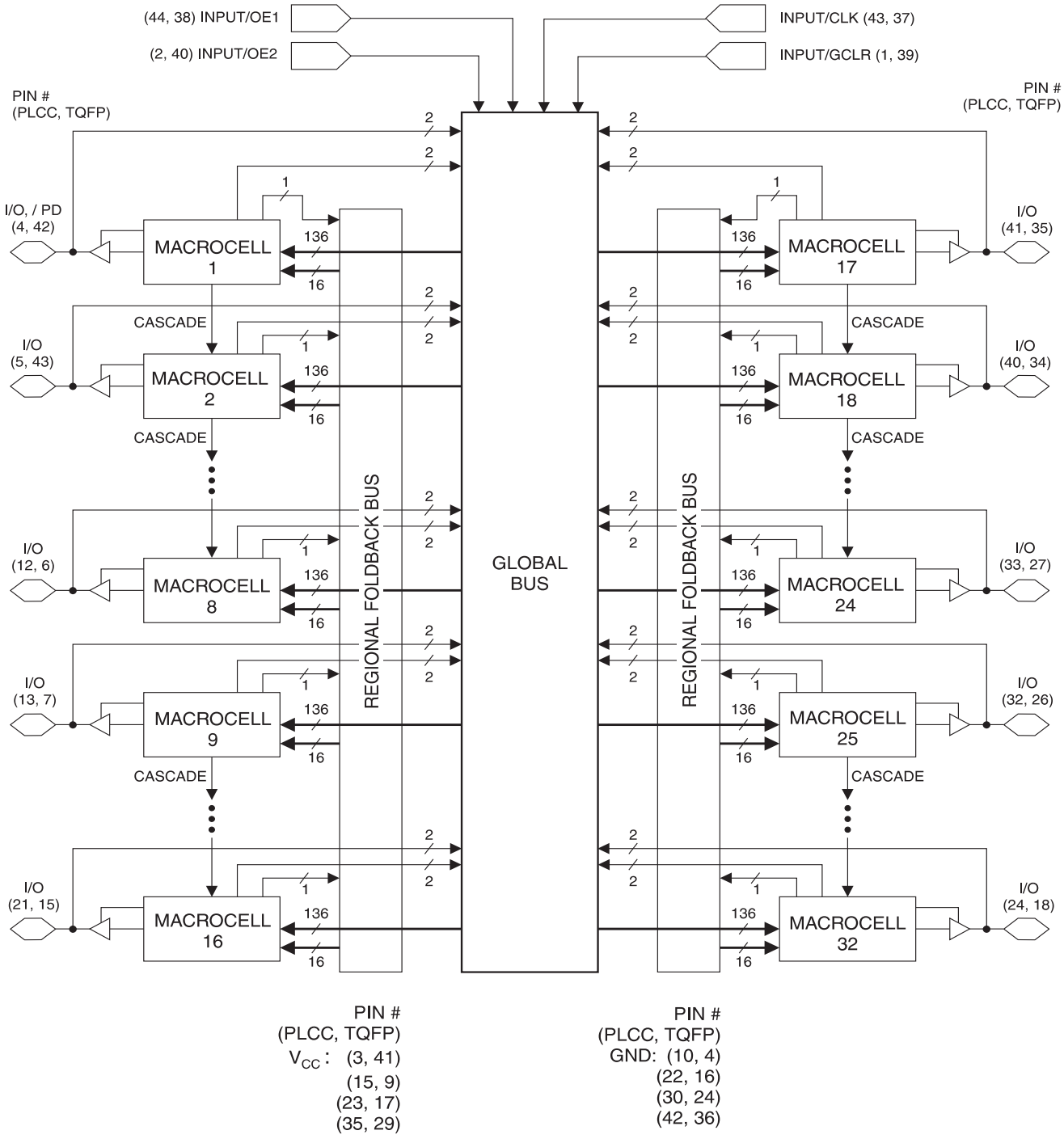
Top View



High-performance EPLD

ATF1500A
ATF1500AL

Functional Logic Diagram[1]



Note: 1. Arrows connecting macrocells indicate direction and groupings of CASIN/CASOUT data flow.

The ATF1500A has 32 bi-directional I/O pins and four dedicated input pins. Each dedicated input pin can also serve as a global control signal: register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 32 logic macrocells generates a buried feedback, which goes to the global bus. Each input and I/O pin also feeds into the global bus. Because of this global busing, each of these signals is always available to all 32 macrocells in the device.

Each macrocell also generates a foldback logic term, which goes to a regional bus. All signals within a regional bus are connected to all 16 macrocells within the region.

Cascade logic between macrocells in the ATF1500A allows fast, efficient generation of complex logic functions. The ATF1500A contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

Bus-friendly Pin-keeper Input and I/O's

All Input and I/O pins on the ATF1500A have programmable "pin-keeper" circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

This circuitry prevents unused Input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Pin-keeper circuits can be disabled. Programming is controlled in the logic design file. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

Speed/Power Management

The ATF1500A has several built-in speed and power management features. The ATF1500A contains circuitry that automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 10 MHz.

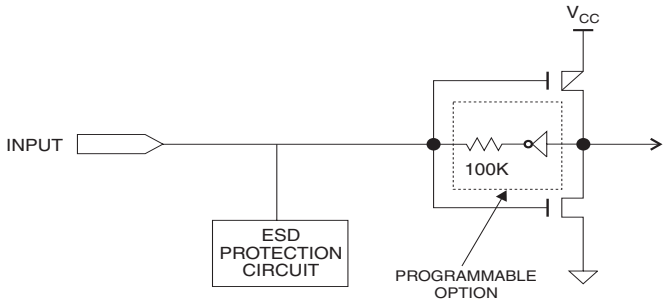
All ATF1500As also have an optional pin-controlled power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, the PD pin is used to power-down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when the PD pin is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs. All pin transitions are ignored until the PD is brought low. When the power-down feature is enabled, the PD cannot be used as a logic input or output. However, the PD pin's macrocell may still be used to generate buried foldback and cascade logic signals.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

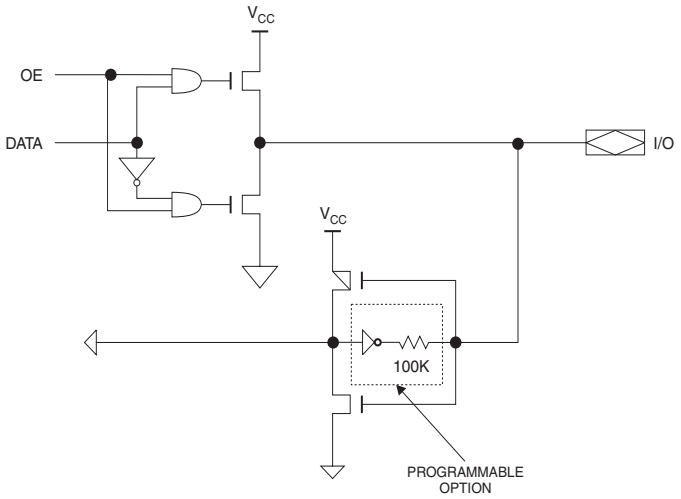
Design Software Support

ATF1500A designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages and formats.

Input Diagram



I/O Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 5.25V for pulses of less than 20 ns.

DC and AC Operating Conditions

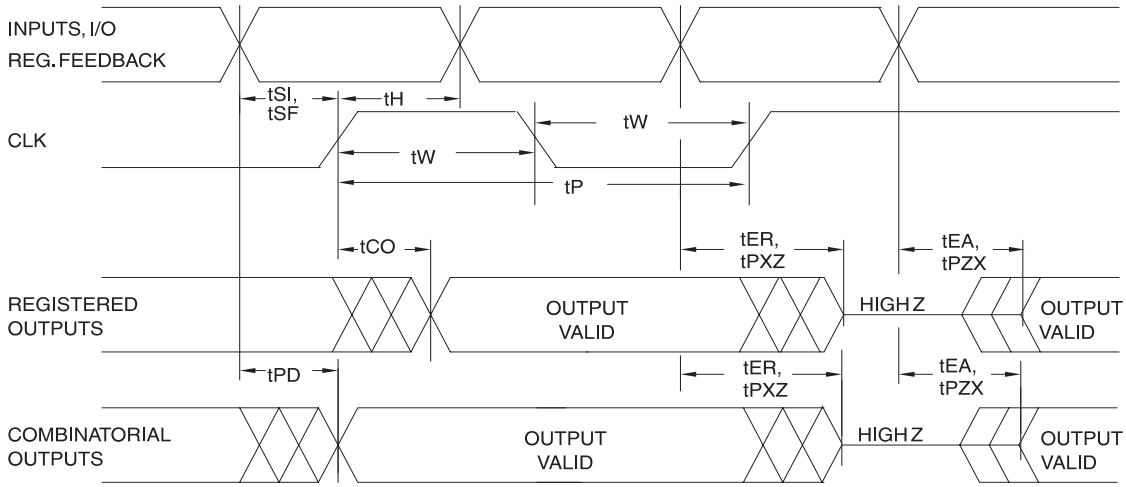
	Commercial	Industrial
Operating Temperature (ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)					-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH}, Min $\le V_{IN} \le V_{CC}$					10	µA
I_{CC1}(1)	Power Supply Current, Standby	V_{CC} = Max, V_{IN} = 0, V_{CC}	ATF1500A	Com.		70		mA
				Ind.		100		mA
			ATF1500AL	Com.			3	mA
				Ind.			5	mA
I_{CC2}	Power Supply Current, Pin-Controlled Power Down Mode	V_{CC} = Max, V_{IN} = 0, V_{CC}				2	10	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V					-130	mA
V_{IL}	Input Low Voltage	V_{CC}, Min < V_{CC} < V_{CC}, Max			-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = Min	I_{OL} = 12 mA				0.45	V
V_{OH}	Output High Voltage	V_{CC} = Min	I_{OH} = -4 mA		2.4			V
			I_{OH} = -0.2 mA		V_{CC} - 0.2			V

Note: 1. All I_{CC} parameters measured with outputs open, and a 16-bit loadable, up/down counter programmed into each region.

AC Waveforms



Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-7		-10		-12		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{COS}[1]	Clock to Output		4.5	2	5	2	6	2	8	2	9	2	9	ns
t_{CFS}	Clock to Feedback		2		2		2		2		2		2	ns
t_{SIS}	I, I/O Setup Time		6		8		10		11		14		16	ns
t_{SFS}	Feedback Setup Time		6		8		10		11		12		13	ns
t_{HS}	Input, I/O, Feedback Hold Time	0		0		0		0		0		0		ns
t_{PS}	Clock Period	6		8		9		10		11		12		ns
t_{WS}	Clock Width	3		4		4.5		5		5.5		6		ns
f_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		95		76.9		62.5		52.6		43		40	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		125		100		83.3		76.9		71		66	MHz
	No Feedback $1/(t_{PS})$		166.7		125		111		100		91		83	MHz
t_{RPRS}	Reset Pin Recovery Time	2		3		3		4		5		5		ns
t_{RTRS}	Reset Term Recovery Time	6		9		10		12		13		14		ns

Note: 1. For slow slew outputs, add t_{SSO} .

Register AC Characteristics, Product Term Clock

Symbol	Parameter	-7		-10		-12		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{COA} [1]	Clock to Output		7.5		10		12		15		18		20	ns
t_{CFA}	Clock to Feedback		5		7		7		9		12		15	ns
t_{SIA}	I, I/O Setup Time	3		3		4		4		8		10		ns
t_{SFA}	Feedback Setup Time	3		3		4		4		12		15		ns
t_{HA}	Input, I/O, Feedback Hold Time	2		3		4		4		5		5		ns
t_{PA}	Clock Period	6		8		10		12		24		30		ns
t_{WA}	Clock Width	3		4		5		6		12		15		ns
f_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		95.2		76.9		62.5		52.6		38		33.3	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		125		100		90.9		76.9		41.7		33.3	MHz
	No Feedback $1/(t_{PA})$		166.7		125		100		83.3		41.7		33.3	MHz
t_{RPRA}	Reset Pin Recovery Time	0		0		0		0			0	0		ns
t_{RTRA}	Reset Term Recovery Time	4		5		6		6			7	8		ns

Note: 1. For slow slew outputs, add t_{SSO}.

AC Characteristics

Symbol	Parameter	-7		-10		-12		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD} (1)	I, I/O or FB to Non-Registered Output	2	7.5	3	10	3	12	3	15	3	20	3	25	ns
t_{PD2}	I, I/O to Feedback		5		7		8		9		12		14	ns
t_{PD3} (1)	Feedback to Non-Registered Output	2	7.5	3	10	3	12	3	15	3	20	3	25	ns
t_{PD4}	Feedback to Feedback		5		7		8		9		12		14	ns
t_{EA} (1)	OE Term to Output Enable	2	7.5	3	10	3	12	3	15	3	20	3	25	ns
t_{ER}	OE Term to Output Disable	2	7.5	2	10	2	12	2	15	2	20	2	25	ns
t_{PZX} (1)	OE Pin to Output Enable	2	5.5	2	7	2	8	2	9	2	10	2	11	ns
t_{PXZ}	OE Pin to Output Disable	1.5	5.5	1..5	7	1.5	8	1.5	9	1.5	10	1.5	11	ns
t_{PF}	Preset to Feedback		6		9		9		12		18		20	ns
t_{PO} (1)	Preset to Registered Output		8.5		12		14		20		23		25	ns
t_{RPF}	Reset Pin to Feedback		3		4		3		5		5.5		6	ns
t_{RPO} (1)	Reset Pin to Registered Output		5.5		7		8		11		13		15	ns
t_{RTF}	Reset Term to Feedback		6		9		9		12		15		20	ns
t_{RTO} (1)	Reset Term to Registered Output		8.5		12		14		20		23		25	ns
t_{CAS}	Cascade Logic Delay		0.8		0.8		1		1		1.5		1.5	ns
t_{SSO}	Slow Slew Output Adder		3		3		3		4		4		4	ns
t_{FLD}	Foldback Term Delay		4		5		7		8		10		12	ns

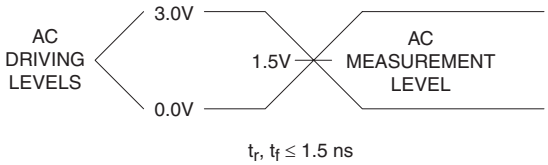
Note: 1. For slow slew outputs, add t_{SSO}.

Power Down AC Characteristics

Symbol	Parameter	-7		-10		-12		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O Before PD High	7		10		12		15		20		25		ns
t_{GVDH}	Valid OE(2) Before PD High	7		10		12		15		20		25		ns
t_{CVDH}	Valid Clock(2) Before PD High	7		10		12		15		20		25		ns
t_{DHIX}	Input Don't Care After PD High		15		20		22		25		30		35	ns
t_{DHGX}	$\overline{OE}$ Don't Care After PD High		15		20		22		25		30		35	ns
t_{DHCX}	Clock Don't Care After PD High		15		20		22		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1		1	µs
t_{DLGV}	PD Low to Valid OE(2)		1		1		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock(2)		1		1		1		1		1		1	µs
t_{DLOV}(1)	PD Low to Valid Output		1		1		1		1		1		1	µs

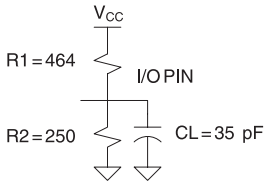
Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or Product Term.

Input Test Waveforms and Measurement Levels



t_r, $t_f \le 1.5$ ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C(1)

	Typ	Max	Units	Conditions
C_{IN}	4.5	5.5	pF	V_{IN} = 0V
C_{OUT}	3.5	4.5	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Ordering Information

Standard Package Options

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	95	ATF1500A-7AC ATF1500A-7JC	44A 44J	Commercial (0°C to 70°C)
10	5	76.9	ATF1500A-10AC ATF1500A-10JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500A-10AI ATF1500A-10JI	44A 44J	Industrial (-40°C to 85°C)
12	6	62.5	ATF1500A-12AC ATF1500A-12JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500A-12AI ATF1500A-12JI	44A 44J	Industrial (-40°C to 85°C)
15	8	52.6	ATF1500A-15AC ATF1500A-15JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500A-15AI ATF1500A-15JI	44A 44J	Industrial (-40°C to 85°C)
20	9	40	ATF1500AL-20AC ATF1500AL-20JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500AL-20AI ATF1500AL-20JI	44A 44J	Industrial (-40°C to 85°C)

Note: 1. The last time buy date is Sept. 30, 2005 for shaded parts. The replacements for fast-speed grade is the ATF1502AS (pin compatible). For others, suggested replacements are available in Green packages.

2. The ATF1500AL-25AC, -25AI, -25JC and -25JI were obsoleted in August 1999. The replacement was the ATF1500AL-20.

Using “C” Product for Industrial

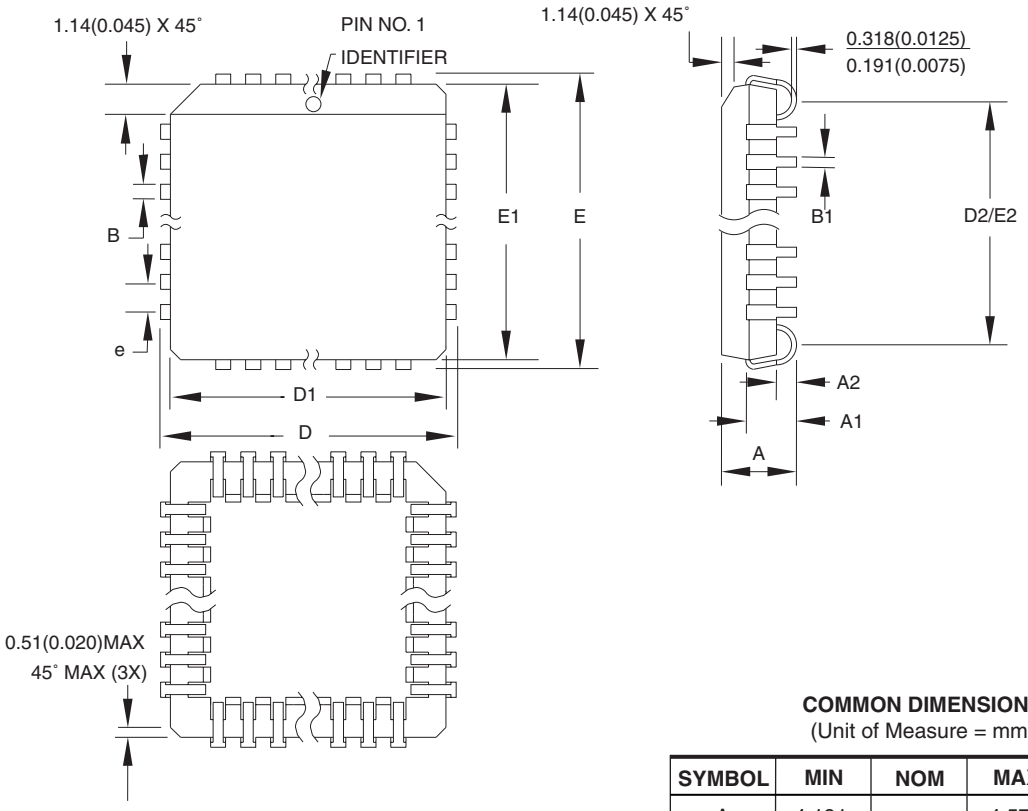
To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
10	5	76.9	ATF1500A-10AU ATF1500A-10JU	44A 44J	Industrial (-40°C to 85°C)
20	9	40	ATF1500AL-20AU ATF1500AL-20JU	44A 44J	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

TITLE	DRAWING NO.
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J