

SRM20V100LLMX7

CMOS 1 M-BIT STATIC RAM

- Low Supply Voltage
- Wide Temperature Range
- Low Supply Current
- Access Time 70ns (2.7V)
- 131,072 Words × 8-Bit Asynchronous

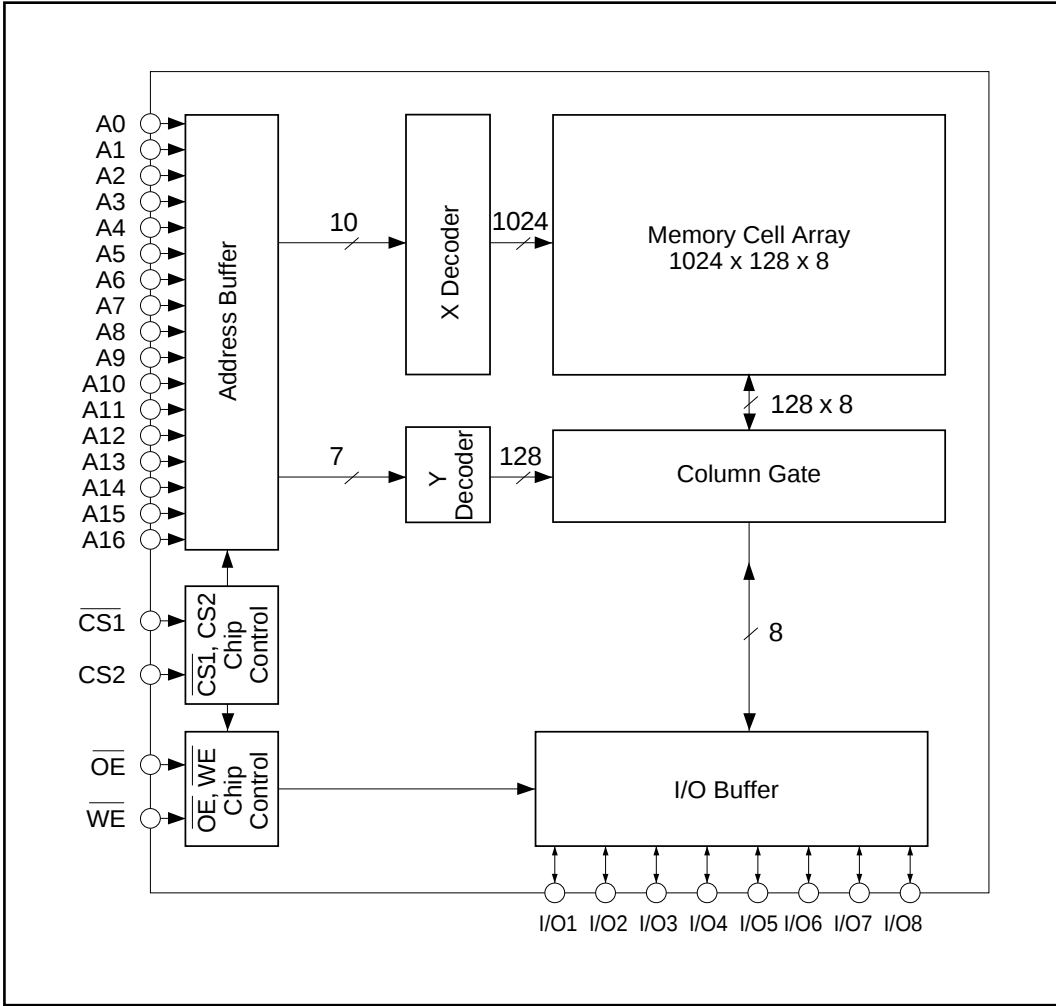
■ DESCRIPTION

The SRM20V100LLMX7 is a 131,072 words × 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The -25 to 85°C operating temperature range makes it ideal for portable equipment. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and 3-state output allows easy expansion of memory capacity.

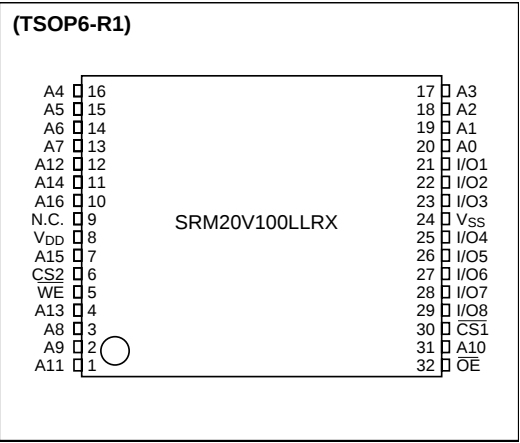
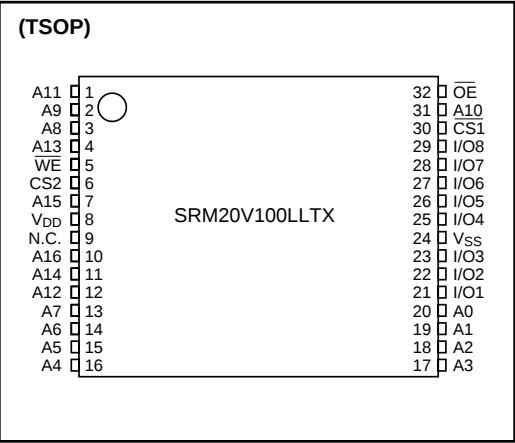
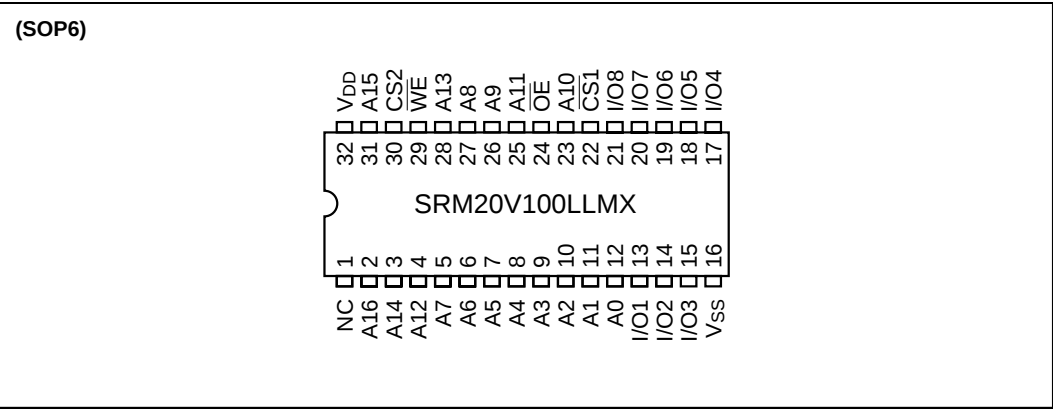
■ FEATURES

- Wide temperature range -25 to 85°C
- Fast Access time. SRM20V100LLMX7 70ns (Max.)
- Low supply current Standby: 0.6 μ A (Typ.)
Operation: 8mA/1MHz (Typ.)
- Completely static. No clock required
- Supply voltage 2.7V to 3.6V
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package SRM20V100LLMX7 SOP6-32pin (plastic)
SRM20V100LLTX7 TSOP (I)-32pin (plastic)
SRM20V100LLRX7 TSOP (I)-32pin-R1 (plastic)

■ BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

A0 to A16	Address input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$, CS2	Chip Select
I/O1 to I/O8	Data I/O
VDD	Power Supply (2.7V to 3.6V)
Vss	Power Supply (0V)
N.C.	No Connection

■ ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	−0.5 to 4.6	V
Input voltage	V _I	−0.5 to V _{DD} + 0.3	V
Input/output voltage	V _{I/O}	−0.5 to V _{DD} + 0.3	V
Power dissipation	P _D	0.5	W
Operating temperature	T _{OPR}	−25 to 85	°C
Storage temperature	T _{STG}	−65 to 150	°C
Soldering temperature and time	T _{SOL}	260°C, 10s (Lead only)	—

Note: V_I, V_{I/O} (Min.) = −3.0V (pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, T_a = −25 to 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	—	2.7	3.0	3.6	V
	V _{SS}	—	0	0	0	V
Input voltage	V _{IH}	—	2.2	—	V _{DD} + 0.3	V
	V _{IL}	—	−0.3*	—	0.4	V

* If pulse width is less than 50ns, it is −3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, T_a = –25 to 85°C)

Parameter	Symbol	Conditions	SRM20V100LLMX7			Unit
			Min	Typ*	Max	
Input leakage	I _{LI}	V _I = 0 to V _{DD}	–1	—	1	μA
Output leakage	I _{LO}	$\overline{CS1} = V_{IH}$ or CS2 = V _{IL} or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{I/O} = 0 to V _{DD}	–1	—	1	μA
Standby supply current	I _{DDS}	$\overline{CS1} = V_{IH}$ or CS2 = V _{IL}	—	—	1.0	mA
	I _{DDS1}	$\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or CS2 ≤ 0.2V	—	0.6	60	μA
Average operating current	I _{DDA}	V _I = V _{IL} , V _{IH} I _{I/O} = 0mA, t _{CYC} = Min	—	20	35	mA
	I _{DDA1}	V _I = V _{IL} , V _{IH} I _{I/O} = 0mA, t _{CYC} = 1μs	—	8	15	mA
Operating supply current	I _{DDO}	V _I = V _{IL} , V _{IH} I _{LO} = 0mA	—	8	15	mA
High level output voltage	V _{OH}	V _{DD} ≥ 3V, I _{OH} = –2.0mA	2.4	—	—	V
		I _{OH} = –100μA,	V _{DD} –0.2	—	—	
Low level output voltage	V _{OL}	V _{DD} ≥ 3V, I _{OL} = –2.0mA	—	—	0.4	V
		I _{OL} = 100μA	—	—	0.2	

*1 Typical values are measured at T_a = 25°C and V_{DD} = 3.0V

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C _{ADD}	V _{ADD} = 0V	—	—	8	pF
Input capacitance	C _I	V _I = 0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

SRM20V100LLMX7

● AC Electrical Characteristics

○ Read Cycle

VDD = 2.7V to 3.6V, VSS = 0V, Ta = -25 to 85°C

Parameter	Symbol	Conditions	SRM20V100LLMX7		Unit
			Min.	Max.	
Read cycle time	tRC	*1	70	—	ns
Address access time	tACC		—	70	ns
Chip select1 access time	tACS1		—	70	ns
Chip select2 access time	tACS2		—	70	ns
Output enable access time	tOE		—	40	ns
Chip select1 output set time	tCLZ1	*2	5	—	ns
Chip select1 output floating	tCHZ1		—	30	ns
Chip select2 output set time	tCLZ2		5	—	ns
Chip select2 output floating	tCHZ2		—	30	ns
Output enable output set time	tOLZ		0	—	ns
Output enable output floating	tOHZ		—	30	ns
Output hold time	tOH	*1	10	—	ns

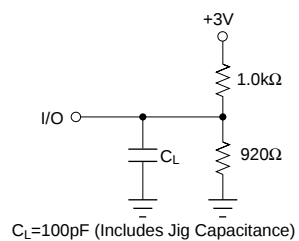
○ Write Cycle

$V_{DD} = 2.7V$ to $3.6V$, $V_{SS} = 0V$, $T_a = -25$ to $85^{\circ}C$

Parameter	Symbol	Conditions	SRM20V100LLMX7		Unit
			Min.	Max.	
Write cycle time	tWC	*1	70	—	nS
Chip Select time1	tcW1		60	—	nS
Chip Select time2	tcW2		60	—	nS
Address enable	tAW		60	—	nS
Address setup time	tAS		0	—	nS
Write pulse width	tWP		55	—	nS
Address hold time	tWR		0	—	nS
Input data setup time	tDW		30	—	nS
Input data hold time	tDH		0	—	nS
$\overline{WE}$ output floating	tWHZ	*2	—	30	nS
$\overline{WE}$ output setup time	tOW		5	—	nS

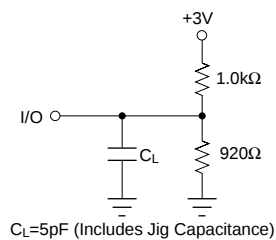
***1. Test Conditions**

1. Input pulse level: 0.4V to 2.4V
2. $t_r = t_f = 5ns$
3. Input and output timing reference levels : 1.5V
4. Output load $C_L = 100pF$



***2. Test Conditions**

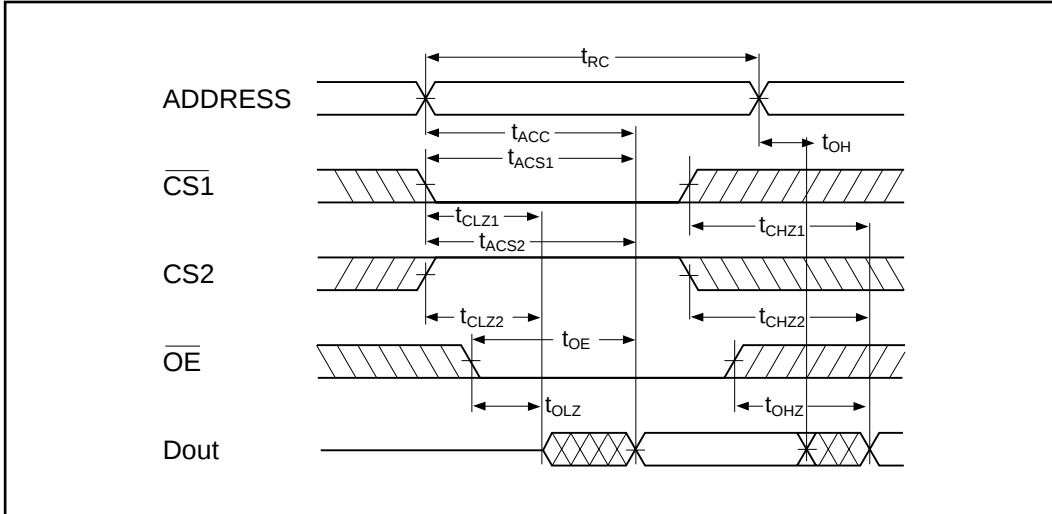
1. Input pulse level: 0.4V to 2.4V
2. $t_r = t_f = 5ns$
3. Input timing reference levels : 1.5V
4. Output timing reference levels: $\pm 200mV$ (the level displaced from stable output voltage level)
5. Output load $C_L = 5pF$



SRM20V100LLMX7

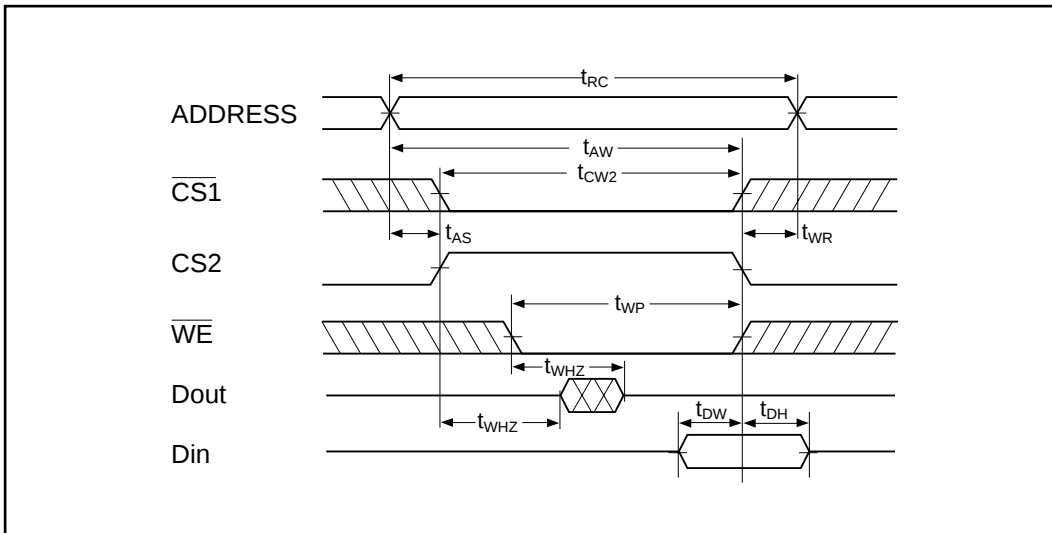
● Timing Charts

○ Read Cycle*1



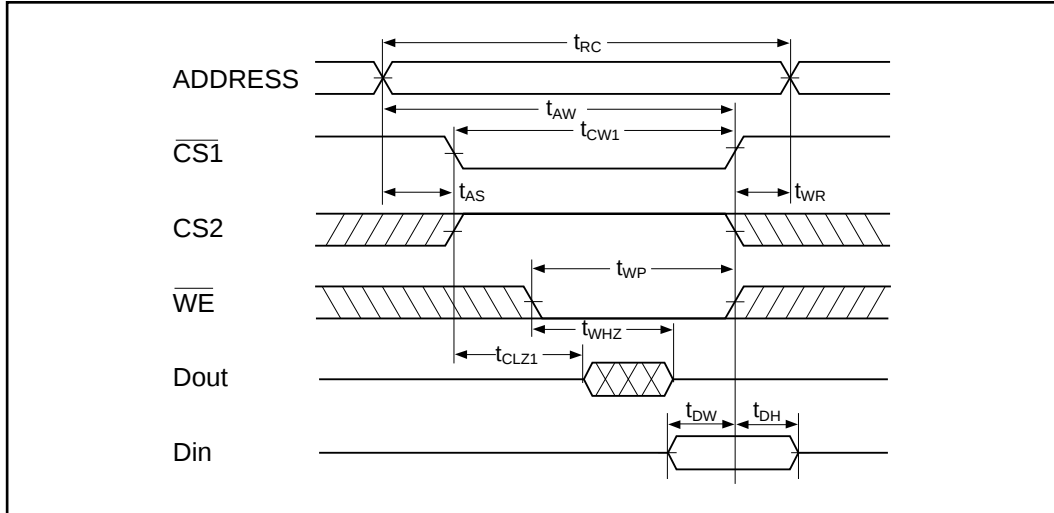
Note: *1. During the read cycle, $\overline{WE}$ must be "H".

○ Write Cycle (1) ($\overline{CS1}$ Control)*2



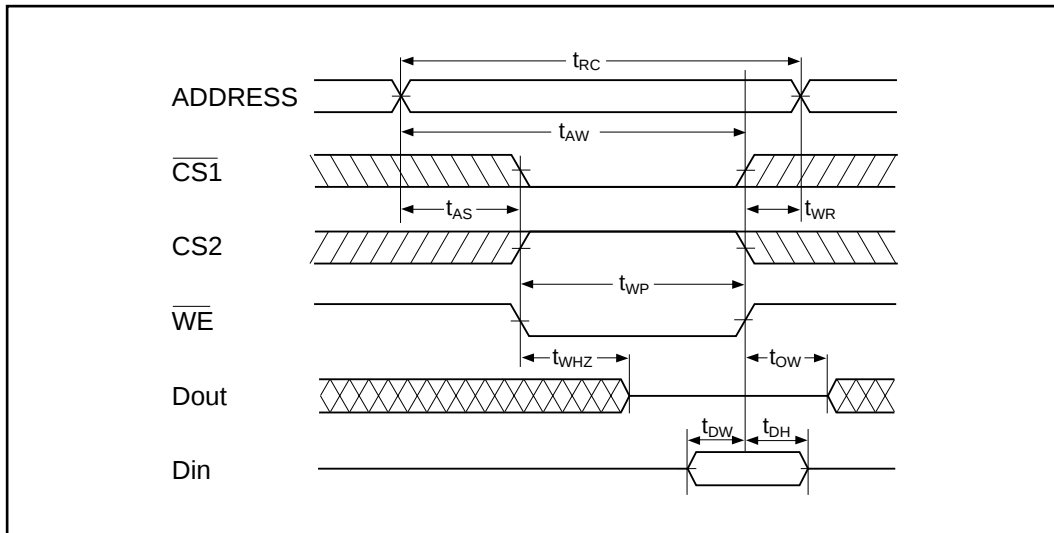
Note: *2. During write cycle that is controlled by $\overline{CS1}$ or $\overline{CS2}$, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".

○ Write Cycle (2) (CS2 Control)*2



Note: *2. During write cycle that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".

○ Write Cycle (3) ($\overline{WE}$ Control)*3, *4



Note: *3. During write cycle that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "H" level.

*4. When I/O terminals are output mode, be careful not to give the opposite signals to the I/O terminals.

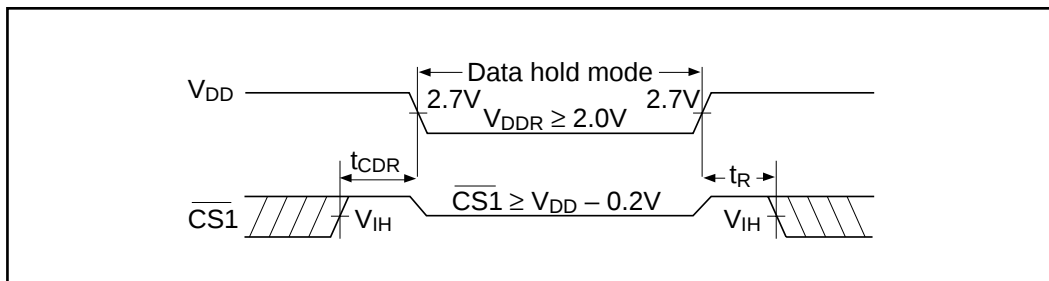
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

$V_{SS} = 0V$, $T_a = -25$ to $85^\circ C$

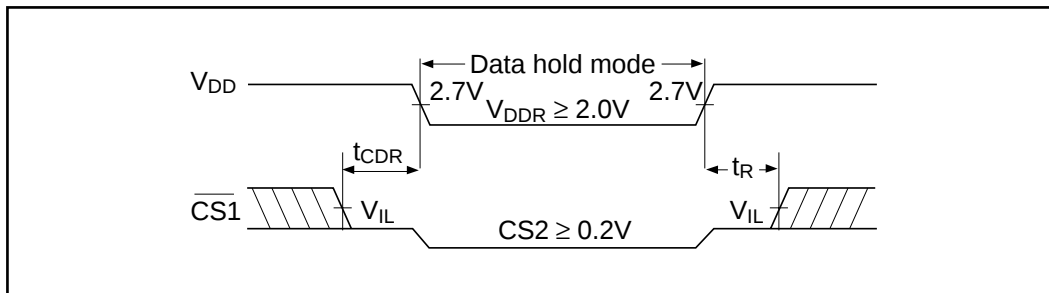
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	3.6	V
Data retention current	I_{DDR}	$V_{DD} = 2.7V$ $\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	—	0.5*	50	μA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		5	—	—	ms

* $T_a = 25^\circ C$

● Data Retention Timing ($\overline{CS1}$ Control)



● Data Retention Timing ($CS2$ Control)



* When retaining data in standby mode, supply voltage can be lowered within a certain range. But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Data I/O	Mode	I _{DD}
H	X	X	X	Hi-Z	Unselected	I _{DDS} , I _{DDS1}
X	L	X	X	Hi-Z	Unselected	I _{DDS} , I _{DDS1}
L	H	X	L	Input data	Write	I _{DDO}
L	H	L	H	Output data	Read	I _{DDO}
L	H	H	H	Hi-Z	Output disable	I _{DDO}

X: "H" or "L"

● Reading Data

Data is able to be read when the address is set while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since data I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing Data

There are the following 4 ways of writing data into memory:

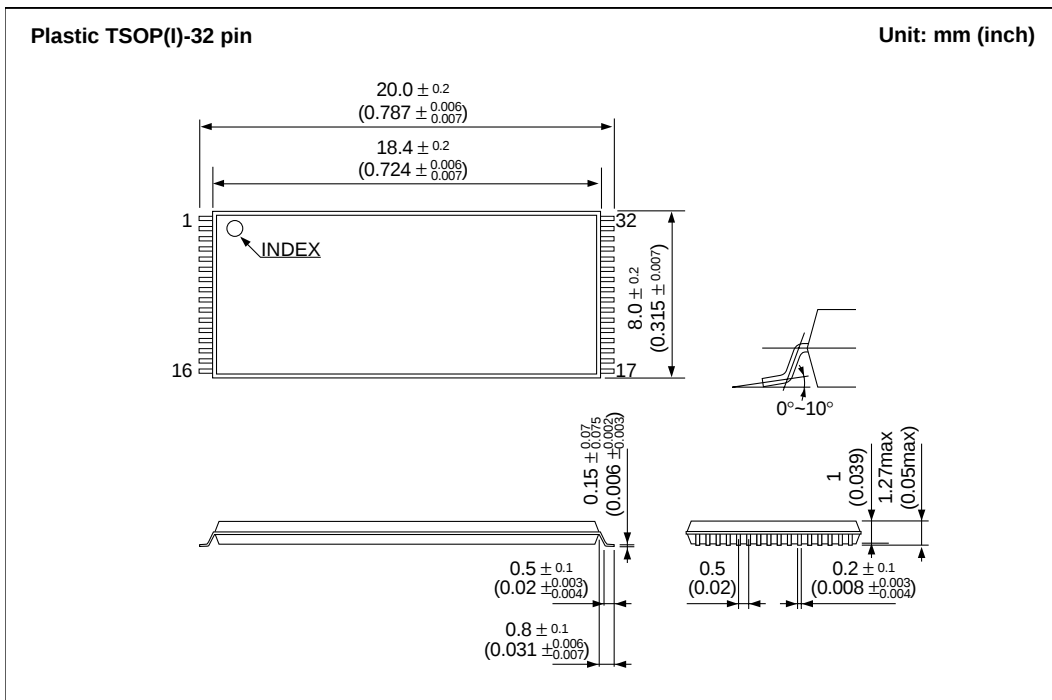
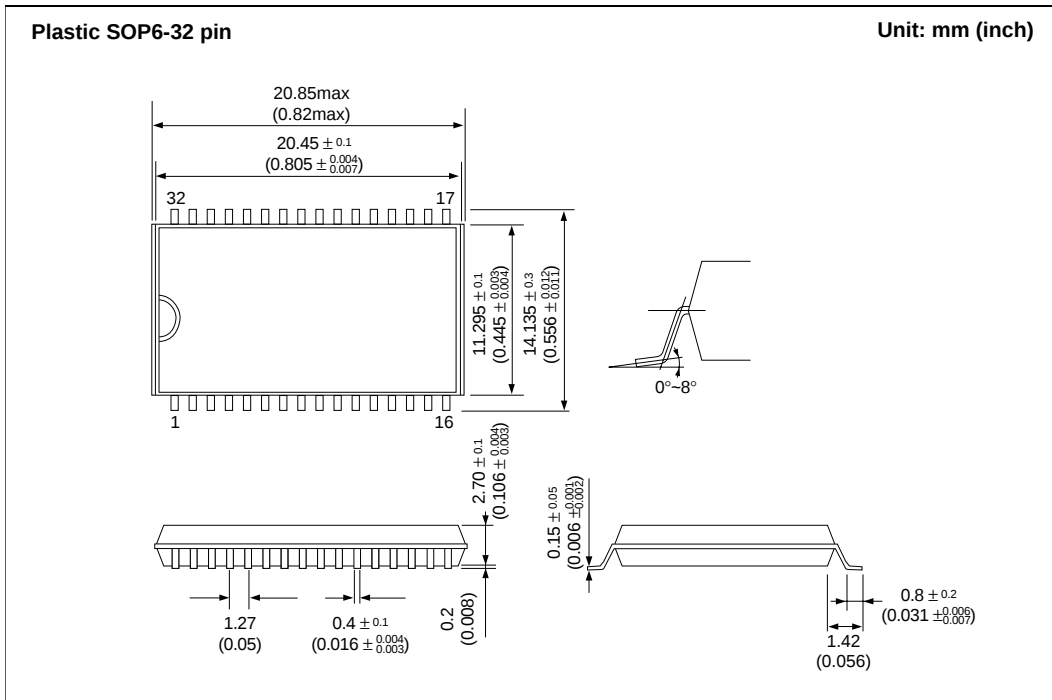
- (1) Hold CS2 = "H", $\overline{WE}$ = "L", set addresses and give "L" pulse to $\overline{CS1}$.
- (2) Hold $\overline{CS1}$ = "L", $\overline{WE}$ = "L", set addresses and give "H" pulse to CS2.
- (3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to $\overline{WE}$.
- (4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

Anyway, data on the data I/O terminals are latched up into the SRM20V100LLMX7 at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$ = "H", or CS2 = "L", the contention on the data bus can be avoided.

● Standby Mode

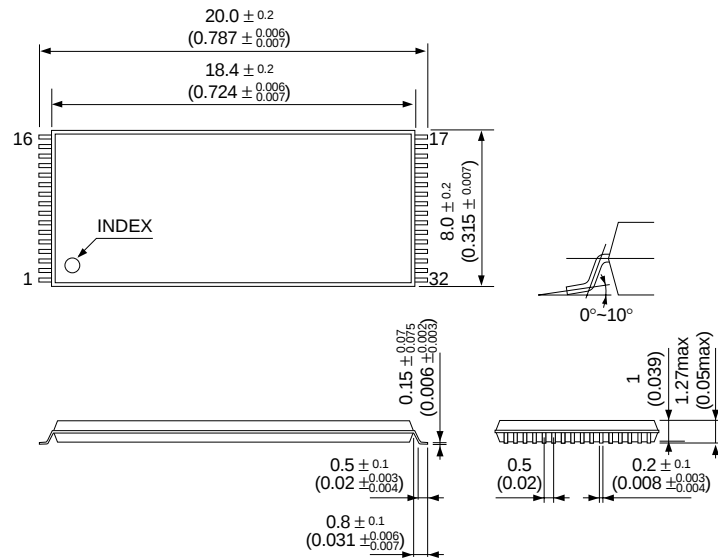
When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM20V100LLMX7 is in the standby mode which has retaining data operation. In this case, data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS1}$ and CS2 level are in the range over $V_{DD}-0.2V$, CS2 level is in the range under 0.2V, in the SRM20V100LLMX7 there is almost no current flow except through the high resistance parts of the memory.

■ PACKAGE DIMENSIONS

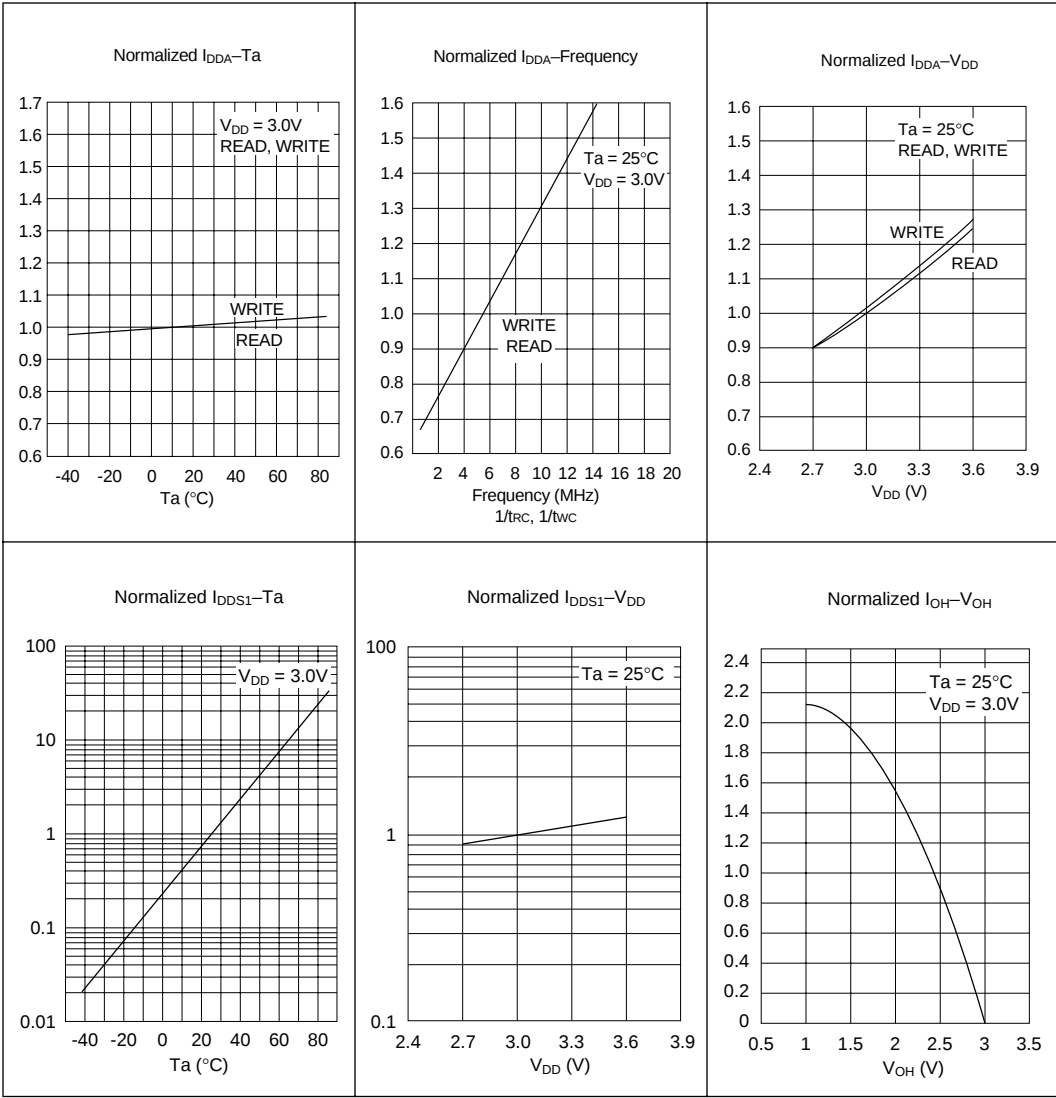


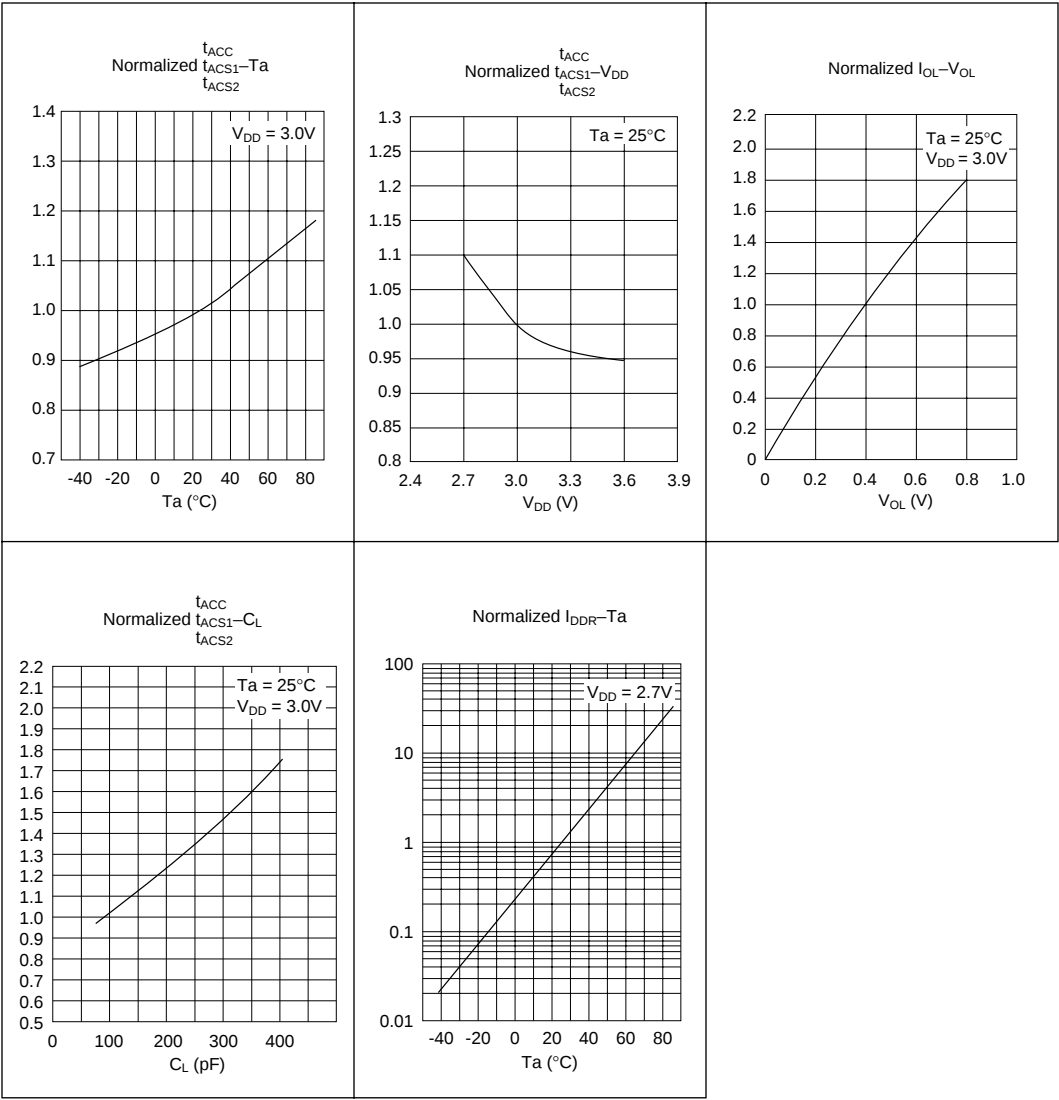
Plastic TSOP (I)-32 pin-R1

Unit: mm (inch)



■ CHARACTERISTIC CURVES





THIS PAGE INTENTIONALLY BLANK