FAIRCHILD SEMICONDUCTOR™

April 1988
Revised September 2000

74F148
8-Line to 3-Line Priority Encoder

General Description

The F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

Features

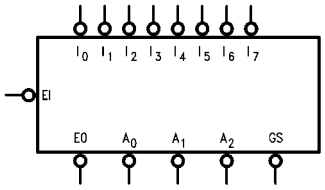
- Encodes eight data lines in priority
- Provides 3-bit binary priority code
- Input enable capability
- Signals when data is present on any input
- Cascadable for priority encoding of n bits

Ordering Code:

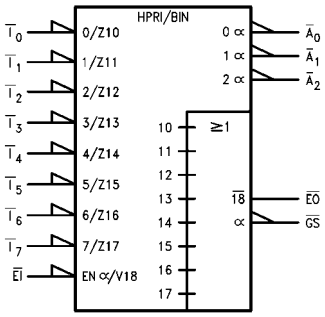
Order Number	Package Number	Package Description
74F148SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F148SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F148PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

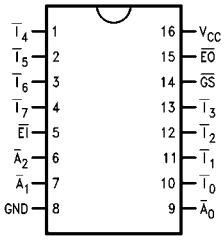
Logic Symbols



IEEE/IEC



Connection Diagram



Truth Table

Inputs									Outputs				
$\overline{EI}$	$\overline{I_0}$	$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

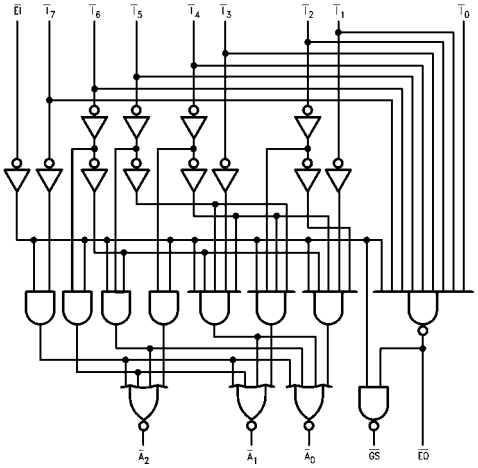
Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{I}_0$	Priority Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{I}_1$–$\overline{I}_7$	Priority Inputs (Active LOW)	1.0/2.0	20 µA/–1.2 mA
$\overline{EI}$	Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{EO}$	Enable Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{GS}$	Group Signal Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{A}_0$–$\overline{A}_2$	Address Outputs (Active LOW)	50/33.3	–1 mA/20 mA

Functional Description

The F148 8-input priority encoder accepts data from eight active LOW inputs ($\overline{I}_0$–$\overline{I}_7$) and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.A Group Signal output ($\overline{GS}$) and Enable Output ($\overline{EO}$) are provided along with the three priority data outputs ($\overline{A}_2$, $\overline{A}_1$, $\overline{A}_0$). $\overline{GS}$ is active LOW when any input is LOW: this indicates when any input is active. $\overline{EO}$ is active LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows cascading for priority encoding on any number of input signals. Both $\overline{EO}$ and $\overline{GS}$ are in the inactive HIGH state when the Enable Input is HIGH.

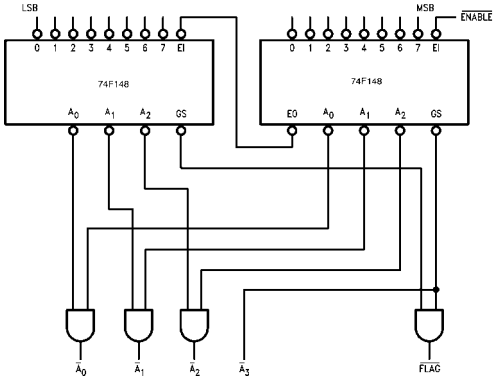
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Application

16-Input Priority Encoder



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

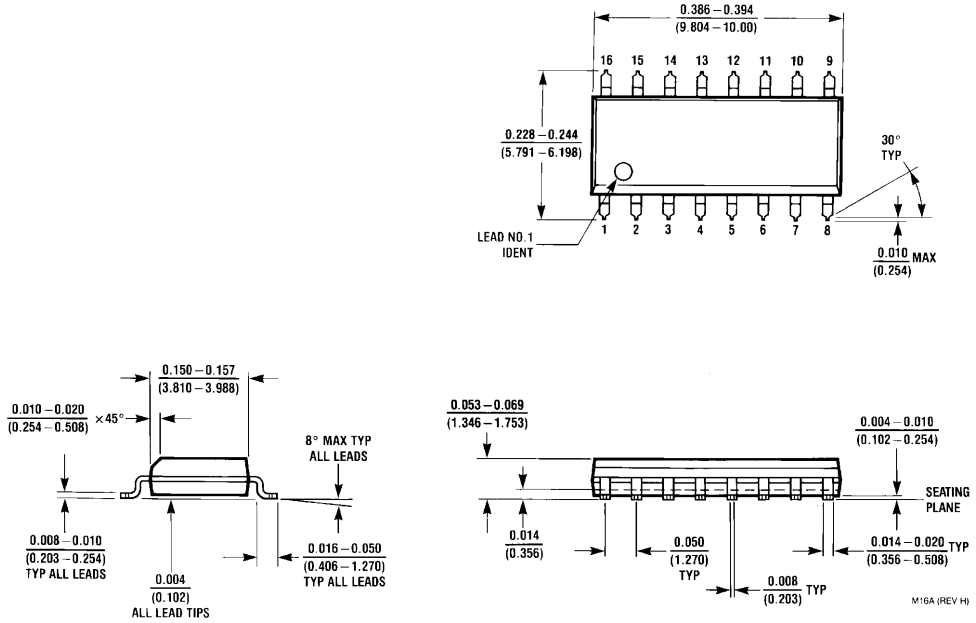
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output High Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V ($\bar{I}_0$, $\overline{EI}$)
					−1.2	mA		V_{IN} = 0.5V ($\bar{I}_1$–$\bar{I}_7$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current				35	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				35	mA	Max	V_O = LOW

AC Electrical Characteristics

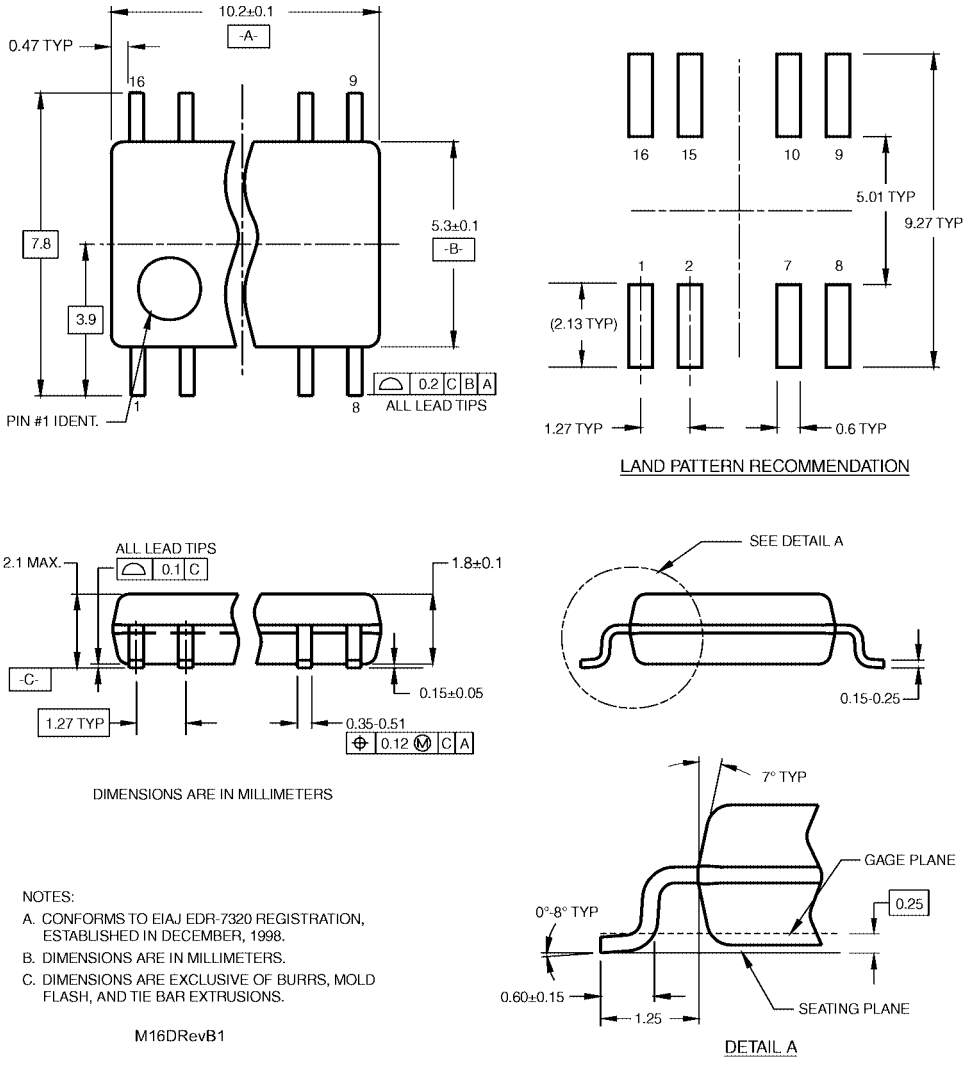
Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	7.0	9.0	3.0	10.0	ns
t_{PHL}	$\overline{I}_n$ to $\overline{A}_n$	3.0	8.0	10.5	3.0	12.0	
t_{PLH}	Propagation Delay	2.5	5.0	6.5	2.5	7.5	ns
t_{PHL}	$\overline{I}_n$ to $\overline{EO}$	2.5	5.5	7.5	2.5	8.5	
t_{PLH}	Propagation Delay	2.5	7.0	9.0	2.5	10.0	ns
t_{PHL}	$\overline{I}_n$ to $\overline{GS}$	2.5	6.0	8.0	2.5	9.0	
t_{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	9.5	ns
t_{PHL}	$\overline{EI}$ to $\overline{A}_n$	2.5	6.0	8.0	2.5	9.0	
t_{PLH}	Propagation Delay	2.5	5.0	7.0	2.5	8.0	ns
t_{PHL}	$\overline{EI}$ to $\overline{GS}$	2.5	6.0	7.5	2.5	8.5	
t_{PLH}	Propagation Delay	2.5	5.5	7.0	2.5	8.0	ns
t_{PHL}	$\overline{EI}$ to $\overline{EO}$	3.0	8.0	10.5	3.0	12.0	

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

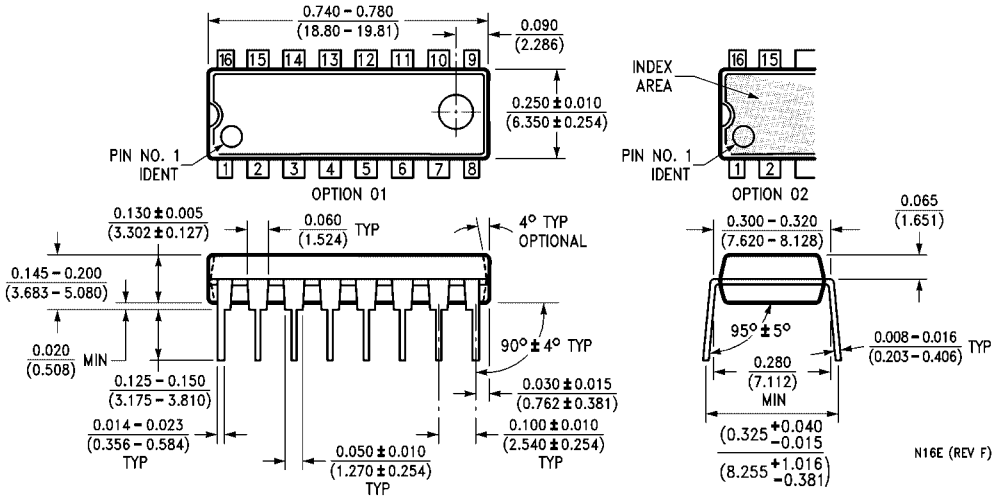
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E