



HEF4528B

Dual monostable multivibrator

Rev. 12 — 19 August 2024

Product data sheet

1. General description

The HEF4528B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW input ($\overline{nA}$), and active HIGH input (nB), an active LOW clear direct input ($\overline{nCD}$), an output (nQ) and its complement ($\overline{nQ}$), and two external timing component connecting pins ($nCEXT$, always connected to ground, and $nREXT/CEXT$).

An external timing capacitor (C_{EXT}) must be connected between $nCEXT$ and $nREXT/CEXT$ and an external resistor (R_{EXT}) must be connected between $nREXT/CEXT$ and V_{DD} . The output pulse duration is determined by the external timing components C_{EXT} and R_{EXT} . A HIGH-to-LOW transition on $\overline{nA}$ when nB is LOW or a LOW-to-HIGH transition on nB when $\overline{nA}$ is HIGH produces a positive pulse (LOW-HIGH-LOW) on nQ and a negative pulse (HIGH-LOW-HIGH) on $\overline{nQ}$ if the $\overline{nCD}$ is HIGH. A LOW on $\overline{nCD}$ forces nQ LOW, $\overline{nQ}$ HIGH and inhibits any further pulses until $\overline{nCD}$ is HIGH.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

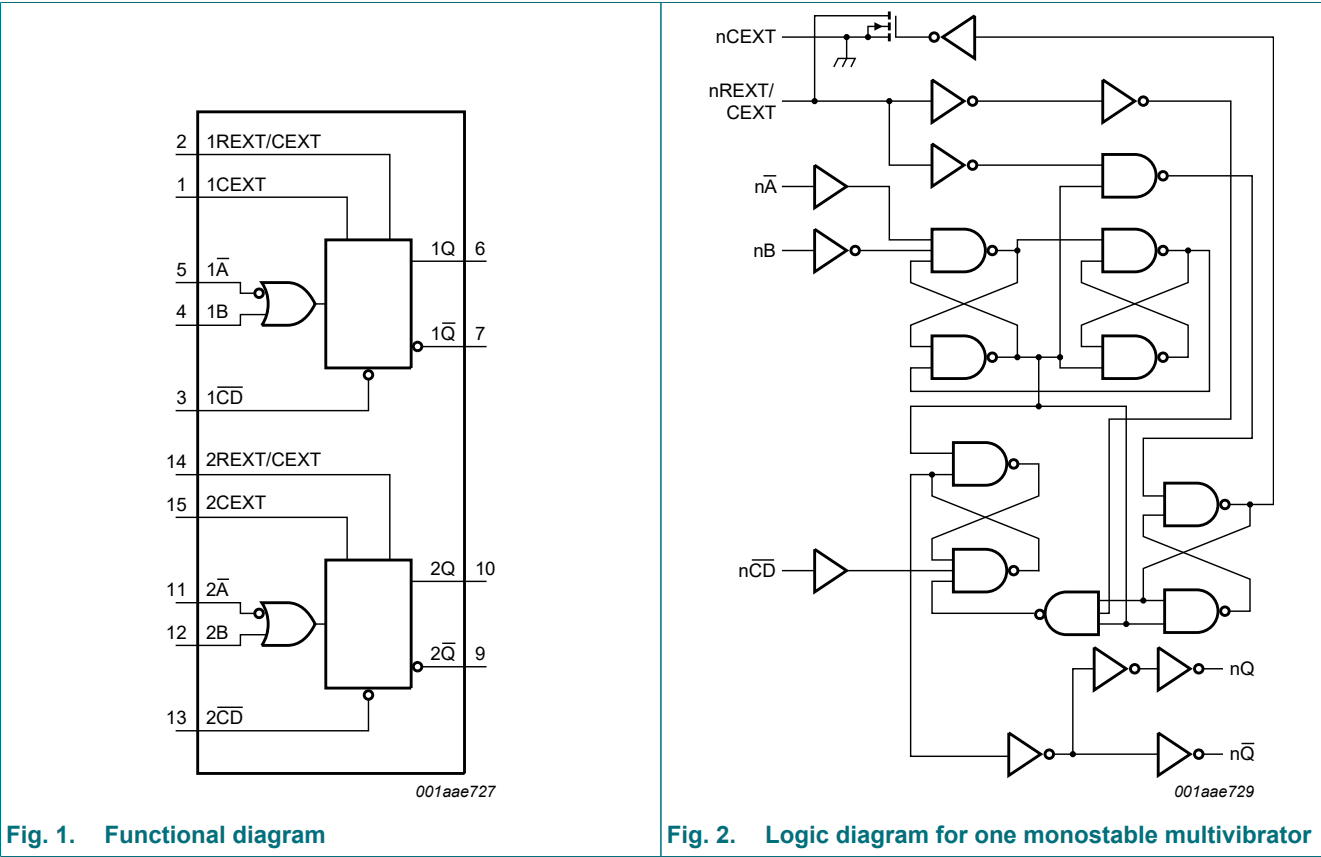
- Fully static operation
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

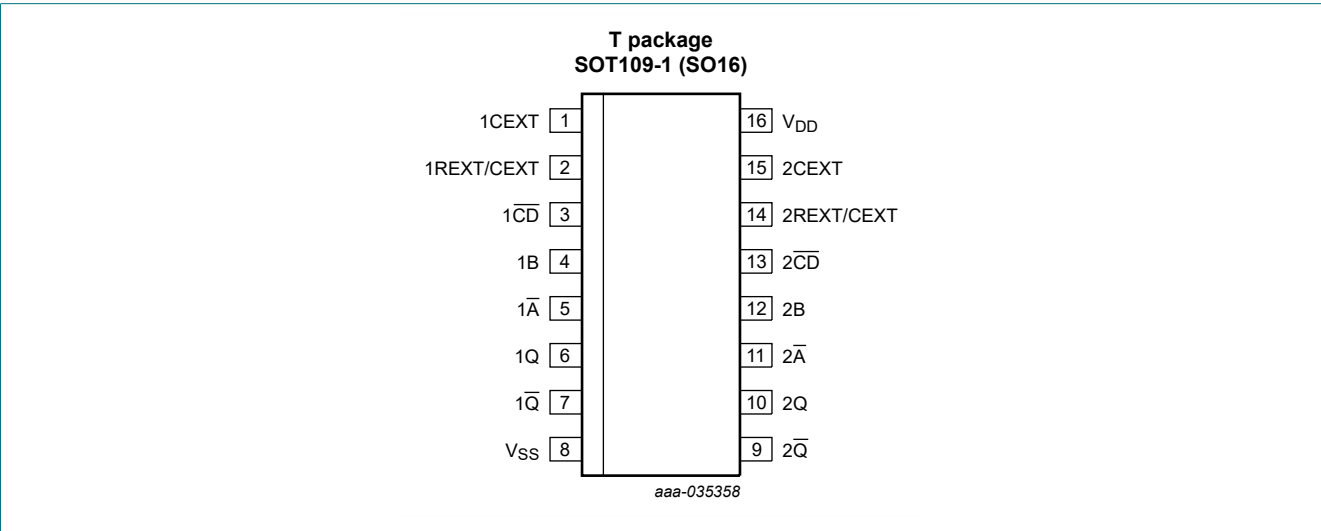
Type number	Package			
	Temperature range	Name	Description	Version
HEF4528BT	40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CEXT, 2CEXT	1, 15	external capacitor connection (always connected to ground)
1REXT/CEXT, 2REXT/CEXT	2, 14	external capacitor/resistor connection
1CD, 2CD	3, 13	clear direct input (active LOW)
1B, 2B	4, 12	input (LOW-to-HIGH triggered)
1A, 2A	5, 11	input (HIGH-to-LOW triggered)
1Q, 2Q	6, 10	output
1Q, 2Q	7, 9	complementary output (active LOW)
V _{SS}	8	ground supply voltage
V _{DD}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = positive-going transition; ↓ = negative-going transition;
 = one HIGH level output pulse, with the pulse width determined by C_{EXT} and R_{EXT};
 = one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.

Inputs			Outputs	
A	B	CD	Q	Q
↓	L	H		
H	↑	H		
X	X	L	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		3	15	V
V _I	input voltage		0	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{DD} = 5 V	-	3.75	µs/V
		V _{DD} = 10 V	-	0.5	µs/V
		V _{DD} = 15 V	-	0.08	µs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I _{DD}	supply current	all valid input combinations; I _O = 0 A	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified; for waveforms see Fig. 3 to Fig. 5; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	$n\bar{A}$ or nB to $n\bar{Q}$; see Fig. 4	5 V	$113\text{ ns} + (0.55\text{ ns/pF})C_L$	-	140	280	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
		$n\bar{CD}$ to nQ ; see Fig. 4	5 V	$78\text{ ns} + (0.55\text{ ns/pF})C_L$	-	105	210	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	85	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	$n\bar{A}$ or nB to nQ ; see Fig. 4	5 V	$128\text{ ns} + (0.55\text{ ns/pF})C_L$	-	155	305	ns
			10 V	$49\text{ ns} + (0.23\text{ ns/pF})C_L$	-	60	115	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
		$n\bar{CD}$ to $n\bar{Q}$; see Fig. 4	5 V	$93\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	105	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
t_t	transition time	nQ , $n\bar{Q}$; see Fig. 4	5 V [2]	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t_{rec}	recovery time	$n\bar{CD}$ to $n\bar{A}$ or nB ; see Fig. 5	5 V		0	-75	-	ns
			10 V		0	-30	-	ns
			15 V		0	-25	-	ns
t_{su}	set-up time	$n\bar{CD}$ to $n\bar{A}$ or nB ; see Fig. 5	5 V		0	-105	-	ns
			10 V		0	-40	-	ns
			15 V		0	-25	-	ns
t_W	pulse width	$n\bar{A}$ LOW; minimum width; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nB HIGH; minimum width; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		$n\bar{CD}$ LOW; minimum width; see Fig. 5	5 V		60	30	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns
		nQ or $n\bar{Q}$; $R_{EXT} = 5\text{ k}\Omega$; $C_{EXT} = 15\text{ pF}$; see Fig. 5	5 V [3]		-	235	-	ns
			10 V		-	155	-	ns
			15 V		-	140	-	ns
		nQ or $n\bar{Q}$; $R_{EXT} = 10\text{ k}\Omega$; $C_{EXT} = 1\text{ nF}$; see Fig. 5	5 V [4]		-	5.45	-	μs
			10 V		-	4.95	-	μs
			15 V		-	4.85	-	μs

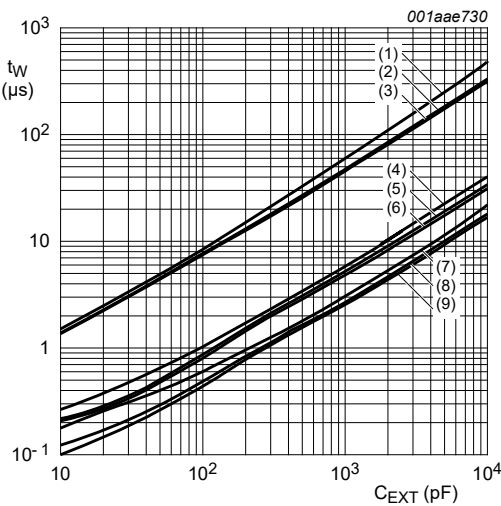
Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
Δt_W	pulse width variation	nQ output variation over temperature range	5 V [5]		-	±3	-	%
			10 V		-	±2	-	%
			15 V		-	±2	-	%
		nQ output variation over voltage range V _{DD} ± 5 %	5 V		-	±2	-	%
			10 V		-	±1	-	%
			15 V		-	±1	-	%
R _{EXT}	external timing resistor	see Fig. 3	5 V		5	-	2	MΩ
			10 V		5	-	2	MΩ
			15 V		5	-	2	MΩ
C _{EXT}	external timing capacitor	see Fig. 3	5 V		no limits			
			10 V		no limits			
			15 V		no limits			

- [1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
- [2] t_i is the same as t_{THL} and t_{TLH}.
- [3] For other R_{EXT}, C_{EXT} combinations and C_{EXT} < 0.01 μF see Fig. 3.
- [4] For other R_{EXT}, C_{EXT} combinations and C_{EXT} > 0.01 μF use formula t_W = K × R_{EXT} × C_{EXT}.
where: t_W = output pulse width (s);
R_{EXT} = external timing resistor (Ω);
C_{EXT} = external timing capacitor (F);
K = 0.42 for V_{DD} = 5 V;
K = 0.32 for V_{DD} = 10 V;
K = 0.30 for V_{DD} = 15 V.
- [5] T_{amb} = -40 °C to +85 °C; Δt_W is referenced to t_W at T_{amb} = 25 °C.

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

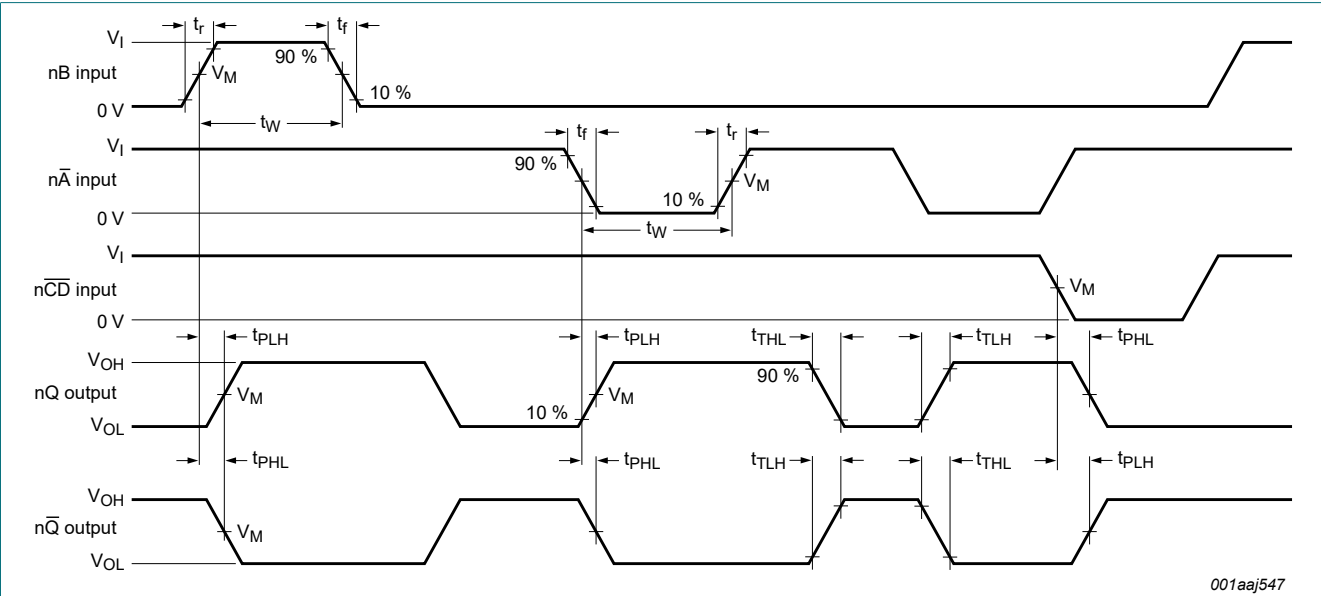
Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	where:
P _D	dynamic power dissipation	5 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f _i = input frequency in MHz; f _o = output frequency in MHz; C _L = output load capacitance in pF; V _{DD} = supply voltage in V; Σ(f _o × C _L) = sum of the outputs.
		10 V	$P_D = 20000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 59000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	



- (1) $R_{EXT} = 100\text{ k}\Omega$, $V_{DD} = 5\text{ V}$.
- (2) $R_{EXT} = 100\text{ k}\Omega$, $V_{DD} = 10\text{ V}$.
- (3) $R_{EXT} = 100\text{ k}\Omega$, $V_{DD} = 15\text{ V}$.
- (4) $R_{EXT} = 10\text{ k}\Omega$, $V_{DD} = 5\text{ V}$.
- (5) $R_{EXT} = 10\text{ k}\Omega$, $V_{DD} = 10\text{ V}$.
- (6) $R_{EXT} = 10\text{ k}\Omega$, $V_{DD} = 15\text{ V}$.
- (7) $R_{EXT} = 5\text{ k}\Omega$, $V_{DD} = 5\text{ V}$.
- (8) $R_{EXT} = 5\text{ k}\Omega$, $V_{DD} = 10\text{ V}$.
- (9) $R_{EXT} = 5\text{ k}\Omega$, $V_{DD} = 15\text{ V}$.

Fig. 3. Output pulse width (t_W) as a function of external timing capacitor (C_{EXT})

10.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 4. Waveforms showing propagation delays and transition times

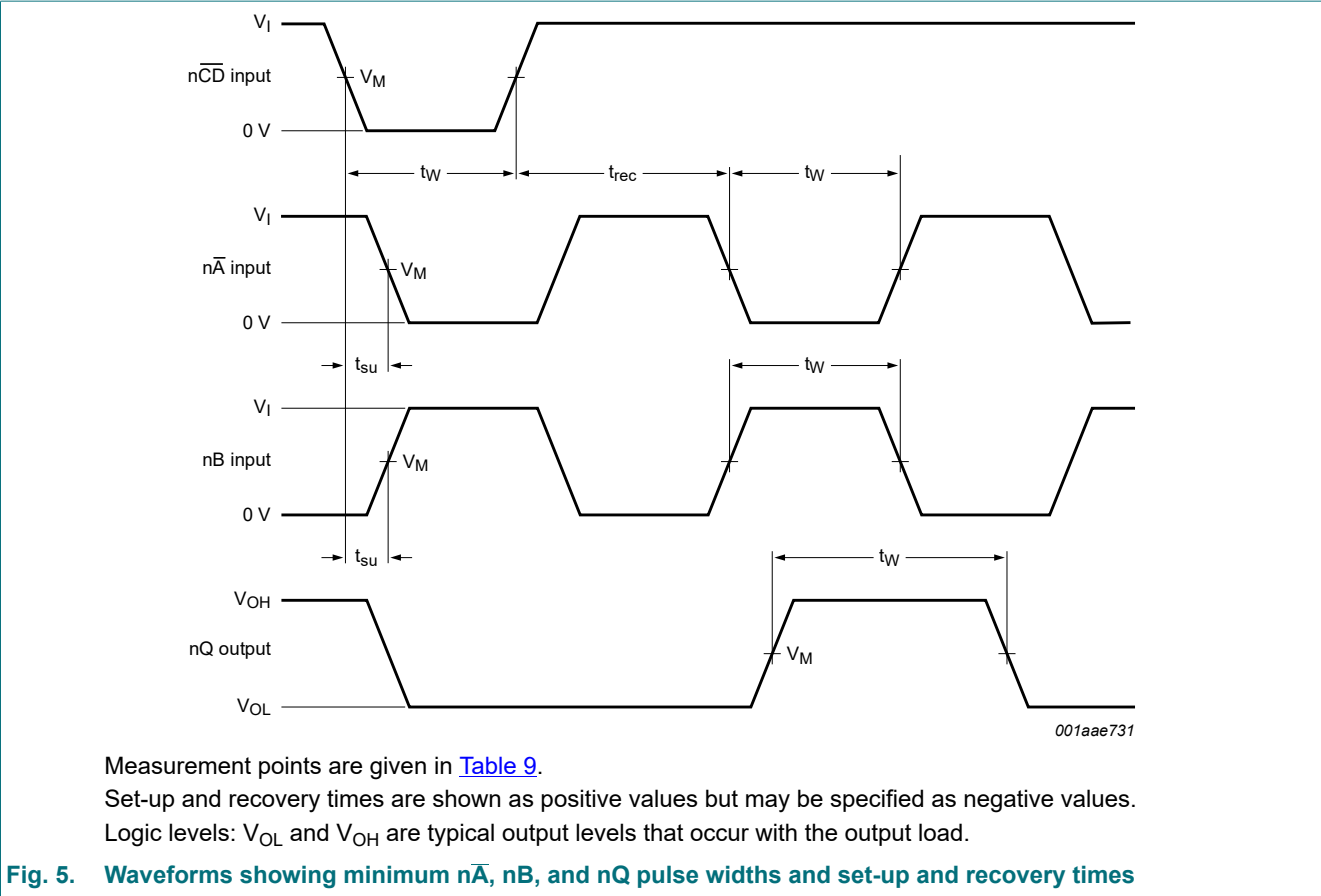
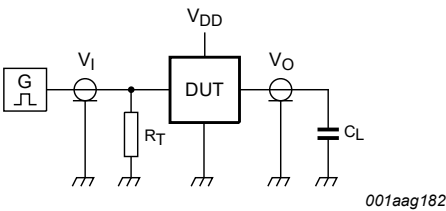


Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$



Test data is given in [Table 10](#).
Definitions for test circuit:
 C_L = load capacitance including jig and probe capacitance;
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. Application information

An example of a HEF4528B application is:

- Non-retriggerable monostable multivibrator

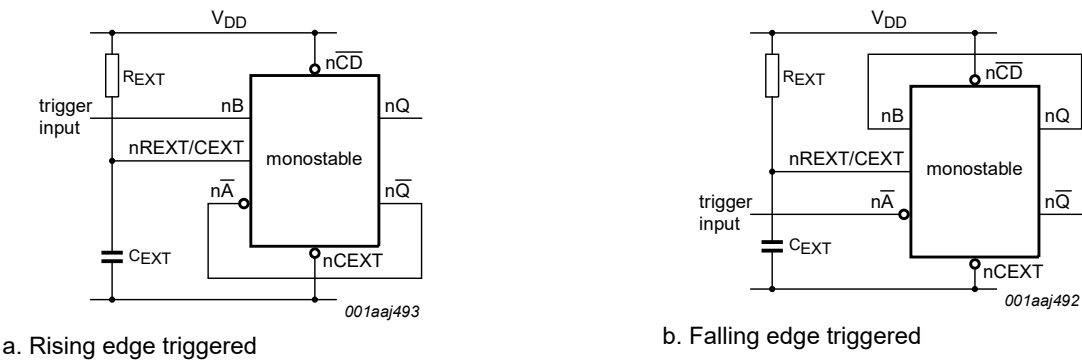


Fig. 7. Non-retriggerable applications

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

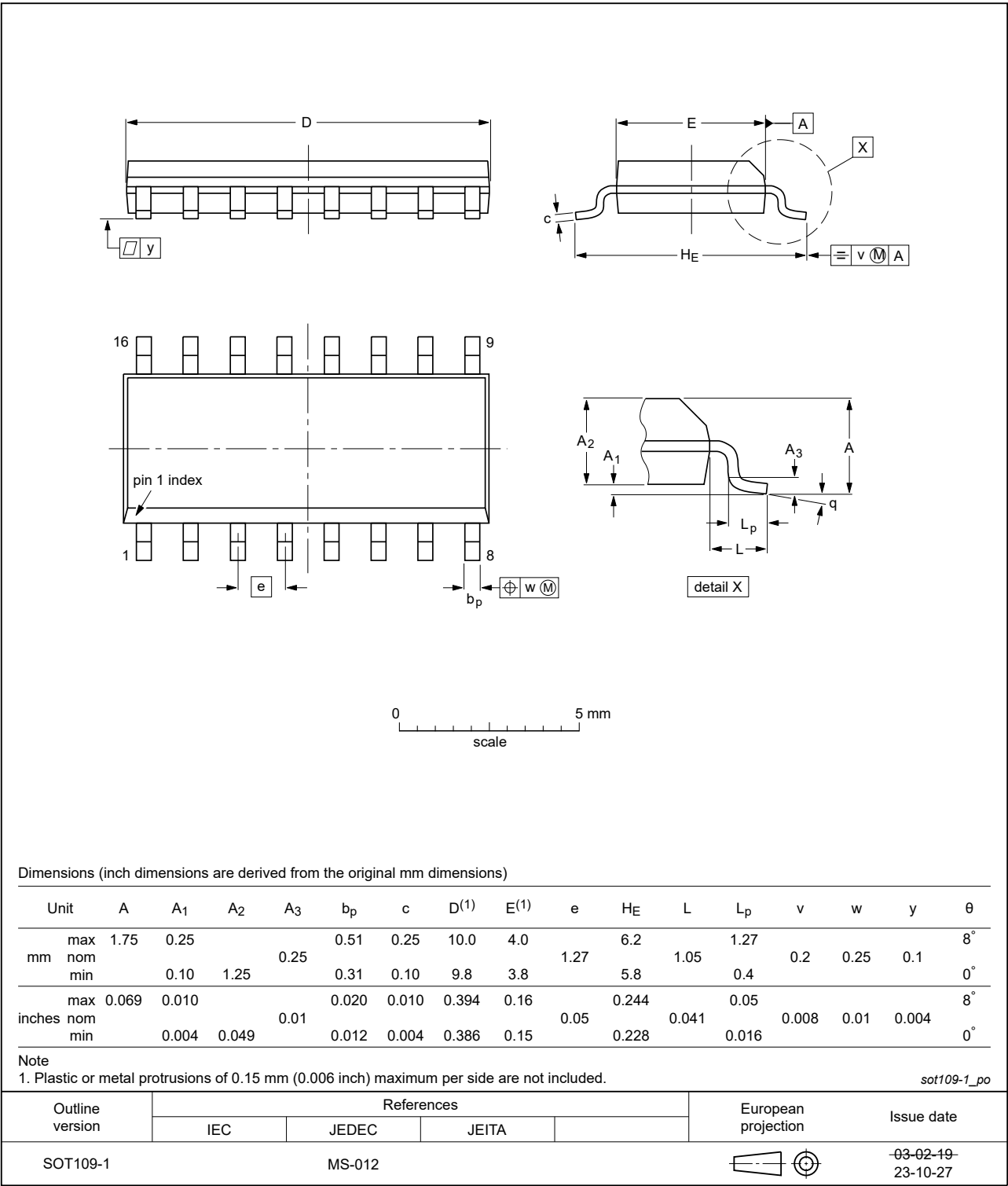


Fig. 8. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4528B v.12	20240819	Product data sheet	-	HEF4528B v.11
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 8: Aligned SO package outline drawing to JEDEC MS-012			
HEF4528B v.11	20220304	Product data sheet	-	HEF4528B v.10
Modifications:	Section 2 and Section 13 updated.			
HEF4528B v.10	20170314	Product data sheet	-	HEF4528B v.9
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
HEF4528B v.9	20160530	Product data sheet	-	HEF4528B v.8
Modifications:	Fig. 2: Logic diagram modified.			
HEF4528B v.8	20160331	Product data sheet	-	HEF4528B v.7
Modifications:	Type number HEF4528BP (SOT38-4) removed.			
HEF4528B v.7	20111122	Product data sheet	-	HEF4528B v.6
Modifications:	- Section Applications removed - Table 6: I_{OH} minimum values changed to maximum			
HEF4528B v.6	20091127	Product data sheet	-	HEF4528B v.5
HEF4528B v.5	20090813	Product data sheet	-	HEF4528B v.4
HEF4528B v.4	20090209	Product data sheet	-	HEF4528B_CNV v.3
HEF4528B_CNV v.3	19950101	Product specification	-	HEF4528B_CNV v.2
HEF4528B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 19 August 2024