

IR2110/IR2113

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +500V or +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

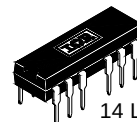
Product Summary

V_{OFFSET} (IR2110)	500V max.
(IR2113)	600V max.
$I_{\text{O+/-}}$	2A / 2A
V_{OUT}	10 - 20V
$t_{\text{on/off}}$ (typ.)	120 & 94 ns
Delay Matching	10 ns

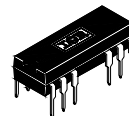
Packages



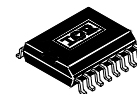
14 Lead PDIP
IR2110/IR2113



14 Lead PDIP
w/o Lead 4
IR2110-1/IR2113-1

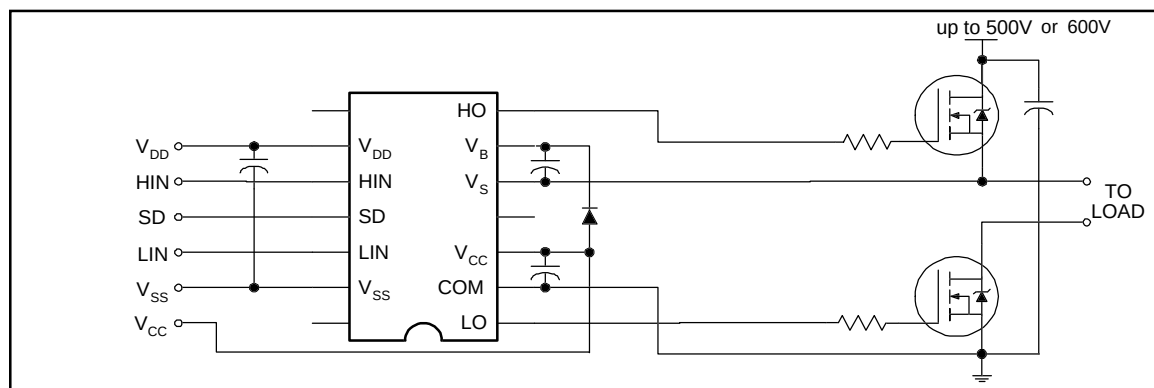


16 Lead PDIP
w/o leads 4 & 5
IR2110-2/IR2113-2



16 Lead SOIC
IR2110S/IR2113S

Typical Connection



IR2110/IR2113

Absolute Maximum Ratings

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Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage (IR2110)	-0.3	525	V
	(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{DD}	Logic supply voltage	-0.3	$V_{SS} + 25$	
V_{SS}	Logic supply offset voltage	$V_{CC} - 25$	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN, LIN & SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$ (14 lead DIP)	—	1.6	W
	(14 lead DIP w/o lead 4)	—	1.5	
	(16 lead DIP w/o leads 4 & 5)	—	1.6	
	(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient (14 lead DIP)	—	75	$^\circ\text{C/W}$
	(14 lead DIP w/o lead 4)	—	85	
	(16 lead DIP w/o leads 4 & 5)	—	75	
	(16Lead SOIC)	—	100	
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage (IR2110)	Note 1	500	
	(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	$V_{SS} + 4.5$	$V_{SS} + 20$	
V_{SS}	Logic supply offset voltage	-5	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	$^\circ\text{C}$
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	8	—	94	125		$V_S = 500V/600V$
t_{sd}	Shutdown propagation delay	9	—	110	140		$V_S = 500V/600V$
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off	—	—	—	10		Figure 5

Static Electrical Characteristics

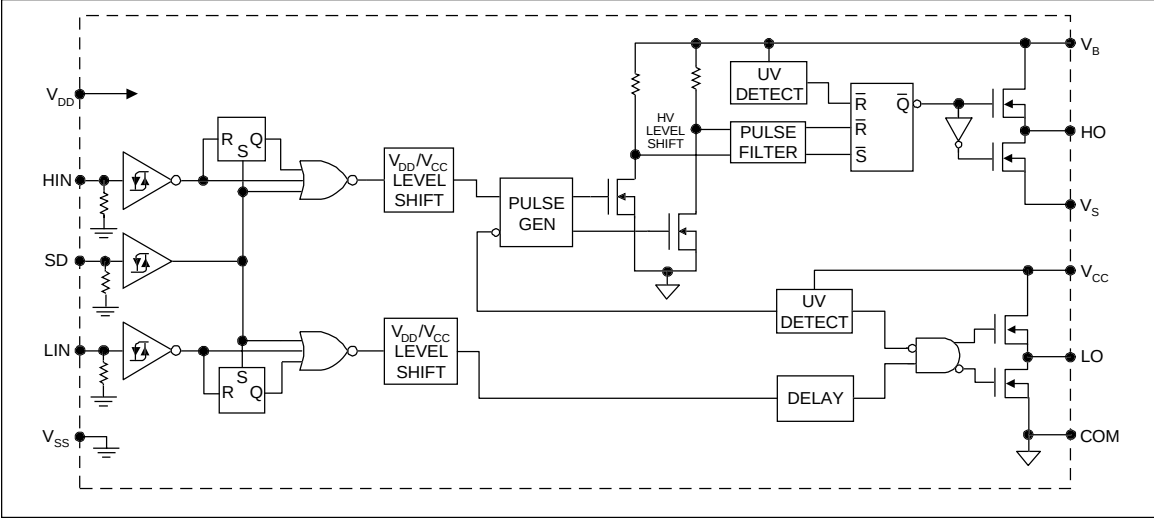
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	14	—	—	1.2		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		$I_O = 0A$
I_{LK}	Offset supply leakage current	16	—	—	50	μA	$V_B = V_S = 500V/600V$
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

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Functional Block Diagram



Lead Definitions

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

IR2110/IR2113	IR2110-1/IR2113-1	IR2110-2/IR2113-2	IR2110S/IR2113S
Part Number			

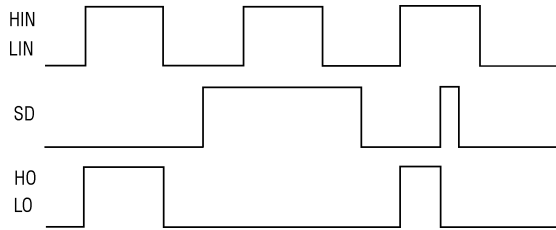


Figure 1. Input/Output Timing Diagram

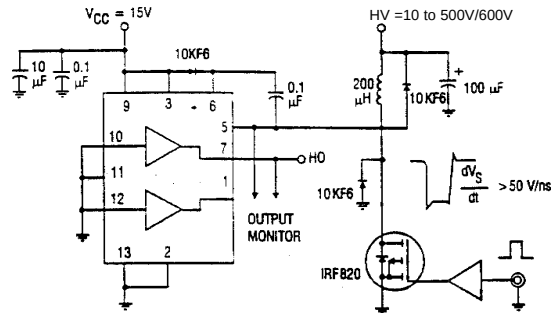


Figure 2. Floating Supply Voltage Transient Test Circuit

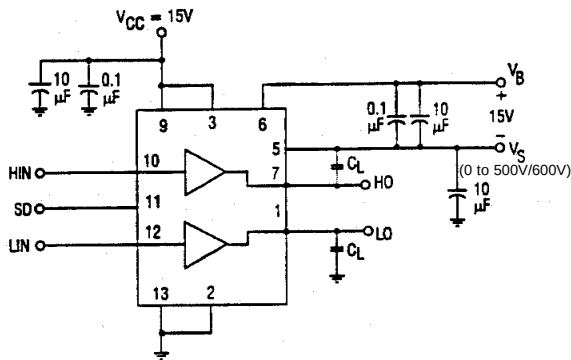


Figure 3. Switching Time Test Circuit

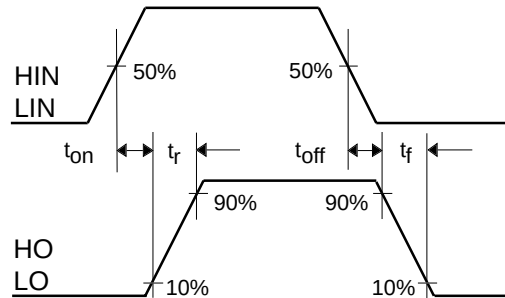


Figure 4. Switching Time Waveform Definition

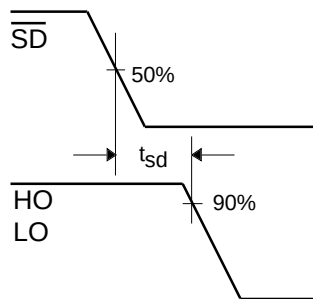


Figure 5. Shutdown Waveform Definitions

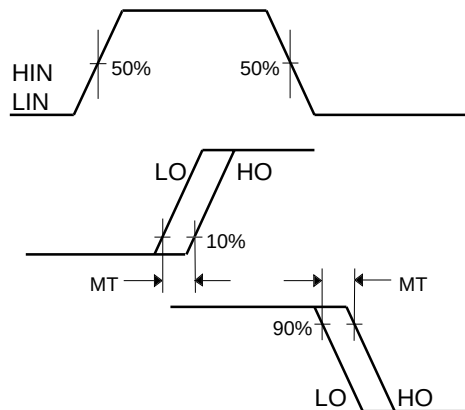


Figure 6. Delay Matching Waveform Definitions

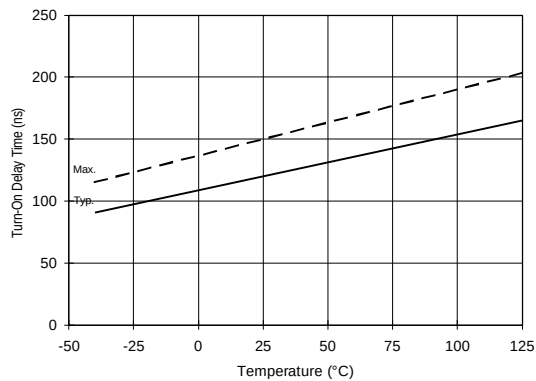


Figure 7A. Turn-On Time vs. Temperature

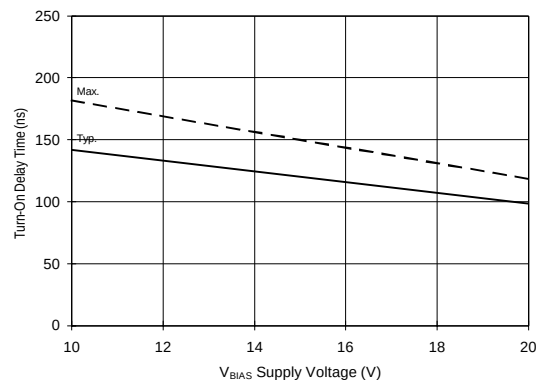


Figure 7B. Turn-On Time vs. Voltage

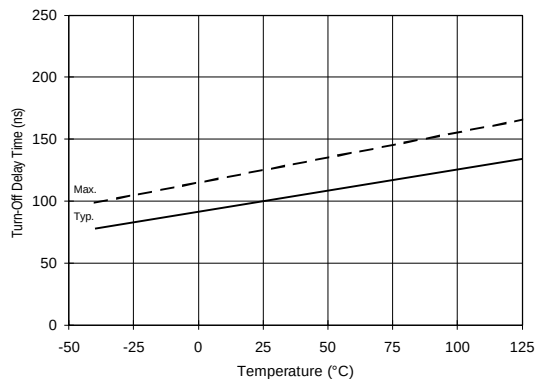


Figure 8A. Turn-Off Time vs. Temperature

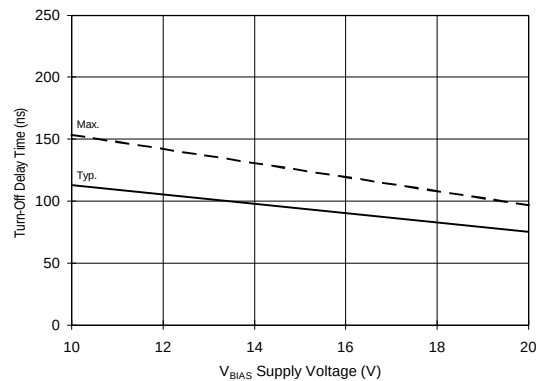


Figure 8B. Turn-Off Time vs. Voltage

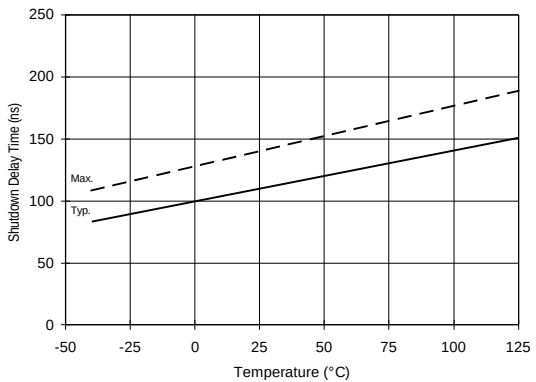


Figure 9A. Shutdown Time vs. Temperature

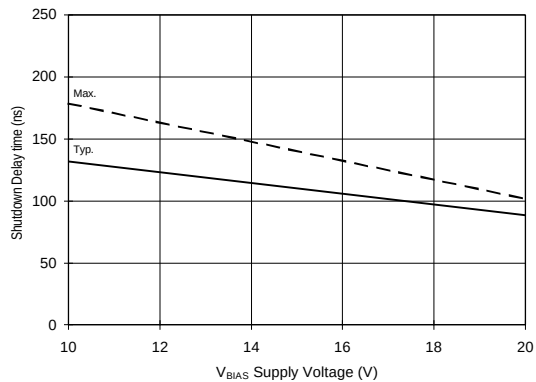


Figure 9B. Shutdown Time vs. Voltage

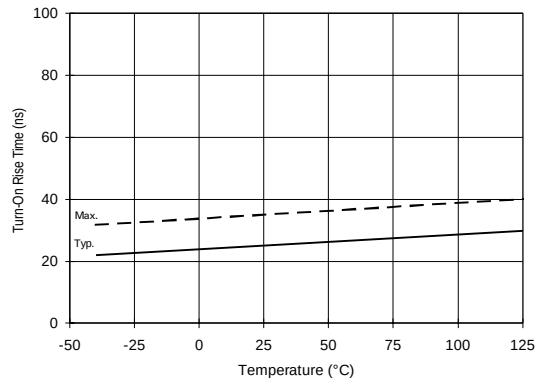


Figure 10A. Turn-On Rise Time vs. Temperature

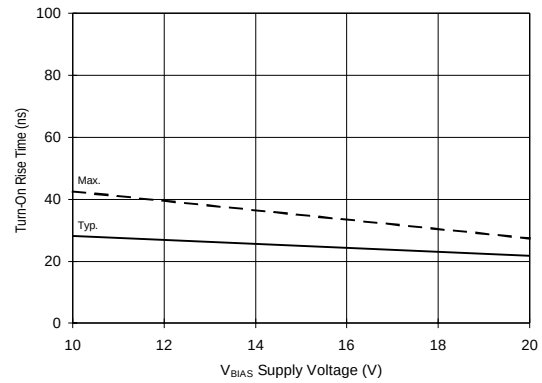


Figure 10B. Turn-On Rise Time vs. Voltage

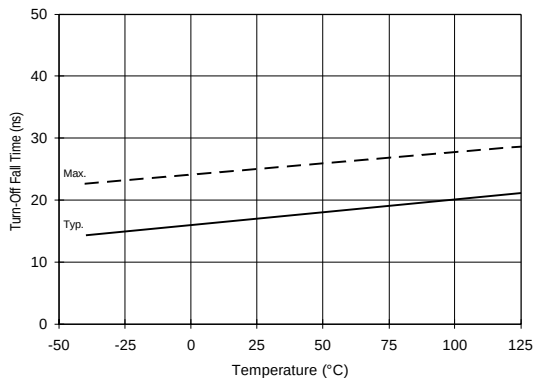


Figure 11A. Turn-Off Fall Time vs. Temperature

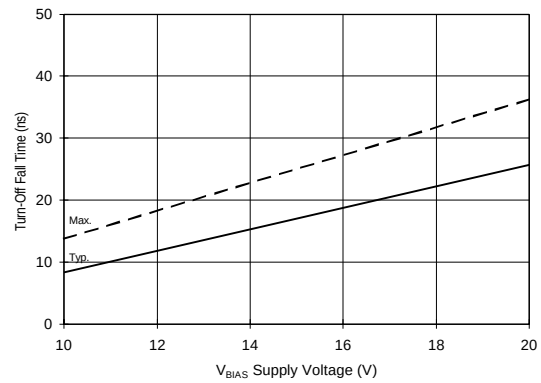


Figure 11B. Turn-Off Fall Time vs. Voltage

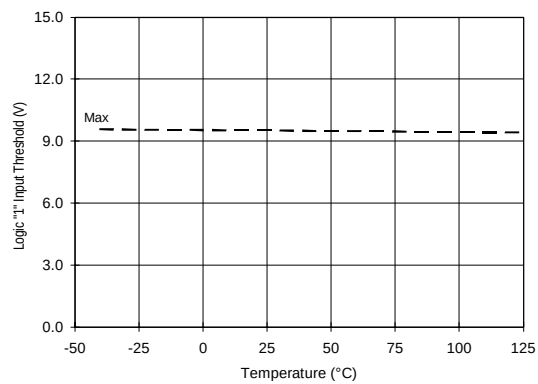


Figure 12A. Logic "1" Input Threshold vs. Temperature

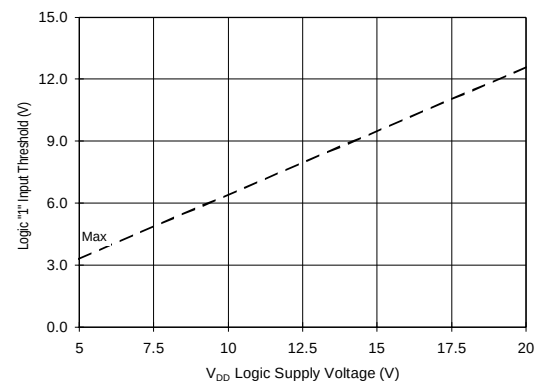


Figure 12B. Logic "1" Input Threshold vs. Voltage

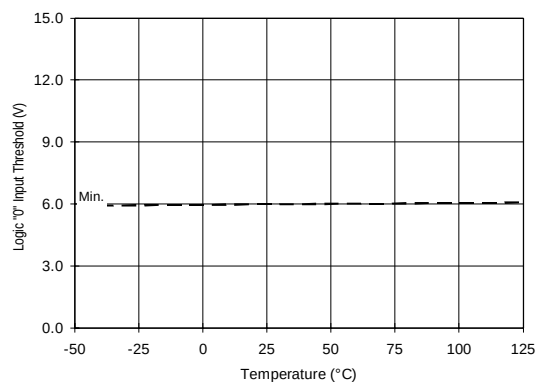


Figure 13A. Logic "0" Input Threshold vs. Temperature

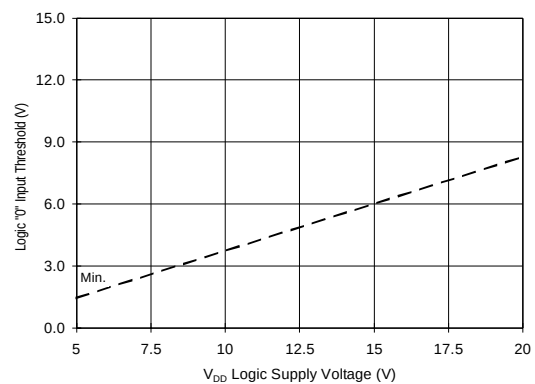


Figure 13B. Logic "0" Input Threshold vs. Voltage

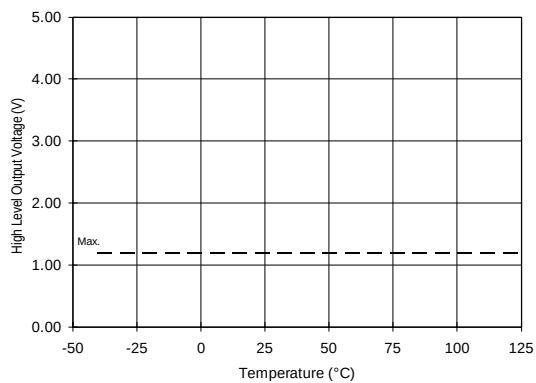


Figure 14A. High Level Output vs. Temperature

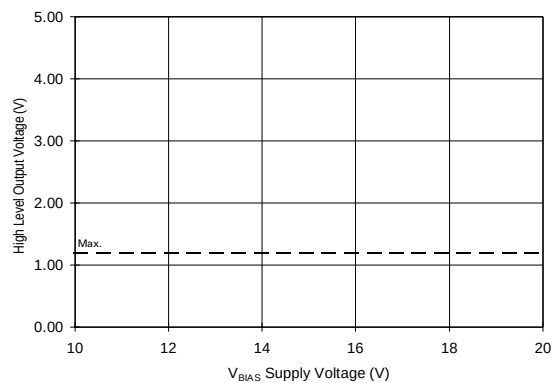


Figure 14B. High Level Output vs. Voltage

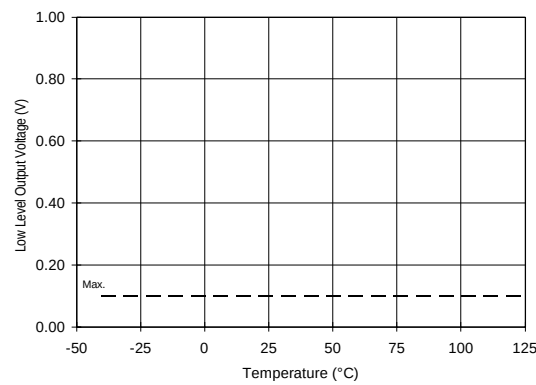


Figure 15A. Low Level Output vs. Temperature

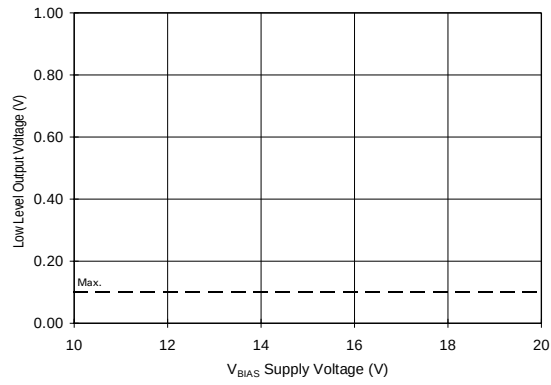


Figure 15B. Low Level Output vs. Voltage

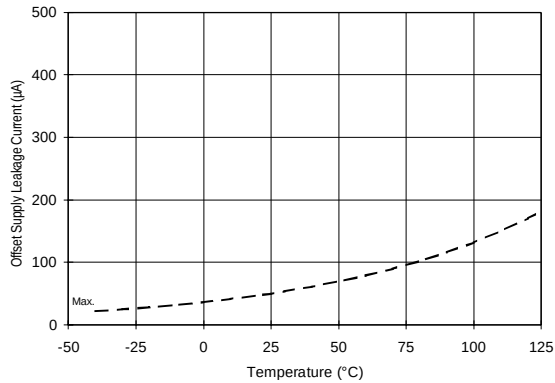


Figure 16A. Offset Supply Current vs. Temperature

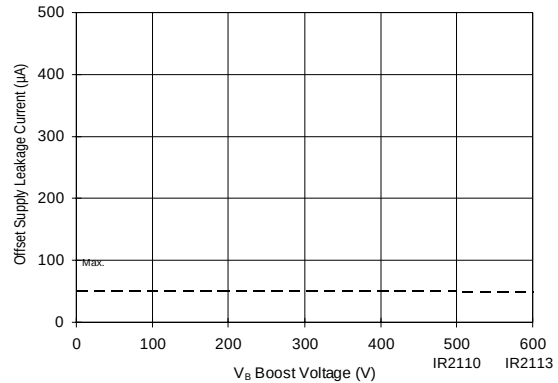


Figure 16B. Offset Supply Current vs. Voltage

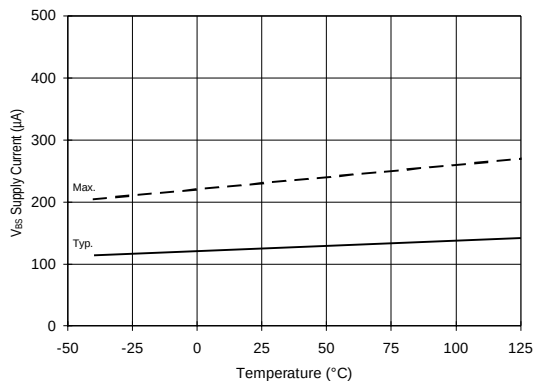


Figure 17A. V_{BS} Supply Current vs. Temperature

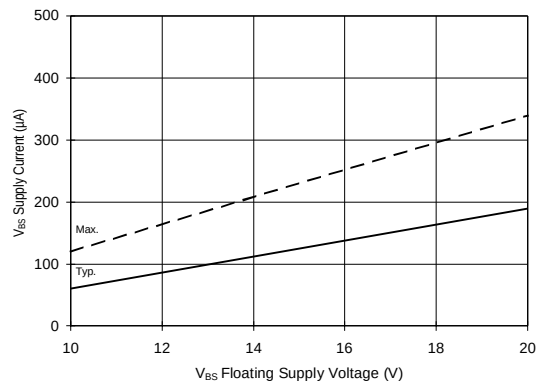


Figure 17B. V_{BS} Supply Current vs. Voltage

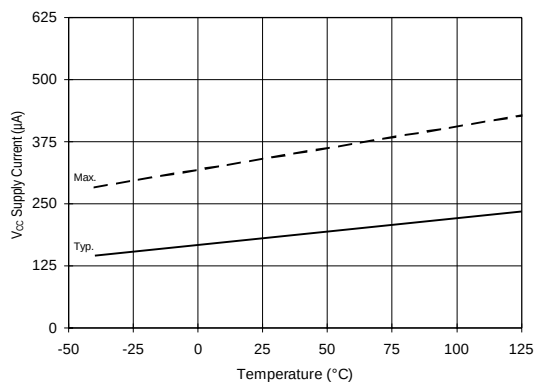


Figure 18A. V_{CC} Supply Current vs. Temperature

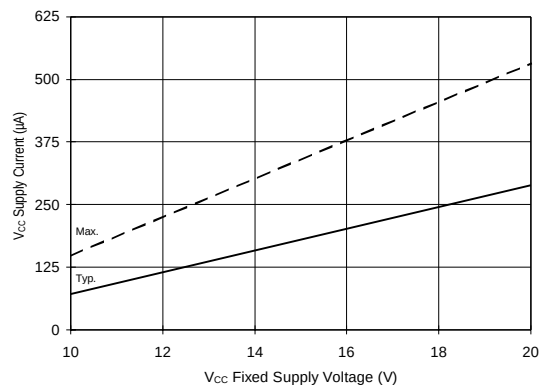


Figure 18B. V_{CC} Supply Current vs. Voltage

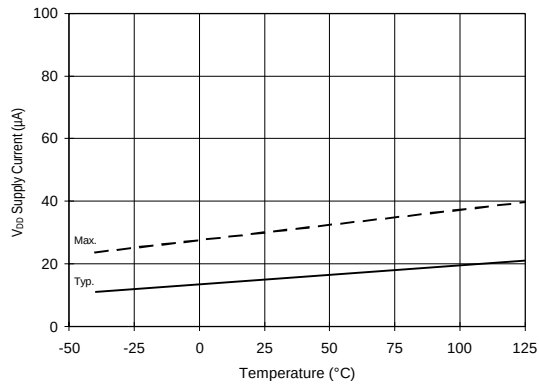


Figure 19A. V_{DD} Supply Current vs. Temperature

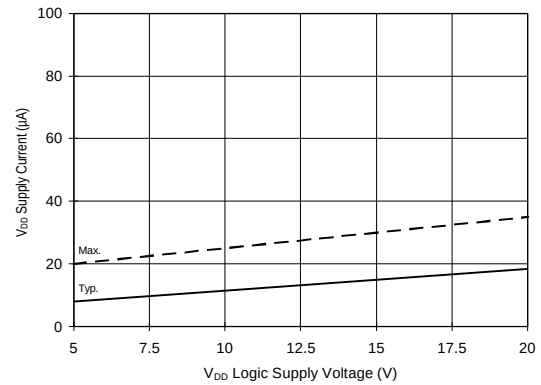


Figure 19B. V_{DD} Supply Current vs. Voltage

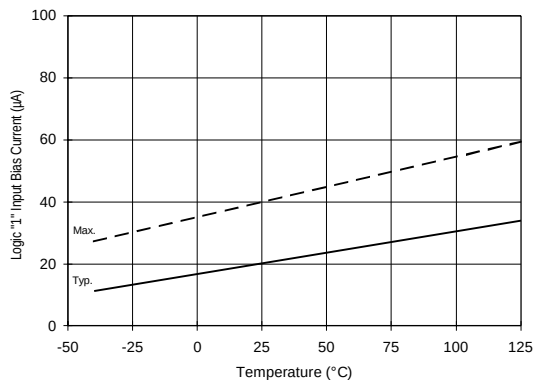


Figure 20A. Logic "1" Input Current vs. Temperature

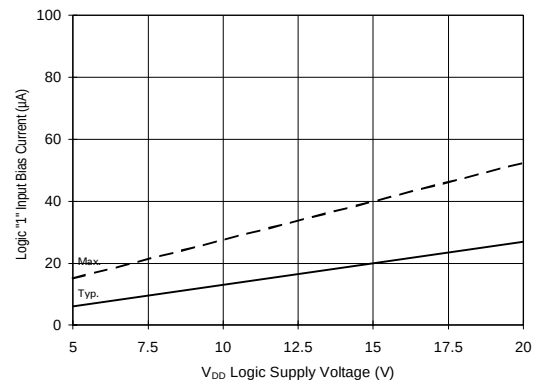


Figure 20B. Logic "1" Input Current vs. Voltage

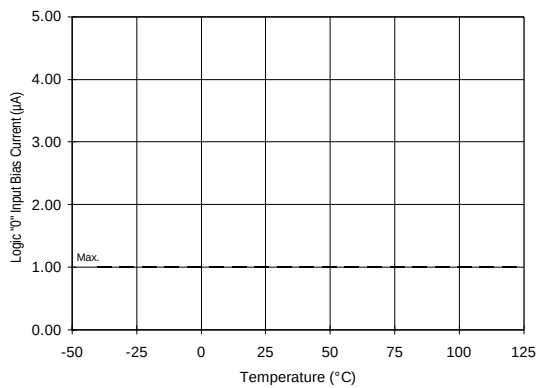


Figure 21A. Logic "0" Input Current vs. Temperature

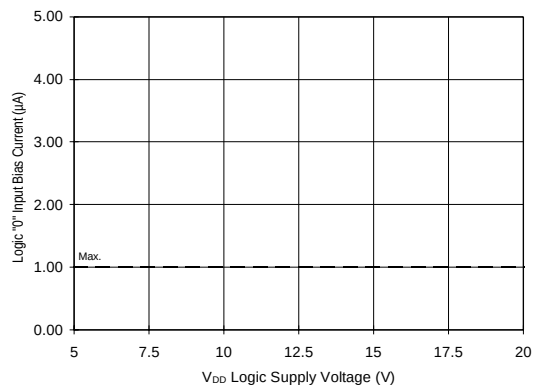


Figure 21B. Logic "0" Input Current vs. Voltage

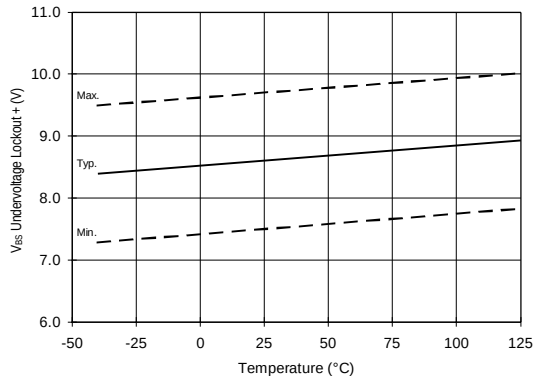


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

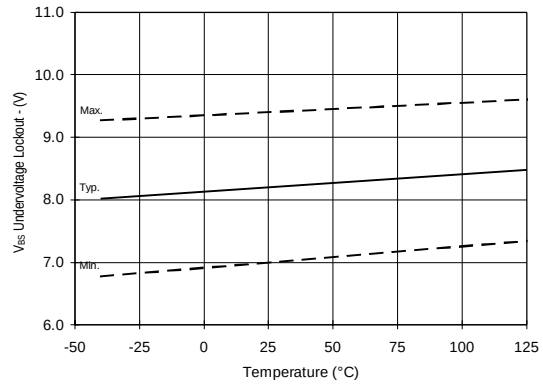


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

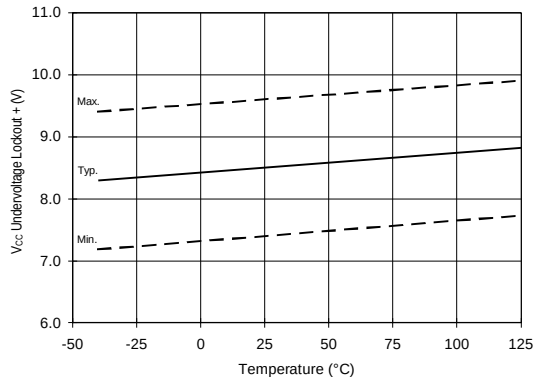


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

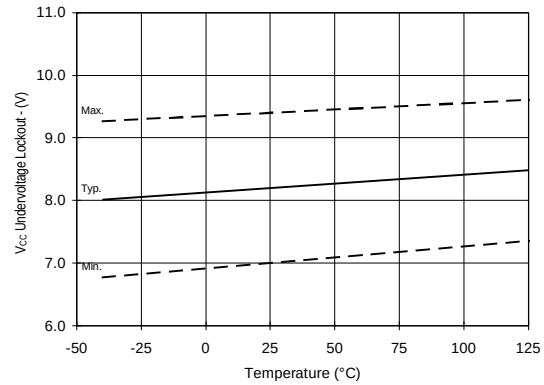


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

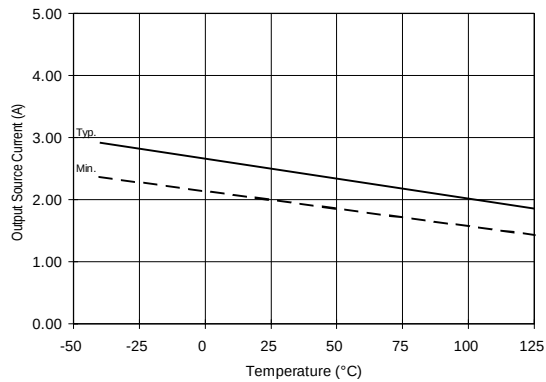


Figure 26A. Output Source Current vs. Temperature

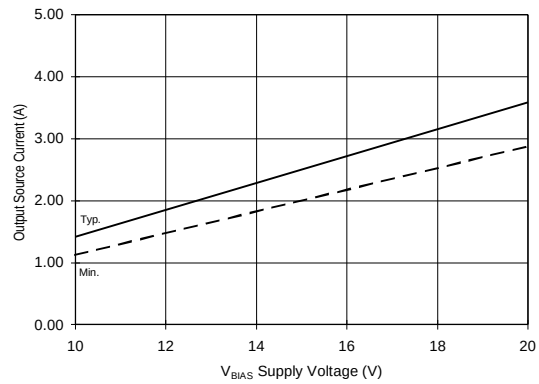


Figure 26B. Output Source Current vs. Voltage

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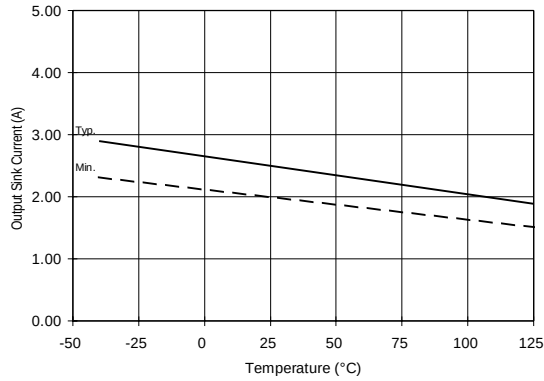


Figure 27A. Output Sink Current vs. Temperature

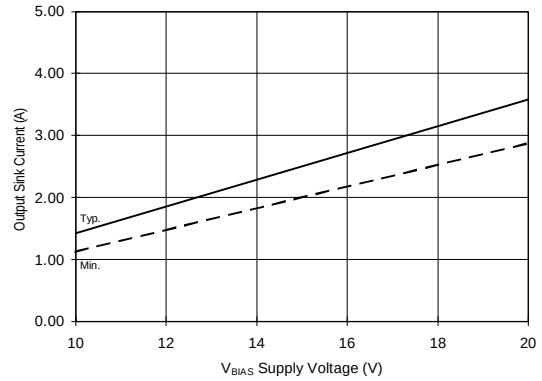


Figure 27B. Output Sink Current vs. Voltage

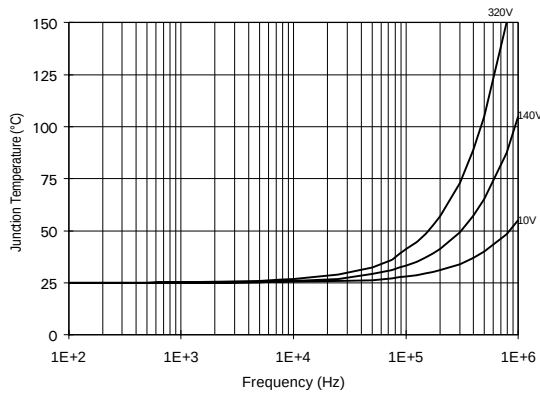


Figure 28. IR2110/IR2113 T_J vs. Frequency
(IRFBC20) $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

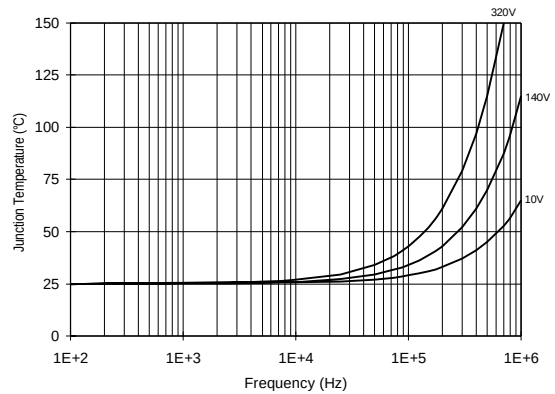


Figure 29. IR2110/IR2113 T_J vs. Frequency
(IRFBC30) $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

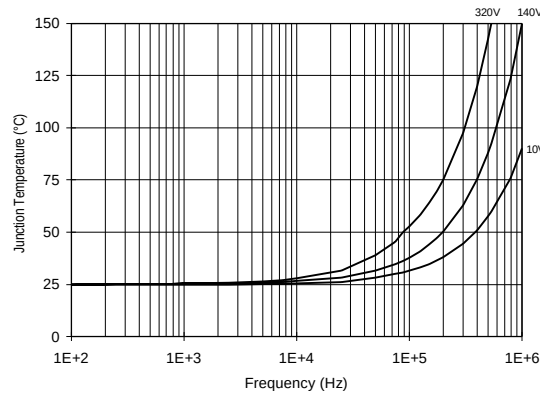


Figure 30. IR2110/IR2113 T_J vs. Frequency
(IRFBC40) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

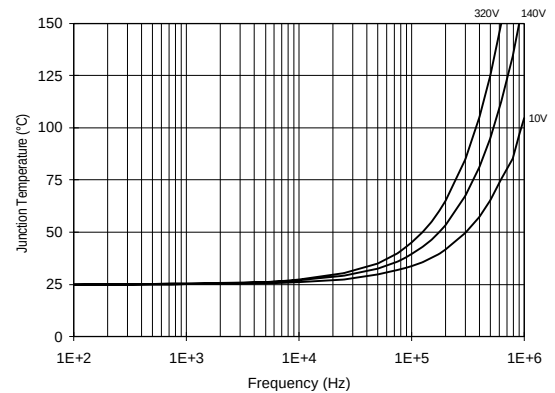


Figure 31. IR2110/IR2113 T_J vs. Frequency
(IRFPE50) $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

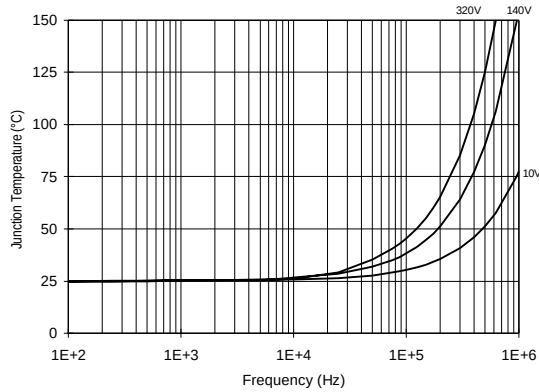


Figure 32. IR2110S/IR2113S T_J vs. Frequency (IRFBC20) $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

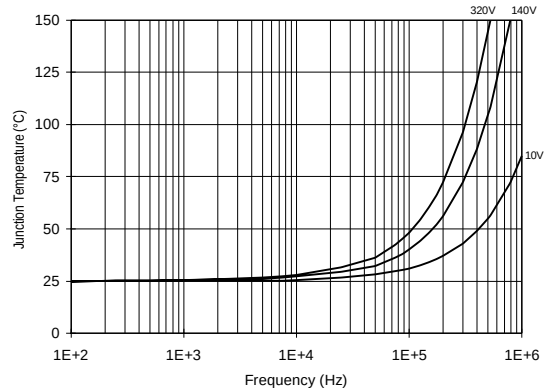


Figure 33. IR2110S/IR2113S T_J vs. Frequency (IRFBC30) $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

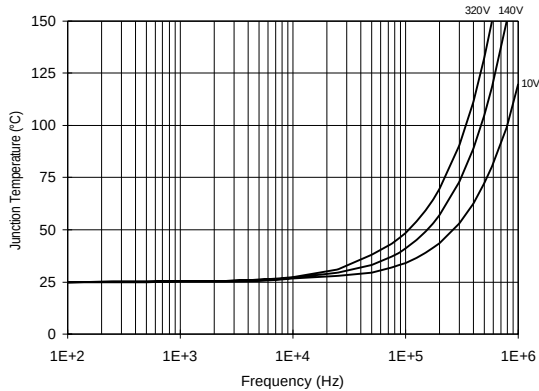


Figure 34. IR2110S/IR2113S T_J vs. Frequency (IRFBC40) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

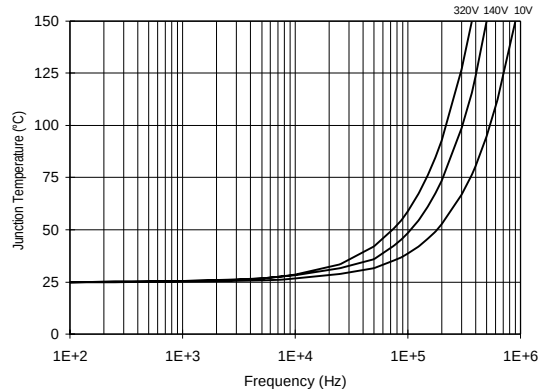


Figure 35. IR2110S/IR2113S T_J vs. Frequency (IRFPE50) $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

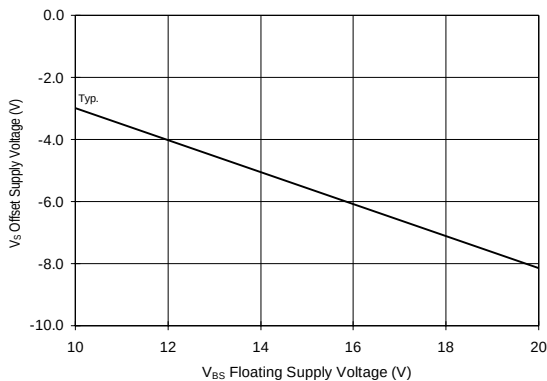


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

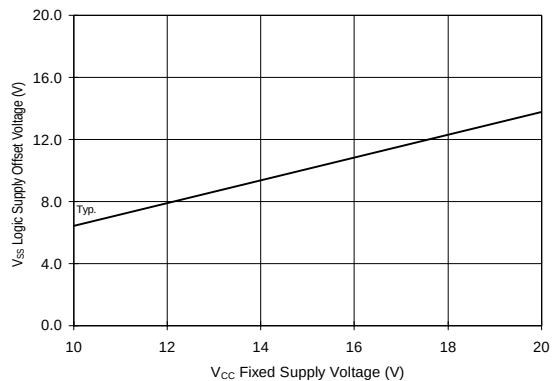


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

International
IOR Rectifier

Top View:

- Overall width: 20.19 [.795] / 18.42 [.725]
- Pin pitch: 1.77 [.070] / 1.15 [.045]
- Lead length: 14X
- Dimension A: -A-
- Dimension B: -B-
- Feature 6: Mold protusions

Side View:

- Maximum height: 5.33 [.210] MAX
- Minimum height: 0.39 [.015] MIN.
- Feature C: -C-

Lead Detail View:

- Lead thickness: 0.356 [.014]
- Lead width: 0.558 [.022]
- Lead angle: 14X 0° - 15°
- Lead length: 14X
- Feature D: 0.25 [.010]
- Feature E: 0.381 [.015] / 0.204 [.008]
- Feature F: 7.62 [.300]
- Feature G: 2.54 [.100]
- Feature H: 12X
- Feature I: 4.06 [.160] / 2.93 [.115]
- Feature J: 14
- Feature K: 1

NOTES:

- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
- MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

14 Lead PDIP

01-3002 03

Technical drawing of a 14 Lead PDIP w/o Lead 4 package. The drawing includes a top view, a side view, and a detail view of the lead profile.

Top View Dimensions:

- Overall width: 20.19 [.795] mm, 18.42 [.725] mm
- Lead pitch: 1.77 [.070] mm, 1.15 [.045] mm
- Lead width: 5.08 [.200] mm
- Lead height: 7.11 [.280] mm, 6.10 [.240] mm
- Lead spacing: 5.33 [.210] mm (MAX)
- Lead angle: 13°
- Lead thickness: 0.558 [.022] mm, 0.356 [.014] mm
- Lead width at base: 2.54 [.100] mm (10X)
- Lead thickness at base: 0.25 [.010] mm (M), 0.25 [.010] mm (C), 0.25 [.010] mm (B), 0.25 [.010] mm (S), 0.25 [.010] mm (A), 0.25 [.010] mm (S)

Side View Dimensions:

- Lead height: 5.33 [.210] mm (MAX)
- Lead width: 5.08 [.200] mm
- Lead thickness: 0.558 [.022] mm, 0.356 [.014] mm
- Lead angle: 13°
- Lead thickness at base: 0.25 [.010] mm (M), 0.25 [.010] mm (C), 0.25 [.010] mm (B), 0.25 [.010] mm (S), 0.25 [.010] mm (A), 0.25 [.010] mm (S)

Detail View Dimensions:

- Lead height: 5.33 [.210] mm (MAX)
- Lead width: 5.08 [.200] mm
- Lead thickness: 0.558 [.022] mm, 0.356 [.014] mm
- Lead angle: 13°
- Lead thickness at base: 0.25 [.010] mm (M), 0.25 [.010] mm (C), 0.25 [.010] mm (B), 0.25 [.010] mm (S), 0.25 [.010] mm (A), 0.25 [.010] mm (S)

Notes:

- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
- MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

