P-Channel NexFET™ Power MOSFET

Check for Samples: CSD75301W1015

FEATURES

- **Dual P-Ch MOSFETs**
- **Common Source Configuration**
- **Small Footprint 1mm × 1.5mm**
- **Low Profile – 0.62mm**
- **Ultra Low Qg and Qgd**
- **Pb Free / RoHS Compliant**
- **Halogen Free**

APPLICATIONS

- **Battery Management**
- **Load Switch**
- **Battery Protection**

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View

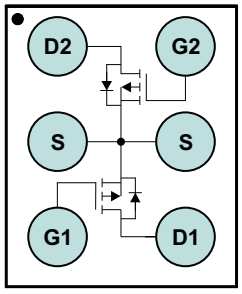


Table 1. PRODUCT SUMMARY

(Per MOSFET unless otherwise stated)				
V_{DS}	Drain to Source Voltage	–20		V
Q_g	Gate Charge Total (4.5V)	1.5		nC
Q_{gd}	Gate Charge Gate to Drain	0.3		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.8V	150	mΩ
		V_{GS} = –2.5V	105	mΩ
		V_{GS} = –4.5V	80	mΩ
$V_{GS(th)}$	Voltage threshold	–0.7		V

ORDERING INFORMATION

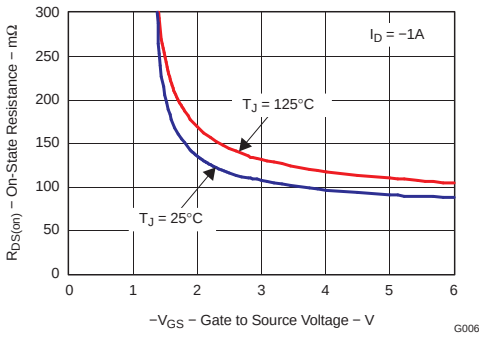
Device	Package	Media	Qty	Ship
CSD75301W1015	1 × 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

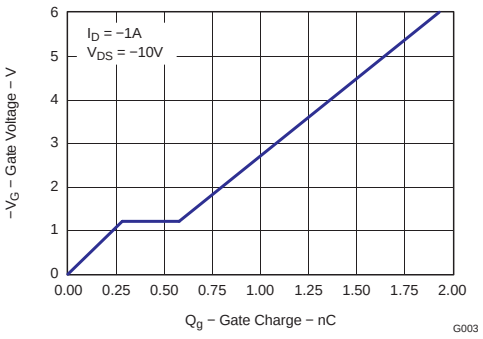
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Continuous Drain Current, T_C = 25°C(1) (2)	–1.2	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(1) (2) (3)	–17.5	A
P_D	Power Dissipation(1) (2)	0.8	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Per device, both devices in conduction.
(2) $R_{\theta JA}$ = 74°C/W on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.
(3) Pulse width ≤300µs, duty cycle ≤2%

$R_{DS(ON)}$ vs V_{GS}



Gate Charge



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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated) (Per MOSFET unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = –250µA	–20			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = –16V			–1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = –8V			–100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250µA	–0.4	–0.7	–1.0	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.8V, I_D = –1A		150	190	mΩ
		V_{GS} = –2.5V, I_D = –1A		105	135	mΩ
		V_{GS} = –4.5V, I_D = –1A		80	100	mΩ
g_{fs}	Transconductance	V_{DS} = –10V, I_D = –1A		5.2		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = –10V, f = 1MHz		150	195	pF
C_{OSS}	Output Capacitance			67	87	pF
C_{RSS}	Reverse Transfer Capacitance			24	31	pF
Q_g	Gate Charge Total (–4.5V)	V_{DS} = –10V, I_D = –1A		1.5	2.1	nC
Q_{gd}	Gate Charge Gate to Drain			0.3		nC
Q_{gs}	Gate Charge Gate to Source			0.28		nC
$Q_{g(th)}$	Gate Charge at Vth			0.12		nC
Q_{OSS}	Output Charge	V_{DS} = –9.5V, V_{GS} = 0V		1.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10V, V_{GS} = –4.5V, I_D = –1A, R_G = 30Ω		3		ns
t_r	Rise Time			1.7		ns
$t_{d(off)}$	Turn Off Delay Time			38		ns
t_f	Fall Time			16		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = –1A, V_{GS} = 0V		–0.81	–1	V
Q_{rr}	Reverse Recovery Charge	V_{dd} = –9.5V, I_F = –1A, di/dt = 200A/µs		2		nC
t_{rr}	Reverse Recovery Time	V_{dd} = –9.5V, I_F = –1A, di/dt = 200A/µs		7.5		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Ambient(1) (2)			136	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(2) (3)			93	°C/W

(1) Device mounted on FR4 material with Minimum Cu mounting area.
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1in^2 of 2 oz Cu.

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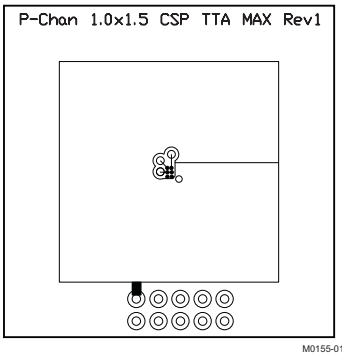
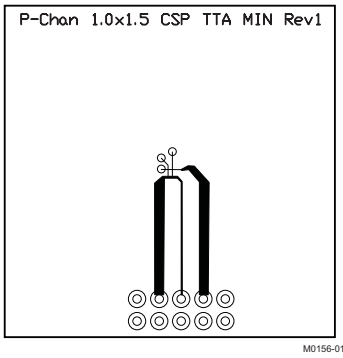


Max $R_{\theta JA}$ = 93°C/W when mounted on 1inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 136°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

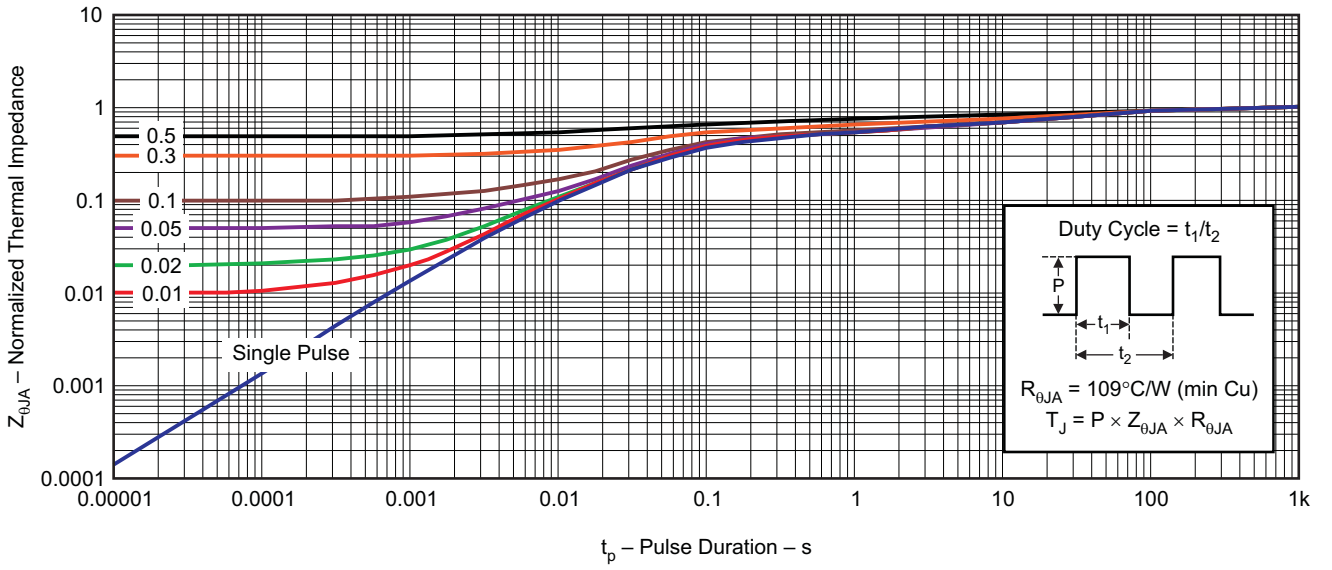


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

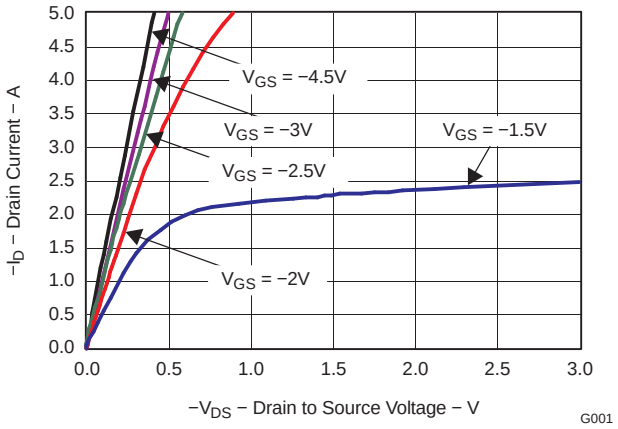


Figure 2. Saturation Characteristics

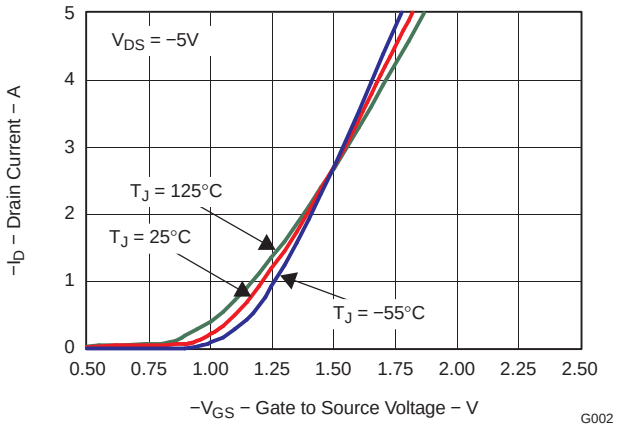


Figure 3. Transfer Characteristics

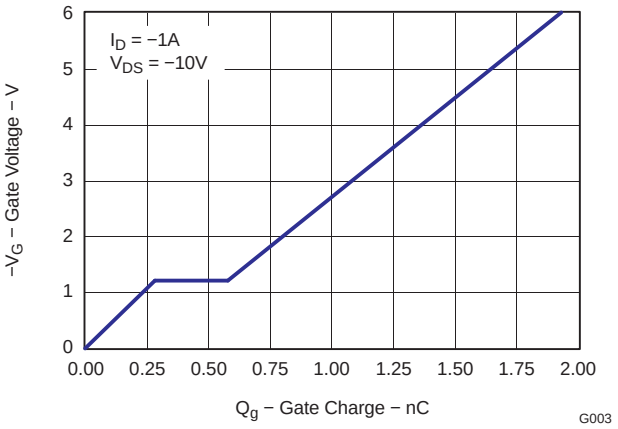


Figure 4. Gate Charge

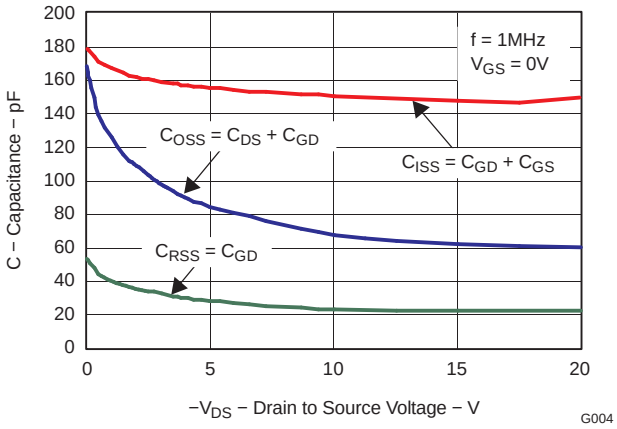


Figure 5. Capacitance

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

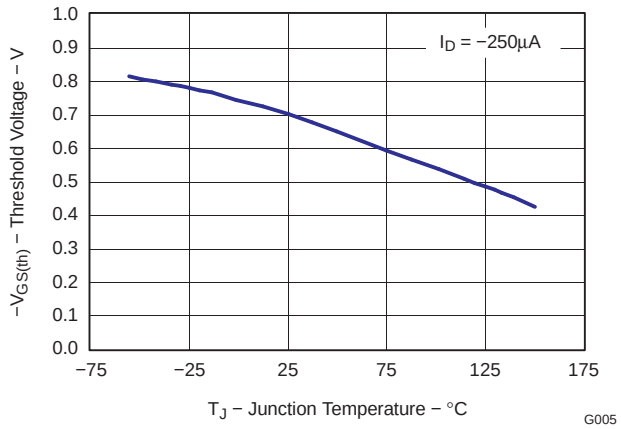

Figure 6. Threshold Voltage vs. Temperature

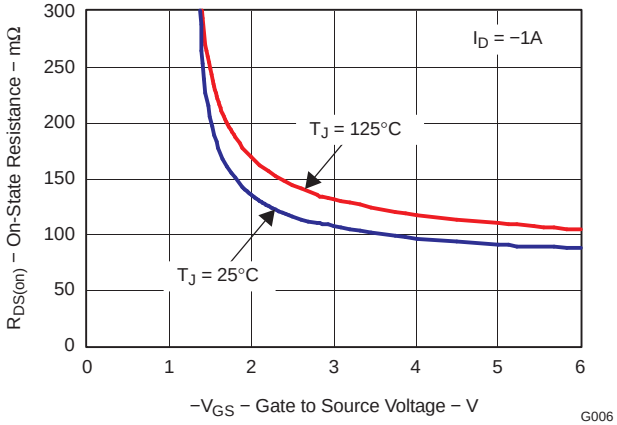

Figure 7. On Resistance vs. Gate Voltage

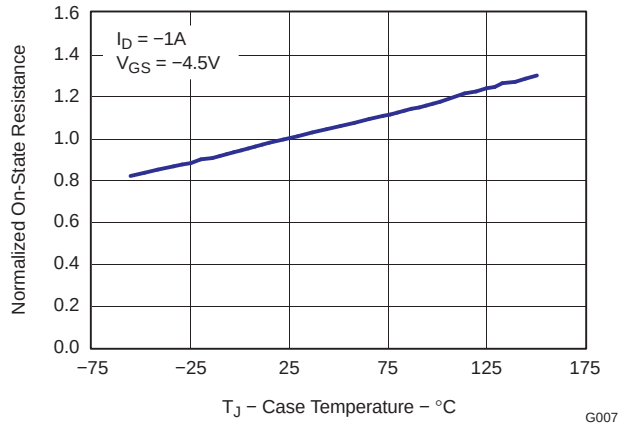

Figure 8. On Resistance vs. Temperature

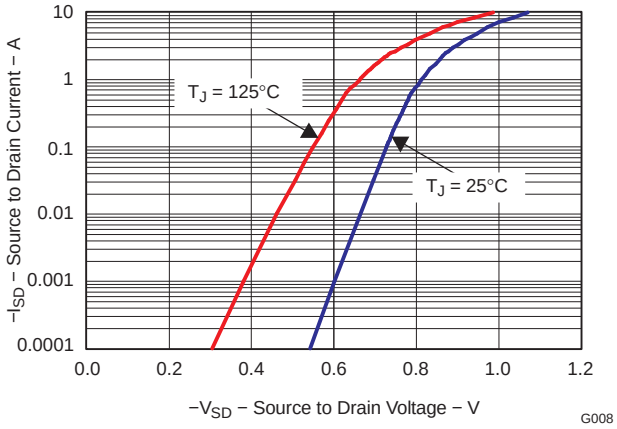

Figure 9. Typical Diode Forward Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

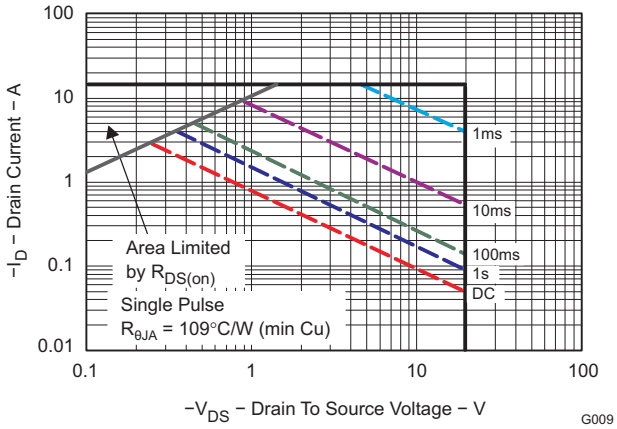

Figure 10. Maximum Safe Operating Area

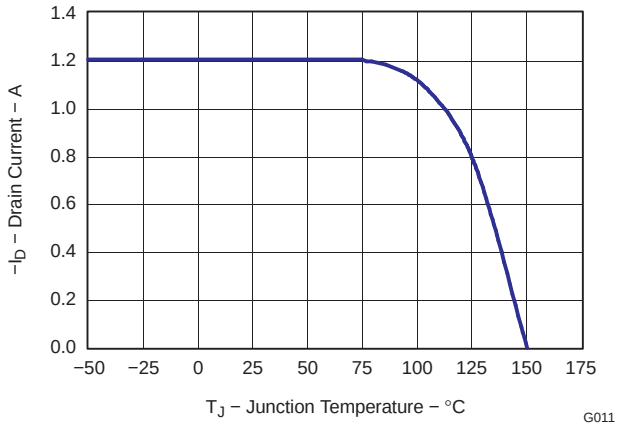

Figure 11. Maximum Drain Current vs. Temperature

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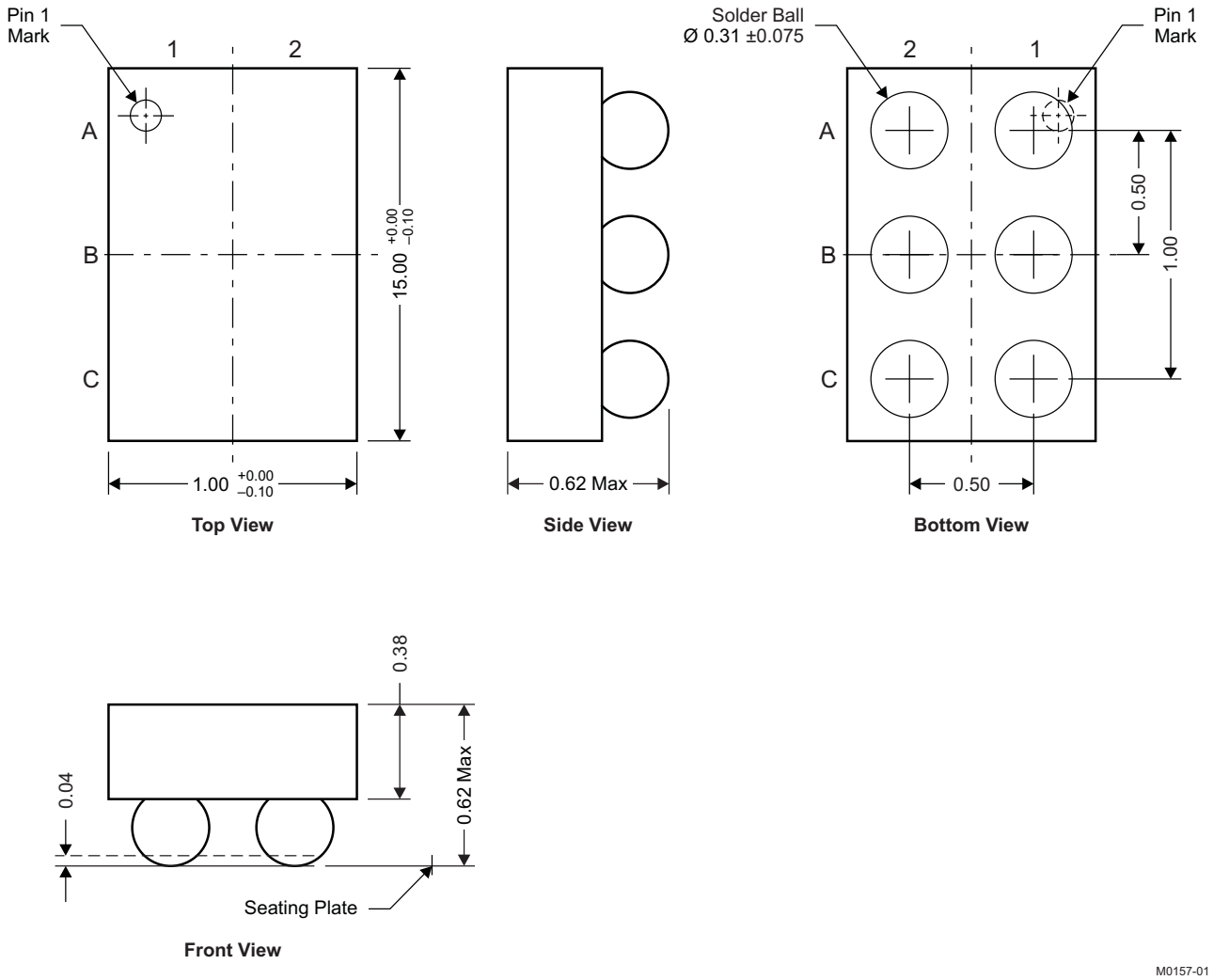
MECHANICAL DATA

CSD75301W1015 Package Dimensions

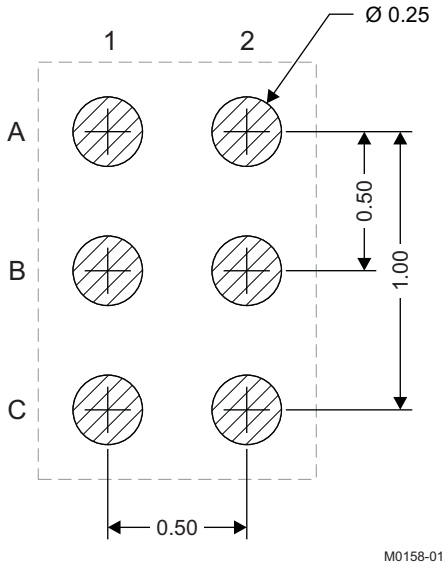


NOTE: All dimensions are in mm (unless othersse specified)

Pinout

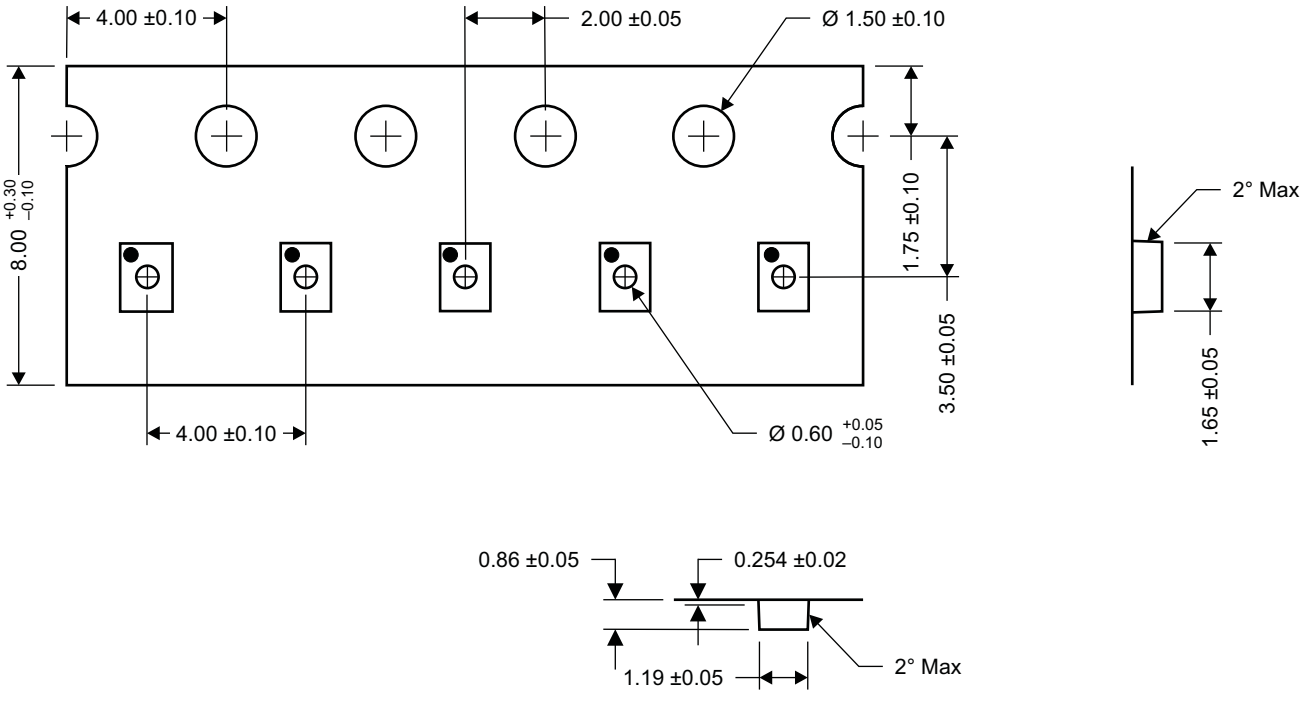
POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless othersse specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless othersse specified)

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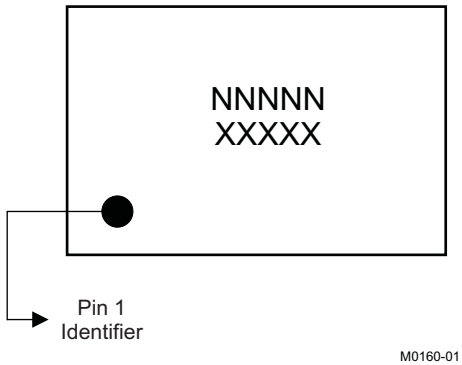
Package Marking Information

Location	
1st Line	
Product Code	= NNNNN, First 5 digits after CSD (Fixed Text)
2nd Line	
XXXXX	= Last 5 digits of lot number



REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• Changed location of the Pin 1 indicator dot in the pin out illustration.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CSD75301W1015	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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