CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING
6 FUNCTIONAL DESCRIPTION
6.1 Functional modes
6.2 Control
6.2.1 Control signals
6.2.2 Clock
6.2.3 Error condition
6.3 System I/O interfaces
6.3.1 Video data input signals
6.3.2 Video data output signals
6.3.3 Auxiliary data
6.4 System block description
6.4.1 Input formatter with filter
6.4.2 Conversion matrix
6.4.3 Video look-up table and output stage
6.4.4 I²C-bus receiver
7 OPERATING CONDITIONS
7.1 Electrical conditions
7.1.1 Start-up condition
7.1.2 Operating time
7.1.3 Temperature range
7.1.4 Backup
7.1.5 Power-down mode
7.1.6 Handling
8 LIMITING VALUES
9 DC CHARACTERISTICS
10 TIMING CHARACTERISTICS
11 PACKAGE OUTLINE
12 SOLDERING
12.1 Introduction
12.2 Reflow soldering
12.3 Wave soldering
12.4 Repairing soldered joints
13 DEFINITIONS
14 LIFE SUPPORT APPLICATIONS
15 PURCHASE OF PHILIPS I²C COMPONENTS

Digital Colour Space Converter (DCSC)

SAA7192A

1 FEATURES

- Input formatter with:
  - multiplexer
  - Y-delay line
  - Cr and Cb interpolating filters
- Conversion matrix (according to CCIR 601)
- Video look-up tables (provide gamma correction)
- Pipeline delay line (horizontal reference signal)
- I²C-bus interface
- All functional blocks are bypassable.

2 GENERAL DESCRIPTION

The Digital Colour Space Converter (DCSC) is a digital matrix which is used to transform 16/24-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 24-bit format in accordance with the *"CCIR-601 recommendations"*.

Accepting inputs from the different formats of the MPC-E decoder family, the device has a constant propagation delay and a maximum data rate of 16 MHz. A matched pipeline delay line is available to permit the HREF signal to be synchronized with the video data at the output.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7192AWP	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

4 BLOCK DIAGRAM

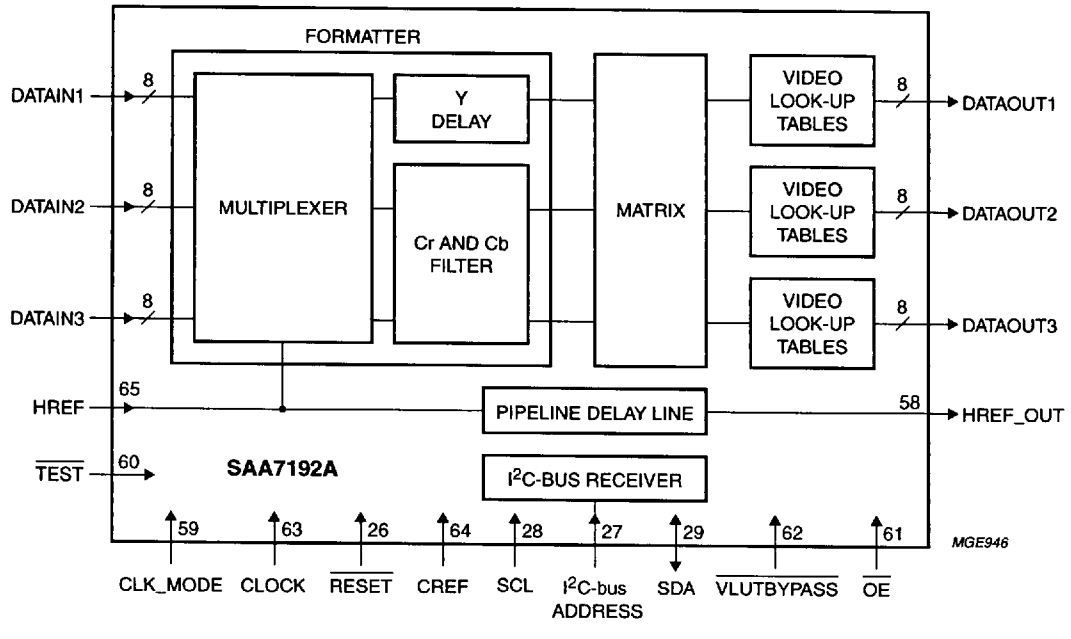


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DATAIN21	1	I	colour difference signal Cr1
DATAIN22	2	I	colour difference signal Cr2
DATAIN23	3	I	colour difference signal Cr3
DATAIN24	4	I	colour difference signal Cr4
DATAIN25	5	I	colour difference signal Cr5
DATAIN26	6	I	colour difference signal Cr6
DATAIN27	7	I	colour difference signal Cr7
DATAIN30	8	I	colour difference signal Cb0 or multiplexed Cb and Cr
DATAIN31	9	I	colour difference signal Cb1 or multiplexed Cb and Cr
DATAIN32	10	I	colour difference signal Cb2 or multiplexed Cb and Cr
DATAIN33	11	I	colour difference signal Cb3 or multiplexed Cb and Cr
DATAIN34	12	I	colour difference signal Cb4 or multiplexed Cb and Cr
DATAIN35	13	I	colour difference signal Cb5 or multiplexed Cb and Cr
DATAIN36	14	I	colour difference signal Cb6 or multiplexed Cb and Cr
DATAIN37	15	I	colour difference signal Cb7 or multiplexed Cb and Cr
DATAIN10	16	I	luminance signal Y0
DATAIN11	17	I	luminance signal Y1
V_{DD}	18	–	positive supply, voltage core (+5 V)
V_{SS}	19	–	negative supply, voltage core (ground)
DATAIN12	20	I	luminance signal Y2
DATAIN13	21	I	luminance signal Y3
DATAIN14	22	I	luminance signal Y4
DATAIN15	23	I	luminance signal Y5
DATAIN16	24	I	luminance signal Y6
DATAIN17	25	I	luminance signal Y7
$\overline{\text{RESET}}$	26	I	initially resets the functions
I²C-bus ADDRESS	27	I	I²C-bus slave address selection
SCL	28	I	I²C-bus serial clock
SDA	29	I/O	I²C-bus serial data
DATAOUT10	30	O	RED0
DATAOUT11	31	O	RED1
DATAOUT12	32	O	RED2
DATAOUT13	33	O	RED3
DATAOUT14	34	O	RED4

SYMBOL	PIN	I/O	DESCRIPTION
V_{DD}	35	–	positive supply voltage, output stages (+5 V)
V_{SS}	36	–	negative supply, output stages
DATAOUT15	37	O	RED5
DATAOUT16	38	O	RED6
DATAOUT17	39	O	RED7
DATAOUT20	40	O	GREEN0
DATAOUT21	41	O	GREEN1
DATAOUT22	42	O	GREEN2
DATAOUT23	43	O	GREEN3
DATAOUT24	44	O	GREEN4
DATAOUT25	45	O	GREEN5
DATAOUT26	46	O	GREEN6
DATAOUT27	47	O	GREEN7
DATAOUT30	48	O	BLUE0
DATAOUT31	49	O	BLUE1
DATAOUT32	50	O	BLUE2
V_{DD}	51	–	positive supply voltage, output stages (+5 V)
V_{SS}	52	–	negative supply, output stages
DATAOUT33	53	O	BLUE3
DATAOUT34	54	O	BLUE4
DATAOUT35	55	O	BLUE5
DATAOUT36	56	O	BLUE6
DATAOUT37	57	O	BLUE7
HREF_OUT	58	O	delayed horizontal reference signal
CLK_MODE	59	I	16 MHz or DMSD clock mode selection
$\overline{TEST}$	60	I	test mode, active LOW, usually not connected
$\overline{OE}$	61	I	output enable (fast switch)
$\overline{VLUTBYPASS}$	62	I	fast switch to operate the VLUTs in bypass
CLOCK	63	I	system clock
CREF	64	I	clock reference signal (DMSD mode)
HREF	65	I	horizontal reference signal
DATAIN20	66	I	colour difference signal Cr0
V_{DD}	67	–	positive supply, voltage core (+5 V)
V_{SS}	68	–	negative supply, voltage core (ground)

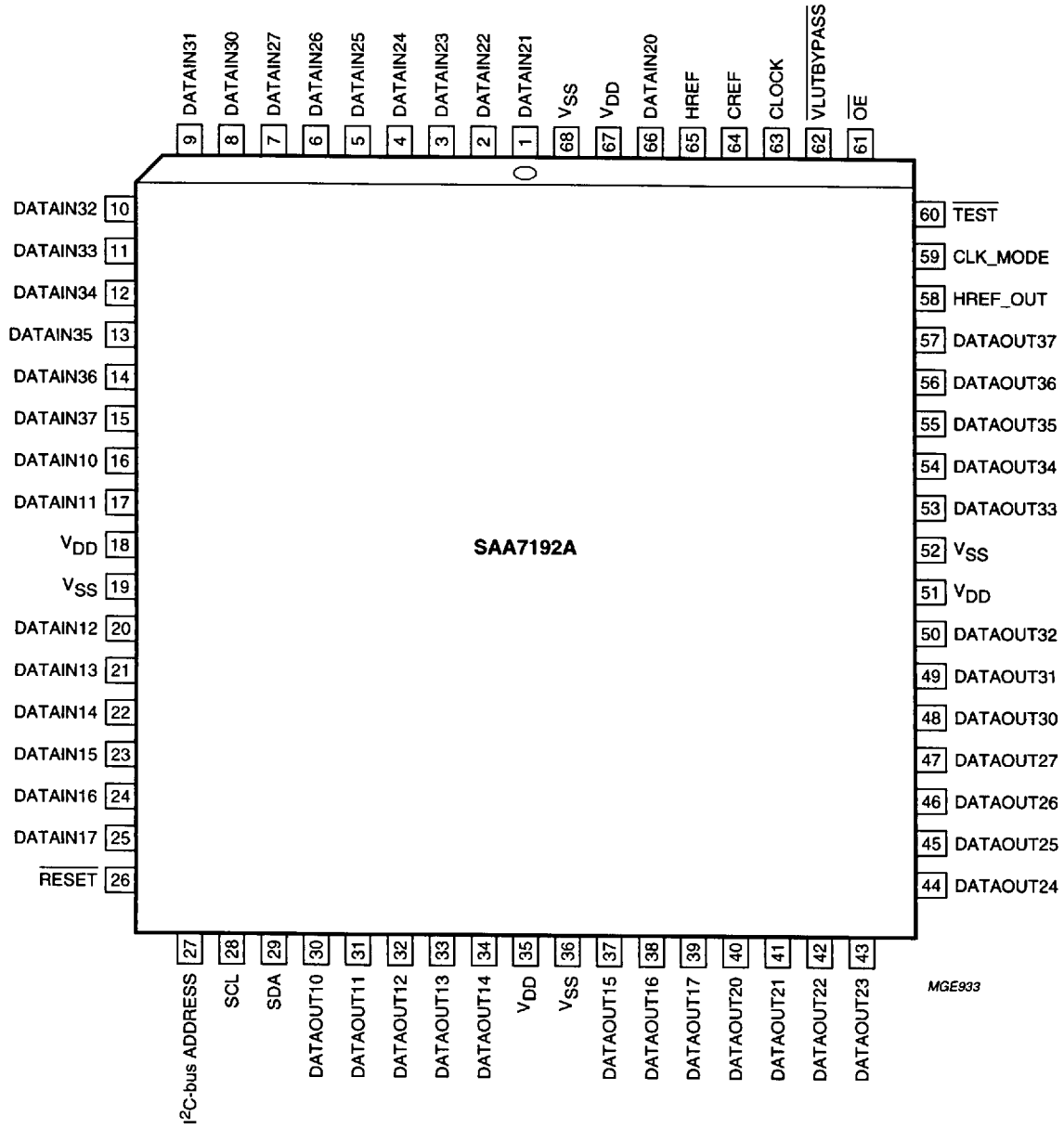


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Functional modes

Table 1 Functional modes (note 1)

MODE	FUNCTION
1	4 : 1 : 1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4 : 1 : 1 filter, matrix, no VLUT; DATAOUT = RGB
3	4 : 1 : 1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4 : 1 : 1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4 : 2 : 2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4 : 2 : 2 filter, matrix, no VLUT; DATAOUT = RGB
7	4 : 2 : 2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4 : 2 : 2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT = DATAIN 'Process Bypass'
10	no filter, matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT
12	no filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

Note

1. Figures 3 to 10 illustrate the functional modes.

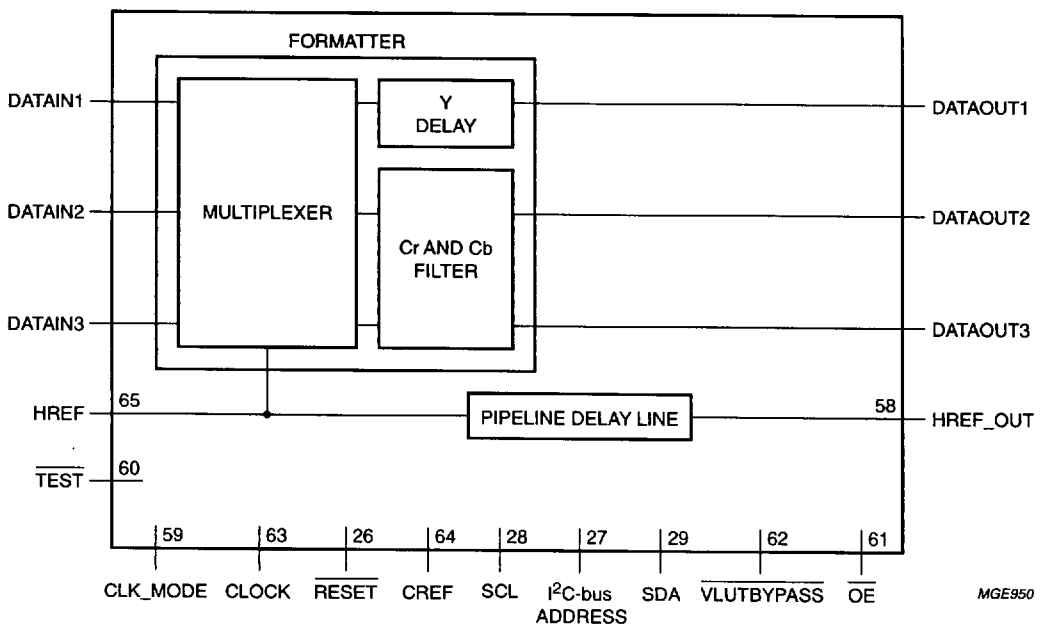


Fig.3 Functional modes 1 and 5.

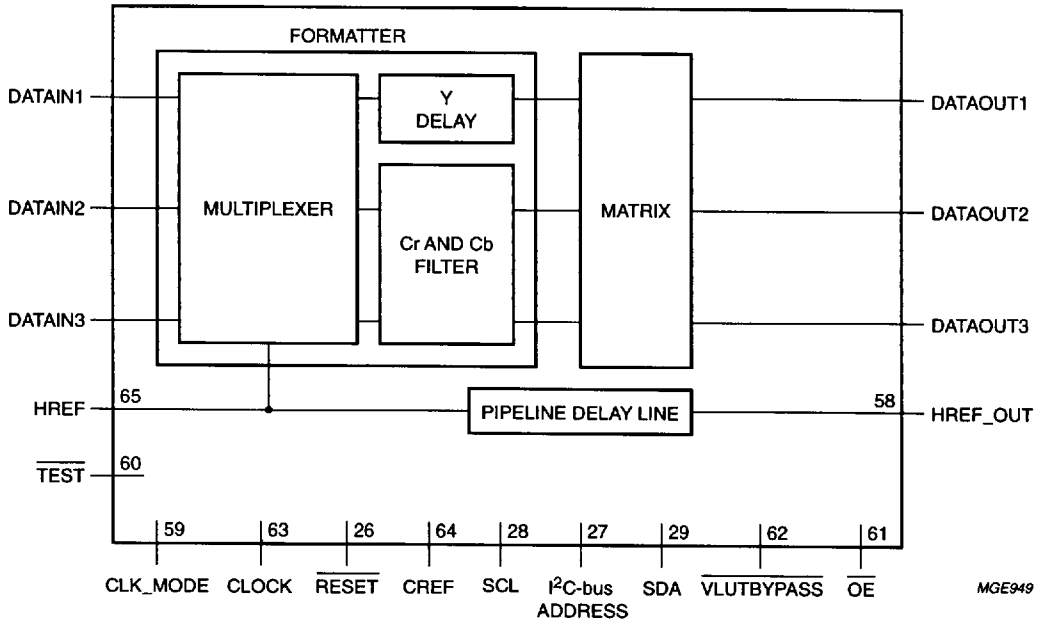


Fig.4 Functional modes 2 and 6.

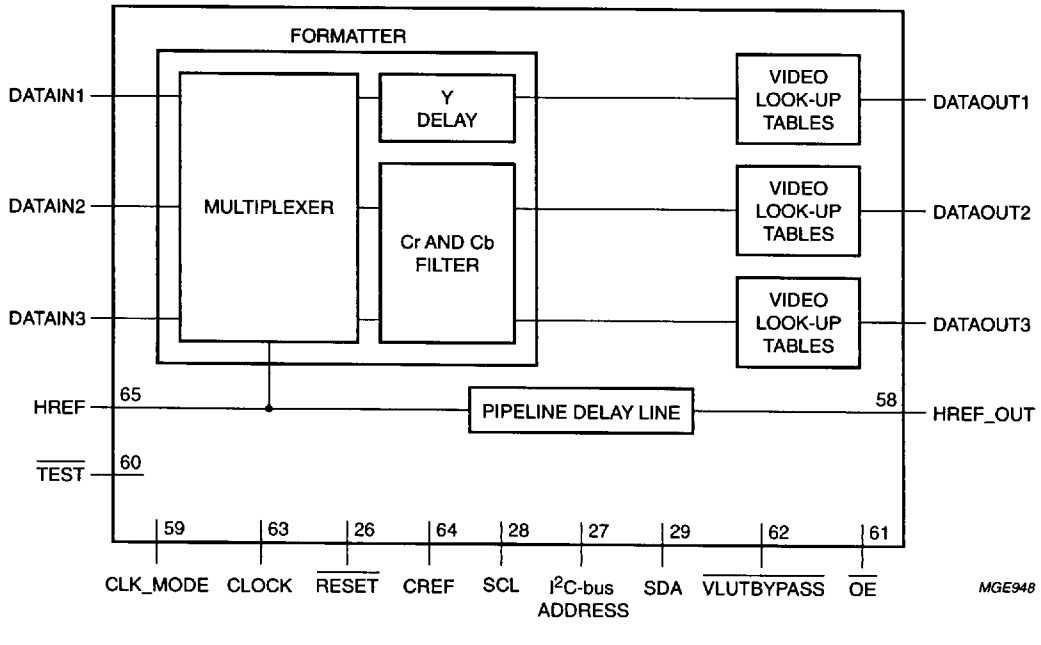


Fig.5 Functional modes 3 and 7.

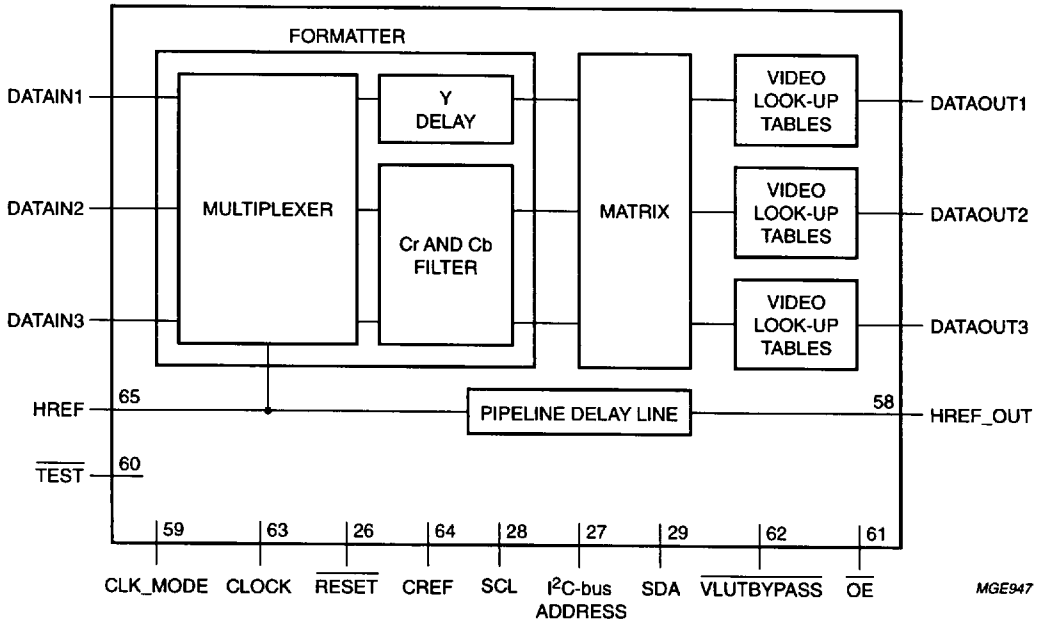


Fig.6 Functional modes 4 and 8.

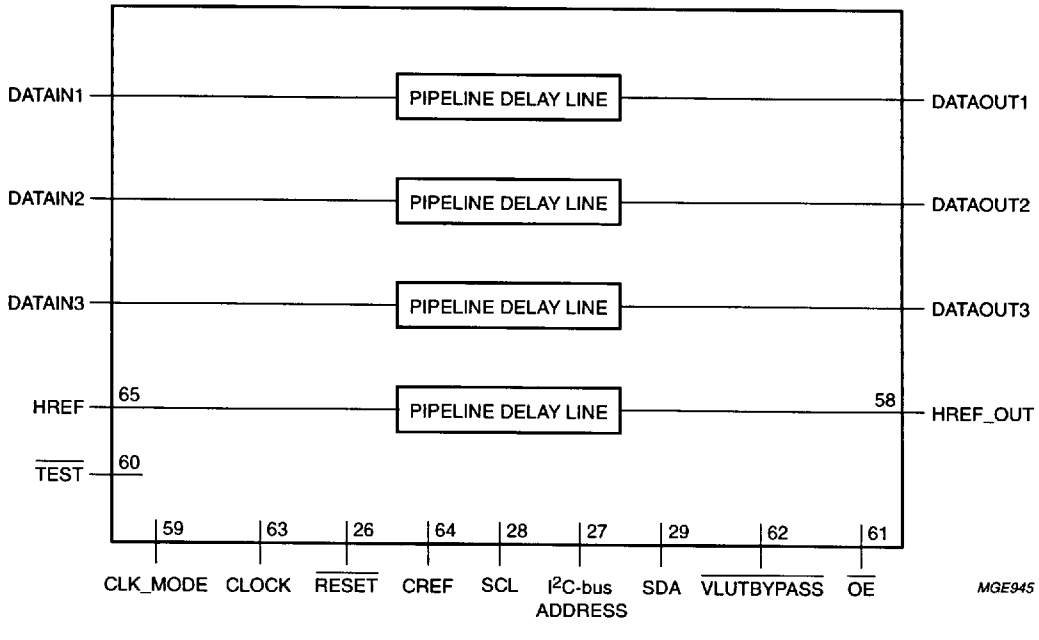


Fig.7 Functional mode 9.

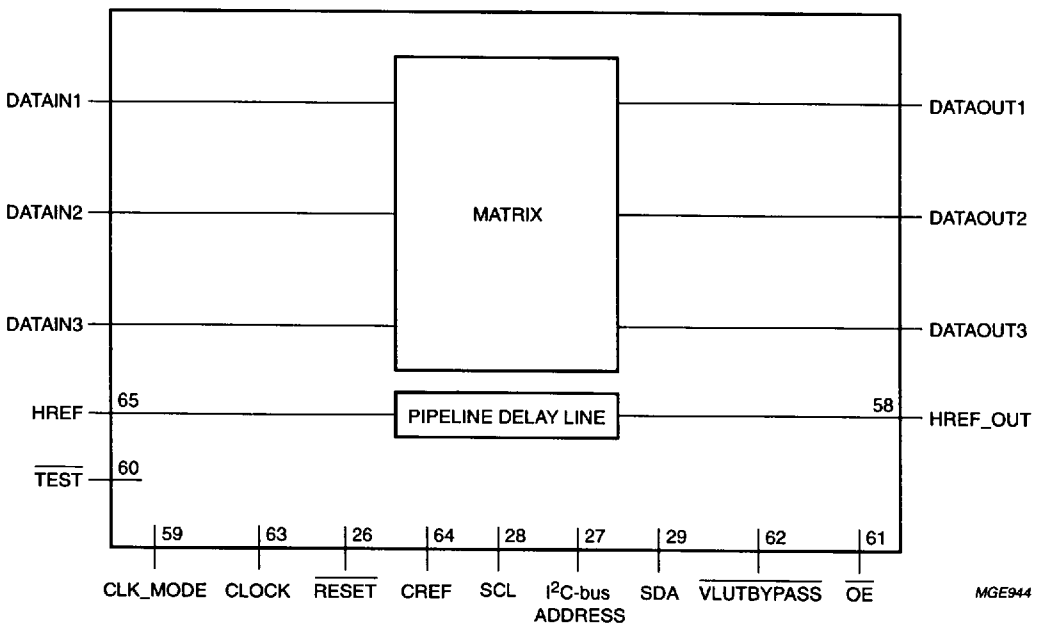


Fig.8 Functional mode 10.

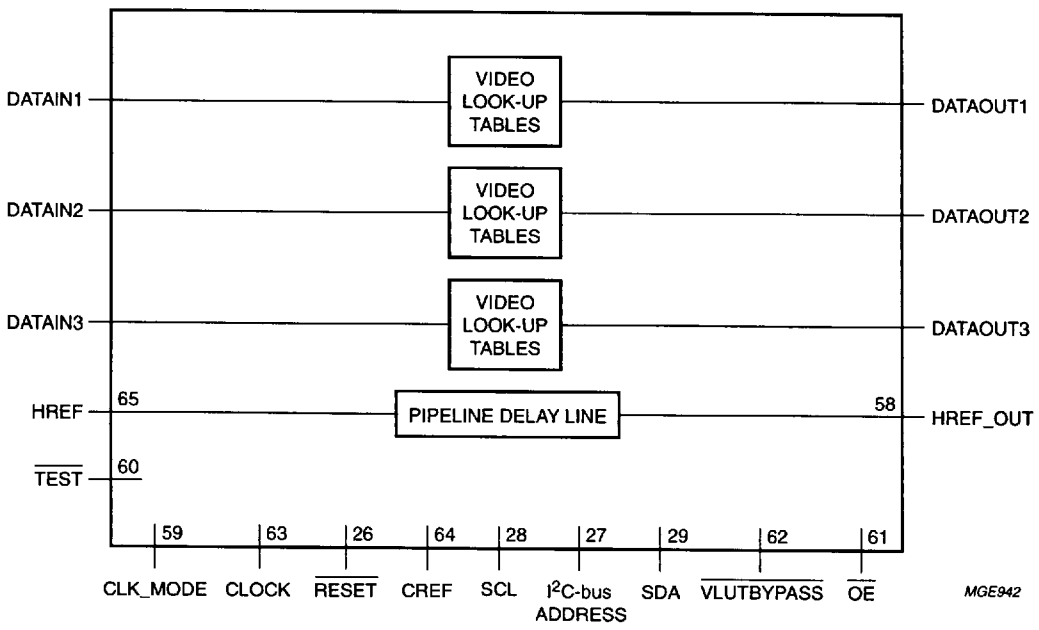


Fig.9 Functional mode 11.

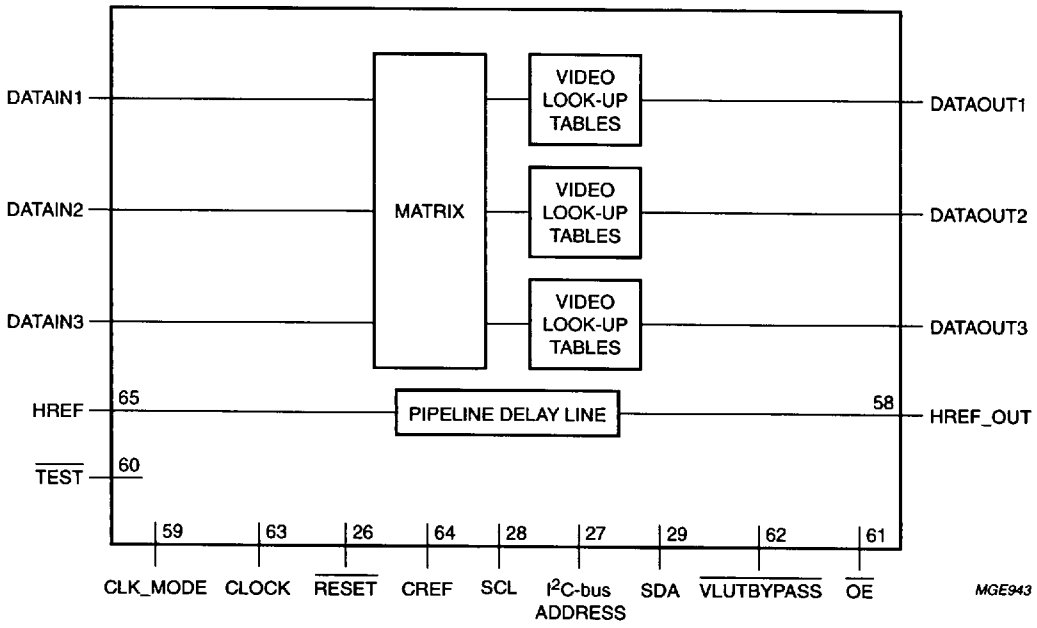


Fig.10 Functional mode 12.

6.2 Control

6.2.1 CONTROL SIGNALS

After power-up all internal control signals are in undefined states. The I²C-bus receiver must therefore be reset by using the external $\overline{\text{RESET}}$ signal.

Table 2 I²C-bus controls (subaddress 00H)

SIGNAL	BIT	FUNCTION
FMTCNTRL	D0 to D2	000; 4 : 1 : 1 format, DMSD2 format
		001; 4 : 1 : 1 format, customized format
		010; 4 : 2 : 2 format, from DMSD2
		011; 4 : 2 : 2 format, parallel
		100; 4 : 4 : 4 format, parallel; default
		101; not used
		110; not used
		111; not used
$\overline{\text{MATBYPASS}}$	D3	logic 1; matrix in use
		logic 0; matrix bypassed; default state after reset
$\overline{\text{INRESET}}$	D4	logic 1; input latches at the formatter are always transparent
		logic 0; at the end of each active video line the input signal will be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0); default state after reset
IICOE	D5	logic 1; $\overline{\text{OE}}$ enabled
		logic 0; switches the output to high impedance mode; default state after reset

Table 3 Selection of functional modes and input formats (see Table 1)

FMTCNTRL(1)	$\overline{\text{MATBYPASS}}$(2)	$\overline{\text{VLUTBYPASS}}$(3)	FUNCTIONAL MODE/INPUT FORMAT
000	0	0	mode 1, input format 0
000	1	0	mode 2, input format 0
001	0	0	mode 1, input format 1
001	1	0	mode 2, input format 1
010	0	0	mode 5, input format 2
010	1	0	mode 6, input format 2
011	0	0	mode 5, input format 3 (parallel IN)
011	1	0	mode 6, input format 3 (parallel IN)
100	0	0	mode 9, input format 4 (parallel IN)
100	1	0	mode 10, input format 4 (parallel IN)
XXX	X	1	each of the above modes will be multiplied by the factor loaded into the VLUT

Notes

1. FMTCNTRL: bits D0 to D2 of I²C-bus.
2. Bit D3 of I²C-bus.
3. Pin 62.

Table 4 Real-time control signals

SIGNAL	PIN	FUNCTION
$\overline{OE}$	61	logic 1; switches the output to high impedance mode
		logic 0; output enable, output stage in use
$\overline{VLUTBYPASS}$	62	logic 1; VLUTs in use
		logic 0; VLUTs bypassed
$\overline{RESET}$	26	logic 1; device in use
		logic 0; general reset
CLK_MODE	59	logic 1; DMSD mode (LL27 clock of DMSD feeds the DCSC)
		logic 0; DCSC is fed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 5 Output enable control

IICOE[1]	$\overline{OE}$[2]	STATE OF CONTROL LINE TO DRIVER STAGES
0	X	logic 1; DATAOUT in high impedance mode
1	1	logic 1; DATAOUT in high impedance mode
1	0	logic 0; DATAOUT working

Notes

1. IICOE: D5; output enable control of I^2C-bus (enables $\overline{OE}$).
2. $\overline{OE}$: pin 61; output enable (fast switch).

6.2.2 Clock

The CLK_MODE signal is used to select the frequency of the system clock (denoted as CLOCK at the DCSC input) and may be chosen from two different clock modes.

6.2.2.1 16 MHz mode

DCSC is used in any environment except that of the MPC-E decoder family. The clock reference signal (CREF) is internally set HIGH.

The maximum CLOCK frequency is 16 MHz.

6.2.2.2 DMSD mode

The DCSC is used in MPC-E digital decoder environment.

The CLOCK signal (pin 63) and the CREF signal (pin 64) are fed by the clock generator circuits or by one of the decoder circuits (clock = LL27). In the latter case the clock is twice the data rate. Internally the clock is set by referencing to CREF (see Section 6.2.2.3). This internal clock is denoted as CLOCK_A in Tables 7, 9, 11, 13 and 15.

The data rate on the input (DATAIN) is as follows:

12.2727 MHz; 60 Hz signals (from SAA7191/7110A)

13.5 MHz; CCIR signals (from SAA7151/7111A)

14.75 MHz; 50 Hz signals (from SAA7191/7110A)

16.0 MHz; maximum frequency.

6.2.2.3 *Timing reference*

The timing reference signals from the MPC-E decoders are used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data.

The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

- CREF: the clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Section 6.3 and also Chapter 7).
- HREF: the horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Chapter 7).

6.2.3 ERROR CONDITION

No information signal is available to the peripheral circuits to inhibit unwanted operations. In the advent of an error the DCSC must be re-started by application of the $\overline{\text{RESET}}$ signal.

6.3 System I/O interfaces

6.3.1 VIDEO DATA INPUT SIGNALS

Table 6 Format 0 (4 : 1 : 1, semi-parallel, MPC-E decoder family format)

INPUT	FUNCTION	SAMPLING FREQUENCY (MHz)	LEVEL
DATAIN1 = Y	luminance signal; 8-bit	12 to 16	0 IRE: black, quantization level 16 100 IRE: white, quantization level 235
DATAIN2	not used	–	–
DATAIN3 = U, V	multiplexed colour difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2	1/4 of the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 7 Timing of Format 0; pin (DATAIN) and bit (U, V) numbers are indicated except clock

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
DATAIN37	U7	U5	U3	U1	U7	U5	U3
DATAIN36	U6	U4	U2	U0	U6	U4	U2
DATAIN35	V7	V5	V3	V1	V7	V5	V3
DATAIN34	V6	V4	V2	V0	V6	V4	V2
CLOCK_A(1)	1	2	3	4	5	6	7

Note

1. CLOCK_A is the internal sampling clock of the system. The clock rate of the DMSD and the DCSC is twice that of CLOCK_A in this mode.

Table 8 Format 1 (4 : 1 : 1, semi-parallel, customized format)

INPUT	FUNCTION	SAMPLING FREQUENCY (MHz)	LEVEL
DATAIN1 = Y	luminance signal; 8-bit	12 to 16	0 IRE: black, quantization level 16 100 IRE: white, quantization level 235
DATAIN2	not used	–	–
DATAIN3 = Cr, Cb	multiplexed colour difference signals, 8-bit	1/4 of the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 9 Timing of Format 1; the indices show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	–	Cr0	–	Cb4	–	Cr4
CLOCK_A[1]	0	1	2	3	4	5	6

Note

1. CLOCK_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

Table 10 Format 2 (4 : 2 : 2, semi-parallel, DMSD2 format)

INPUT	FUNCTION	SAMPLING FREQUENCY (MHz)	LEVEL
DATAIN1 = Y	luminance signal; 8-bit	12 to 16	0 IRE: black, quantization level 16 100 IRE: white, quantization level 235
DATAIN2	not used	–	–
DATAIN3 = Cr, Cb	multiplexed colour difference signals; corresponds to UV7 to UV0 of DMSD2	1/2 of the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 11 Timing of Format 2

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6
CLOCK_A[1]	0	1	2	3	4	5	6

Note

1. CLOCK_A is the internal sampling clock of the system. The clock of the DMSD (also the CLOCK of the DCSC) is twice that of CLOCK_A in this mode.

Table 12 Format 3 (4 : 2 : 2, Y-Cr-Cb, parallel)

INPUT	FUNCTION	SAMPLING FREQUENCY (MHz)	LEVEL
DATAIN1 = Y	luminance signal; 8-bit	12 to 16	0 IRE: black, quantization level 16 100 IRE: white, quantization level 235
DATAIN2 = Cr	colour difference signal R-Y, 8-bit	½ of the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN3 = Cb	colour difference signal B-Y; 8-bit	½ of the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 13 Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	–	Cb2	–	Cb4	–	Cb6
Cr	Cr0	–	Cr2	–	Cr4	–	Cr6
CLOCK_A[1]	0	1	2	3	4	5	6

Note

1. CLOCK_A is the internal sampling clock of the system. The external CLOCK may differ from the CLK_MODE.

Table 14 Format 4 (4 : 4 : 4, Y-Cr-Cb, parallel)

INPUT	FUNCTION	SAMPLING FREQUENCY (MHz)	LEVEL
DATAIN1 = Y	luminance signal; 8-bit	12 to 16	0 IRE: black, quantization level 16 100 IRE: white, quantization level 235
DATAIN2 = Cr	colour difference signal R-Y, 8-bit	as the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; binary 128
DATAIN3 = Cb	colour difference signal B-Y; 8-bit	as the Y signal	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 15 Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
CLOCK_A[1]	0	1	2	3	4	5	6

Note

1. CLOCK_A is the internal sampling clock of the system. The external CLOCK may differ from CLK_MODE.

6.3.2 VIDEO DATA OUTPUT SIGNALS

Table 16 Format of DATAOUT (R-G-B if matrix in use)

OUTPUT	FUNCTION	SAMPLING FREQUENCY (MHz)	LEVEL
DATAOUT1 = R	red signal	equal to DATAIN1	0 IRE: black, binary 16 100 IRE: white, binary 235
DATAOUT2 = G	green signal	equal to DATAIN1	0 IRE: black, binary 16 100 IRE: white, binary 235
DATAOUT3 = B	blue signal	equal to DATAIN1	0 IRE: black, binary 16 100 IRE: white, binary 235

Table 17 Timing of DATAOUT (R-G-B if matrix in use); note 1

DATAOUT1[2]	R0	R1	R2	R3	R4	R5	R6
DATAOUT2[2]	G0	G1	G2	G3	G4	G5	G6
DATAOUT3[2]	B0	B1	B2	B3	B4	B5	B6
CLOCK_A[3]	0	1	2	3	4	5	6

Notes

1. See Fig.24.
2. $\overline{OE}$ (output enable, fast switch, active LOW) and IICOE (I^2C-bus output enable, active HIGH) will switch the DATAOUT lines to their high impedance state or normal mode.
3. CLOCK_A is the internal sampling clock of the system. The system clock may differ from CLK_MODE.

6.3.3 AUXILIARY DATA

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (word length 1-bit) has the same duration as the signal processing of the video data lines.

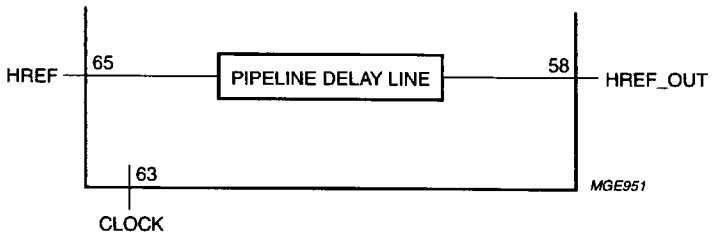


Fig.11 Delayed HREF.

6.4 System block description

6.4.1 INPUT FORMATTER WITH FILTER

The formatter is shown in Fig.12 and consists of five functional blocks:

- The multiplexer, which decodes the luminance and chrominance input signals
- The filter, which interpolates the samples on DATAIN2 and DATAIN3 to the data rate used for DATAIN1
- The luminance delay line
- The timing control which creates the internal reference signals from the various inputs
- The bypass output multiplexer.

The data applied at DATAIN1 to DATAIN3 is converted as follows:

- FIL1: Y Luminance
- FIL2: Cr colour-difference signal R-Y
- FIL3: Cb colour-difference signal B-Y.

In the various functional modes the signal FMTCNTRL switches in the required filters (see Section 6.2).

In all modes the same propagation delay will be realized, (the reference is Cb0, respective to U7 with format 0).

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

The filter for the Cr and Cb signal is realized in one filter design.

- Format 0 and 1; 4 : 1 : 1

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. four times that of the colour signal. Figure 13 illustrates the frequency response of the chrominance section.

- Format 2 and 3; 4 : 2 : 2

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. twice the colour signal. Figure 14 illustrates the frequency response of the chrominance section.

- Format 4; 4 : 4 : 4

A bypass with a specified delay is inserted.

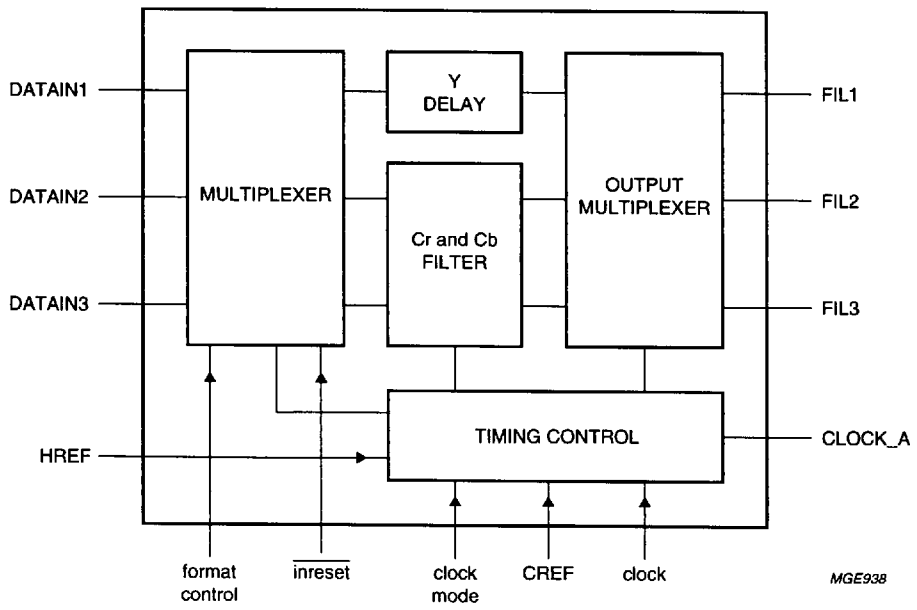


Fig.12 Input formatter.

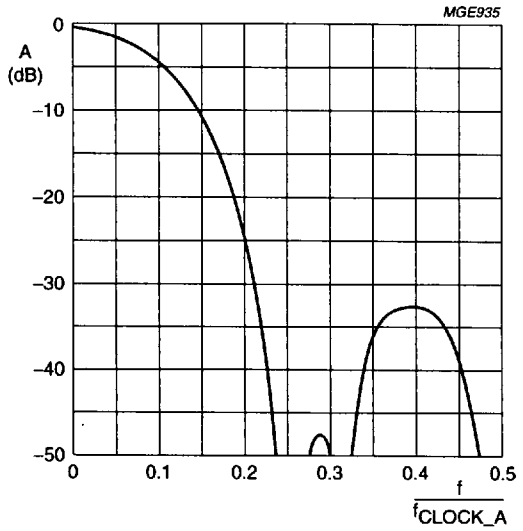


Fig.13 Frequency response of 4 : 1 : 1 filter.

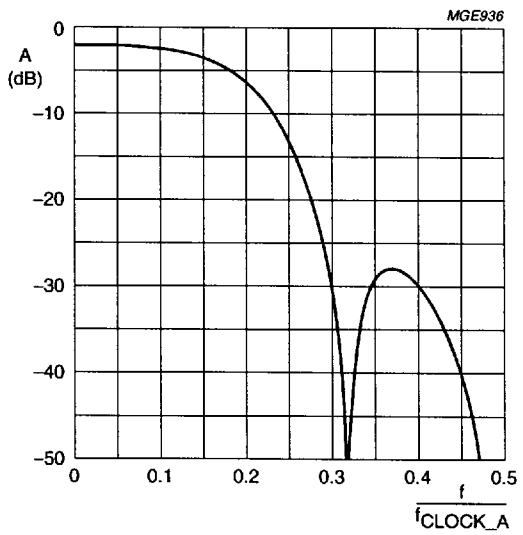


Fig.14 Frequency response of 4 : 2 : 2 filter.

6.4.2 CONVERSION MATRIX

The properties of the conversion matrix are as follows:

- The conversion equations are (according to *"CCIR 601"*, with respect to the different quantization on Y, Cb and Cr)
- Red = Y + 1.371(Cr – 0.5)

  Green = Y – 0.698(Cr – 0.5) – 0.336(Cb – 0.5)

  Blue = Y + 1.732(Cb – 0.5)
- The accuracy of the signal processing is within ±0.5% of the accuracy of a theoretical conversion
- The input and output data lines are 8-bit
- In the advent of non-standard input levels, the limiter reduces the possible output data values to between 0 and 255
- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass which has the same propagation delay as the matrix itself.

Table 18 shows the levels as normalized to unity for primary RGB signals, quantized levels according to *"CCIR Report 629-2"* for input and output signals at the DCSC.

The RGB levels at the output of the DCSC are within ±1 LSB of the levels according to a theoretical transformation.

Table 18 Levels of the colour bar signal (note 1)

CONDITION	E'_R	E'_G	E'_B	Y	C_R	C_B	R	G	B
White	1.0	1.0	1.0	235	128	128	235	235	235
Black	0	0	0	16	128	128	16	16	16
Red	1.0	0	0	82	240	90	236	17	16
Green	0	1.0	0	145	34	54	16	236	17
Blue	0	0	1.0	41	110	240	16	16	235
Yellow	1.0	1.0	0	210	146	16	235	235	16
Cyan	0	1.0	1.0	170	16	166	16	235	236
Magenta	1.0	0	1.0	106	222	202	235	15	234

Note

1. The colour bar signal is described in *"CCIR 601, Rep. 629-2, Table 1"*. It can be used to check the nominal levels (at least for black and white) between the functional blocks of the DCSC.

6.4.3 VIDEO LOOK-UP TABLE AND OUTPUT STAGE

6.4.3.1 VLUTDATA, VLUTSELECT and VLUTVALID

These signals are produced by the I²C-bus receiver to control access to the VLUT RAMs.

The I²C-bus protocol has four subaddresses implemented to direct the data into different VLUT RAMs. Each RAM can be addressed individually or all three RAMs together.

The next byte of the protocol will address the starting address of the individual RAM, e.g. if only parts of the data need to be changed.

In computer applications the VLUT is also known as a Colour Look-Up Table (CLUT). In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.

The Gamma-correction function (also known as Gradation) is given as:

$Y = X^{\gamma}$

The VLUTs are realized by 256 × 8-bit RAMs.

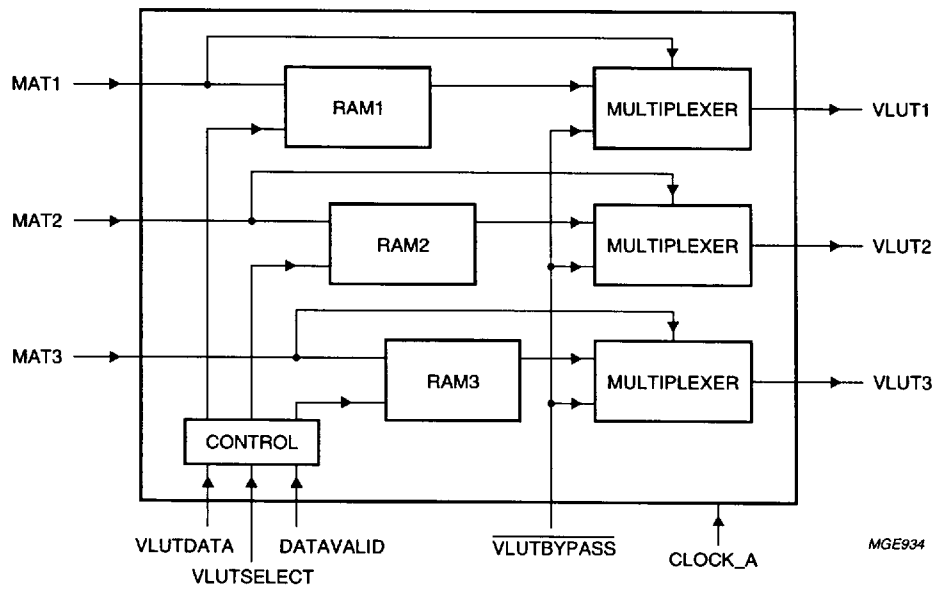


Fig.15 Block diagram video look-up table.

6.4.4 I²C-BUS RECEIVER

The DCSC can be switched to different functional modes via the I²C-bus receiver. To carry out this operation the Control Register is addressed and then loaded with the appropriate data as specified in Table 20. The timing diagram for the loading operation is shown in Fig.19. The I²C-bus receiver is also used to load the VLUT RAMs with data. The timing diagram for this operation is shown in Fig.21.

Full details of the I²C-bus are given in the document *"The I²C-bus and how to use it"*. This document may be ordered using the code 9398 393 40011.

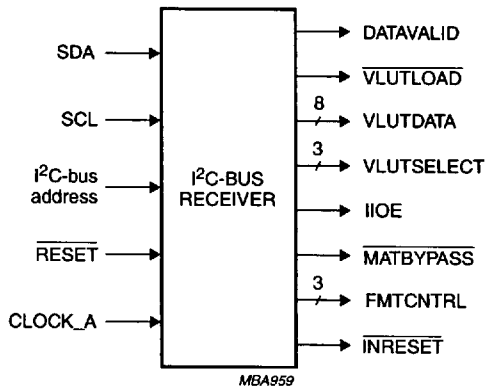


Fig.16 Block diagram of I²C-bus receiver.

6.4.4.1 I²C-bus receiver functional description

Following power-up, all internal control signals are at undefined values. The I²C-bus receiver must therefore be reset to a known state using the external RESET signal; see Table 19.

Table 19 State of I²C-bus internal control signals (subaddress 00H) after an external reset

SIGNAL	BIT	STATE AFTER RESET
IICOE	D5	logic 1; OE pin enabled
INRESET	D4	logic 0; input data set to fixed values
MATBYPASS	D3	logic 0; matrix by-passed
FMTCNTRL	D2 to D0	100; format 4 : 4 : 4

6.4.4.2 *Receiver organisation*

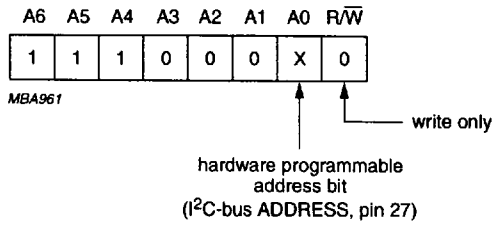
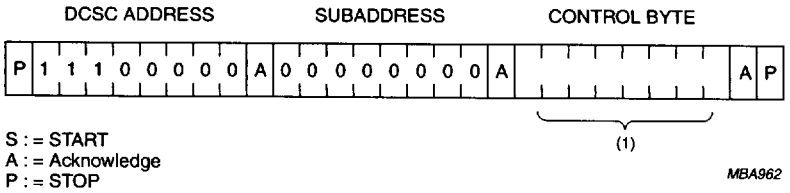


Fig.17 The DCSC address.



(1) See Table 20.

Fig.18 Addressing the control byte (address 00H).

Table 20 Selection of functional modes and input formats (note 1)

FMTCNTRL(2)	$\overline{\text{MATBYPASS}}$(3)	$\overline{\text{VLUTBYPASS}}$(4)	FUNCTIONAL MODE/INPUT FORMAT
000	0	0	mode 1, input format 0
000	1	0	mode 2, input format 0)
001	0	0	mode 1, input format 1
001	1	0	mode 2, input format 1
010	0	0	mode 5, input format 2
010	1	0	mode 6, input format 2
011	0	0	mode 5, input format 3 (parallel IN)
011	1	0	mode 6, input format 3 (parallel IN)
100	0	0	mode 9, input format 4 (parallel IN)
100	1	0	mode 10, input format 4 (parallel IN)
XXX	X	1	each of the above modes will be multiplied by the factor loaded into the VLUT

Notes

1. The functional modes are specified in Table 1.
2. FMTCNTRL: bits D0 to D2 of I²C-bus.
3. Bit D3 of I²C-bus.
4. Pin 62.

Table 21 Other control signals

SIGNAL	STATE	FUNCTION
$\overline{\text{INRESET}}$ (1)	logic 1	input latches at the formatter are always transparent
	logic 0	at the end of each active video line the input signals will be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)
CLK_MODE(2)	logic 1	DMSD mode (LL27 clock of DMSD feeds the DCSC)
	logic 0	DCSC is fed by a maximum 16 MHz clock without CREF signal

Notes

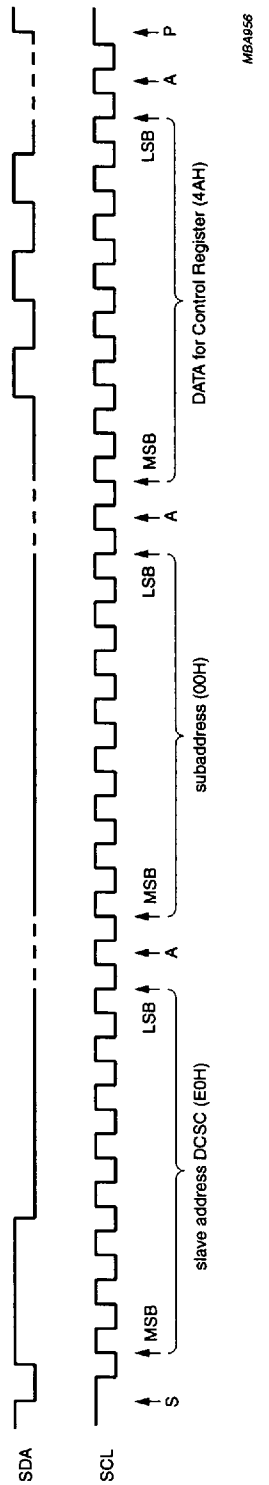
1. Pin of I²C-bus.
2. Pin 59.

Table 22 Output enable control

IICOE(1)	$\overline{\text{OE}}$(2)	STATE OF CONTROL LINE TO DRIVER STAGES
0	X	logic 1; DATAOUT in high impedance mode
1	1	logic 1; DATAOUT in high impedance mode
1	0	logic 0; DATAOUT working

Notes

1. IICOE : D5; output enable control of I²C-bus (enables $\overline{\text{OE}}$).
2. $\overline{\text{OE}}$: pin 61; output enable (fast switch).



S : = START condition

A : = acknowledge from DCSC

P : = STOP condition

In this example the state of the internal control signals are as follows: FMTCNTRL = 010; $\overline{\text{MATBYPASS}}$ = 1; $\overline{\text{INRESET}}$ = 0 and IICOE = 1.

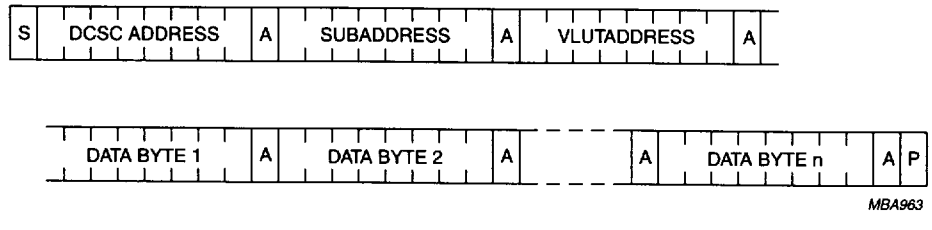
Fig.19 Example of Control Register loading.

6.4.4.3 *VLUTDATA*

Four subaddresses are implemented to load data into the different VLUT RAMs. RAM can be addressed as a whole or each VLUT RAM can be addressed individually, e.g. if only part of the data has to be changed. An example of loading a VLUT RAM is shown in Fig.21.

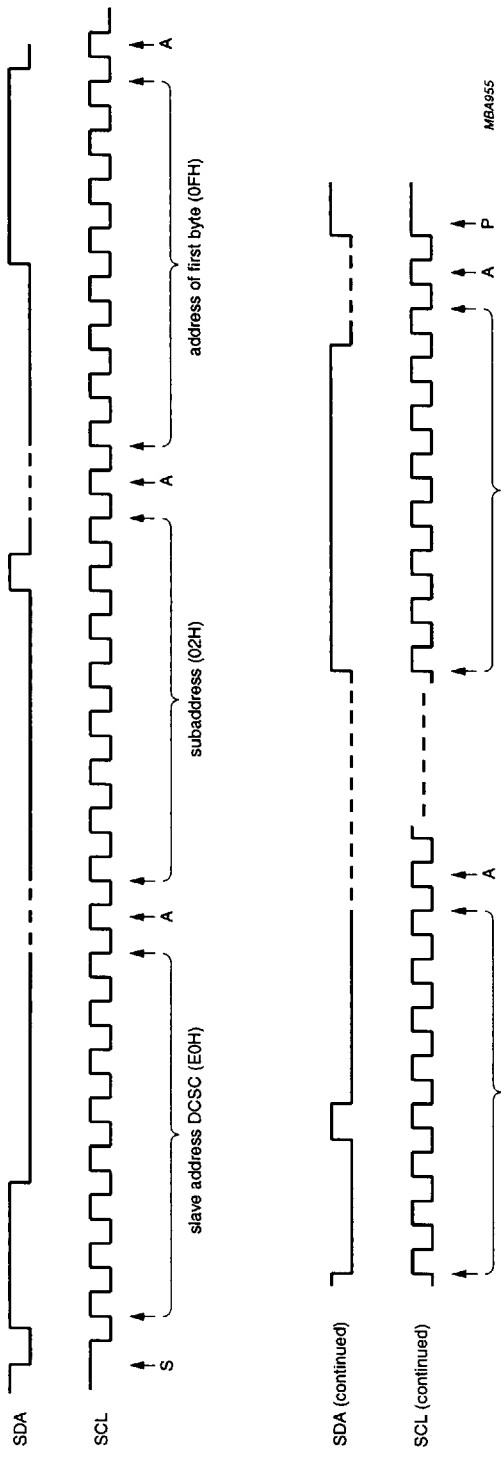
Table 23 Subaddresses VLUTDATA

SUBADDRESS (HEX)	VLUT-ADDRESS (HEX)	DATA BYTES
01	XX	VLUTDATA RAM 1 (RED)
02	XX	VLUTDATA RAM 2 (GREEN)
03	XX	VLUTDATA RAM 3 (BLUE)
04	XX	VLUTDATA RAM 1, 2 and 3



S : = START
A : = Acknowledge
P : = STOP

Fig.20 Subaddresses VLUTDATA.



S : = START condition

A : = acknowledge from DCSC

P : = STOP condition

In this example the second RAM (GREEN) receives new data at the start of address OFH.
The VLUT addresses are automatically incremented by writing data via the SDA line.

Fig.21 Example of VLUT loading.

7 OPERATING CONDITIONS

7.1 Electrical conditions

7.1.1 START-UP CONDITION

No particular function except the external Power-on-reset e.g. for I²C-bus interface (RESET) is intended.

7.1.2 OPERATING TIME

As this device will be used in computers, it has been designed to operate continuously.

7.1.3 TEMPERATURE RANGE

Refer to Chapter 8.

7.1.4 BACKUP

No internal backup capability (standby) is provided.

7.1.5 POWER-DOWN MODE

No internal Power-down capability is provided.

7.1.6 HANDLING

Inputs and outputs are protected against electrostatic discharge during normal handling. It is desirable, however, to observe normal handling precautions appropriate to MOS devices.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	input voltage	−0.5	+7	V
V_O	output voltage	−0.5	+7	V
P_{tot}	total power dissipation	−	1.5	W
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C

9 DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	supply current	note 1	–	150	mA
Inputs					
V_{IL}	LOW level input voltage:				
	except SDA and SCL		−0.5	+0.8	V
	SDA and SCL		−0.5	+1.5	V
V_{IH}	HIGH level input voltage:				
	except SDA, SCL, $\overline{\text{RESET}}$ and CLK_MODE		2	V_{DD} + 0.5	V
	SDA and SCL		3	V_{DD} + 0.5	V
	$\overline{\text{RESET}}$ and CLK_MODE		2.4	–	V
I_{LI}	input leakage current	note 2	–	10	µA
C_I	input capacitance		–	10	pF
Outputs					
V_{OH}	HIGH level output voltage		2.4	V_{DD}	V
V_{OL}	LOW level output voltage		0	0.4	V
I_{OH}	HIGH level output current		–	−4	mA
I_{OL}	LOW level output current:				
	except SDA		–	4	mA
	SDA		–	3	mA
C_L	output load capacitance		–	40	pF
I_{LO}	output leakage current		–	10	µA

Notes

1. The supply current may vary between 30 and 150 mA depending upon the input data. The minimum may be achieved with $\overline{\text{OE}}$ disabled and no clock.
2. All inputs except $\overline{\text{TEST}}$ (internal pull-up resistor).

10 TIMING CHARACTERISTICS

Typical ratings are measured at V_{DD} = 5 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{C27}	clock cycle time	note 1	31	–	45	ns
t_{C16}	clock cycle time	16 MHz mode; note 2	62	–	83	ns
t_{CDL}	clock duty time LOW	note 2	25	–	–	ns
t_{CDH}	clock duty time HIGH	note 2	25	–	–	ns
t_{CS}	CREF set-up time		11	–	–	ns
t_{CH}	CREF hold time		3	–	–	ns
t_{HS}	HREF set-up time		11	–	–	ns
t_{HH}	HREF hold time		3	–	–	ns
t_{RH}	$\overline{\text{RESET}}$ hold time		4 clock periods			
t_{VS}	$\overline{\text{VLUTBYPASS}}$ set-up time	note 3	8	–	–	ns
t_{VH}	$\overline{\text{VLUTBYPASS}}$ hold time	note 3	0	–	–	ns
t_{SU}	DATAIN set-up time		11	–	–	ns
t_{HD}	DATAIN hold time		3	–	–	ns
t_{OS}	DATAOUT set-up time		10	–	–	ns
t_{OH}	DATAOUT hold time		10	–	–	ns
t_{OHS}	HREF_OUT set-up time		9	–	–	ns
t_{OHH}	HREF_OUT hold time		10	–	–	ns
t_{HZ}	output disable time (to 3-state)		–	10	15	ns
t_{ZH}	output enable time (from 3-state)		–	15	21	ns

Notes

1. DMSD mode designates that the DCSC will work in a DMSD environment. The CLOCK and the clock reference signal CREF will be fed by the SCGC (SAA7157); see Figs 22 to 24.
2. 16 MHz mode indicates that the DCSC will work in any other environment. The CREF signal will be set internally to HIGH, the CLOCK signal can be any clock up to 16 MHz; see Figs 23 and 25.
3. Must be set one clock period before DATAOUT; see Fig.25.

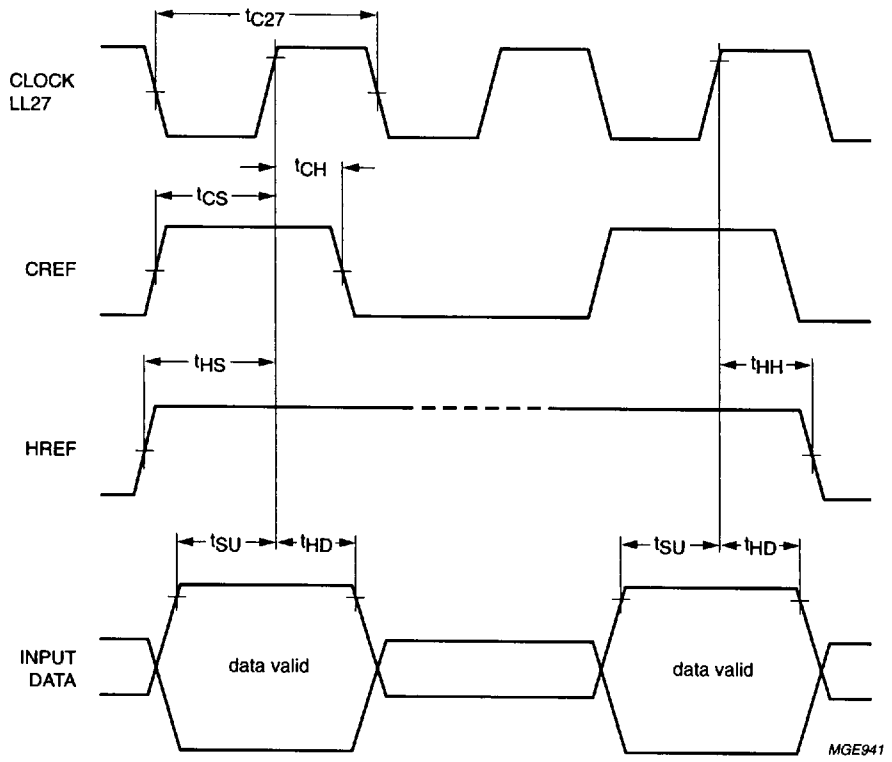


Fig.22 Timing diagram input (DMSD mode).

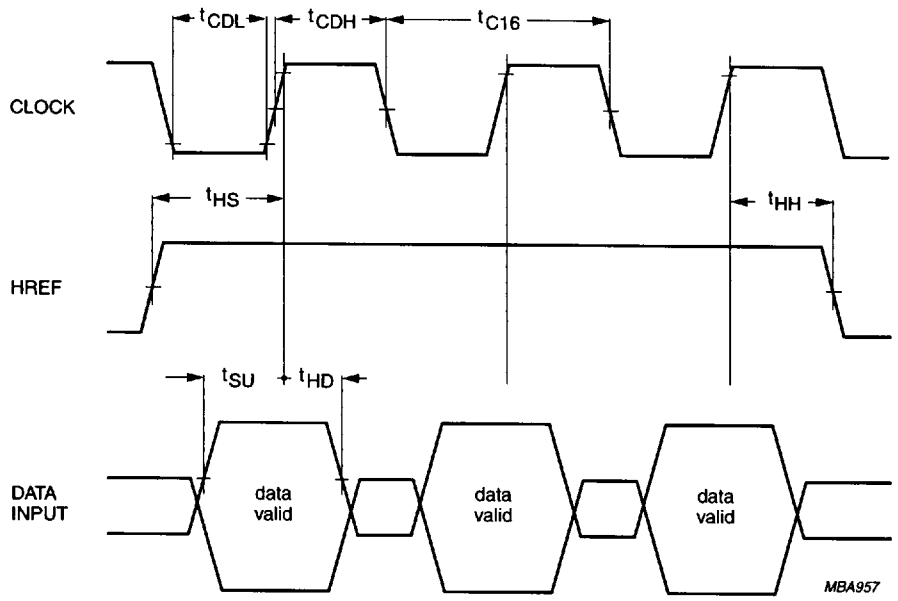
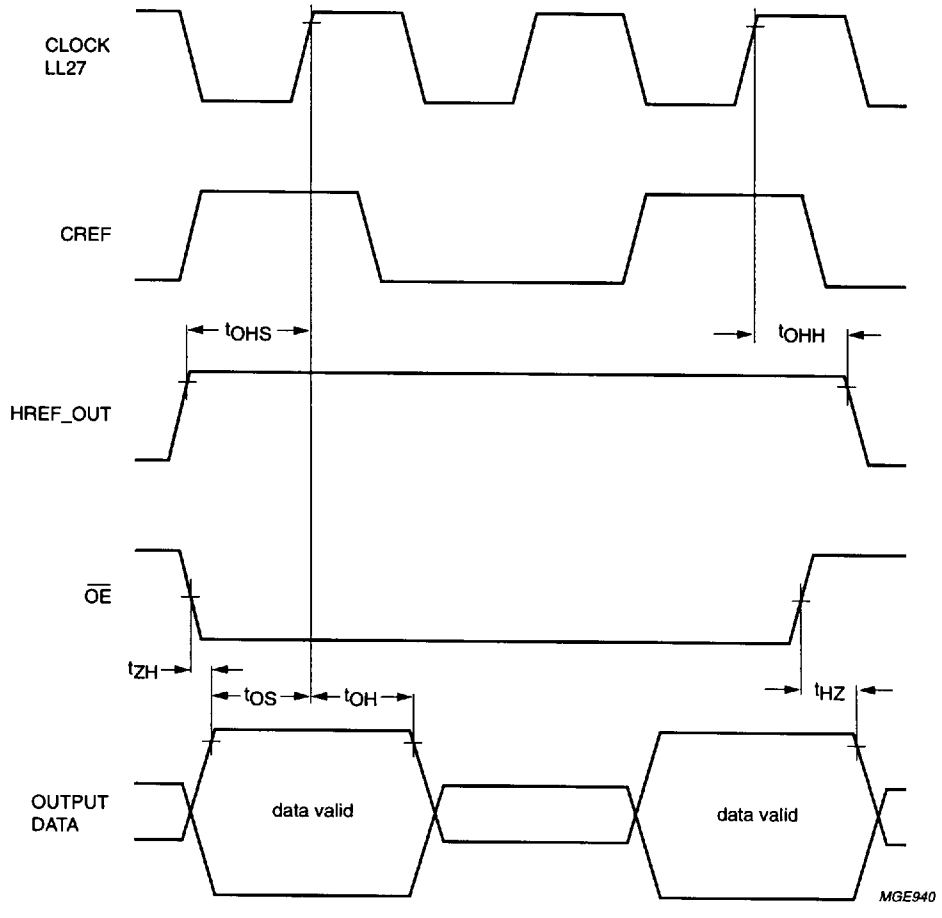
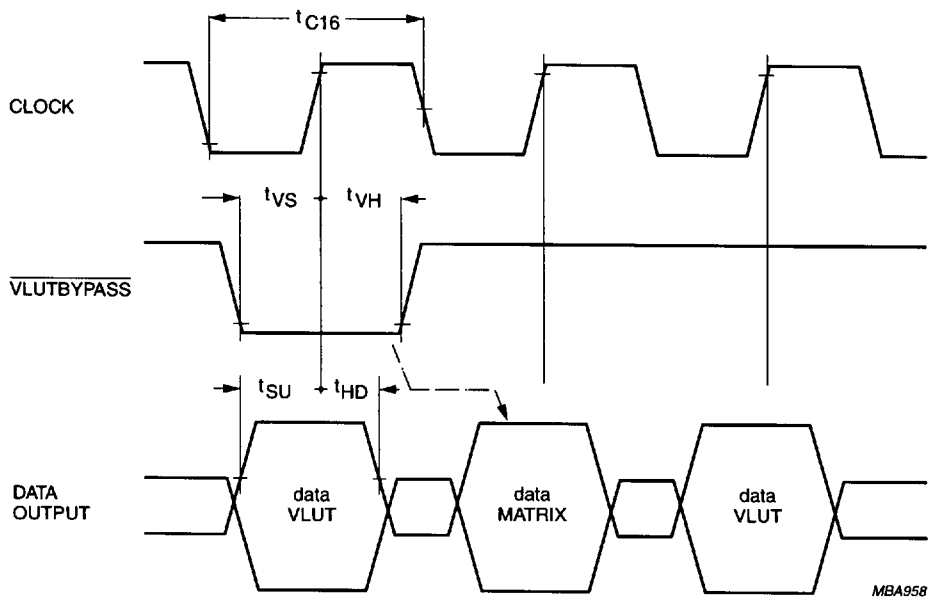


Fig.23 Timing diagram input (16 MHz mode).i



$\overline{OE}$ will also affect HREF_OUT.

Fig.24 Timing diagram output.

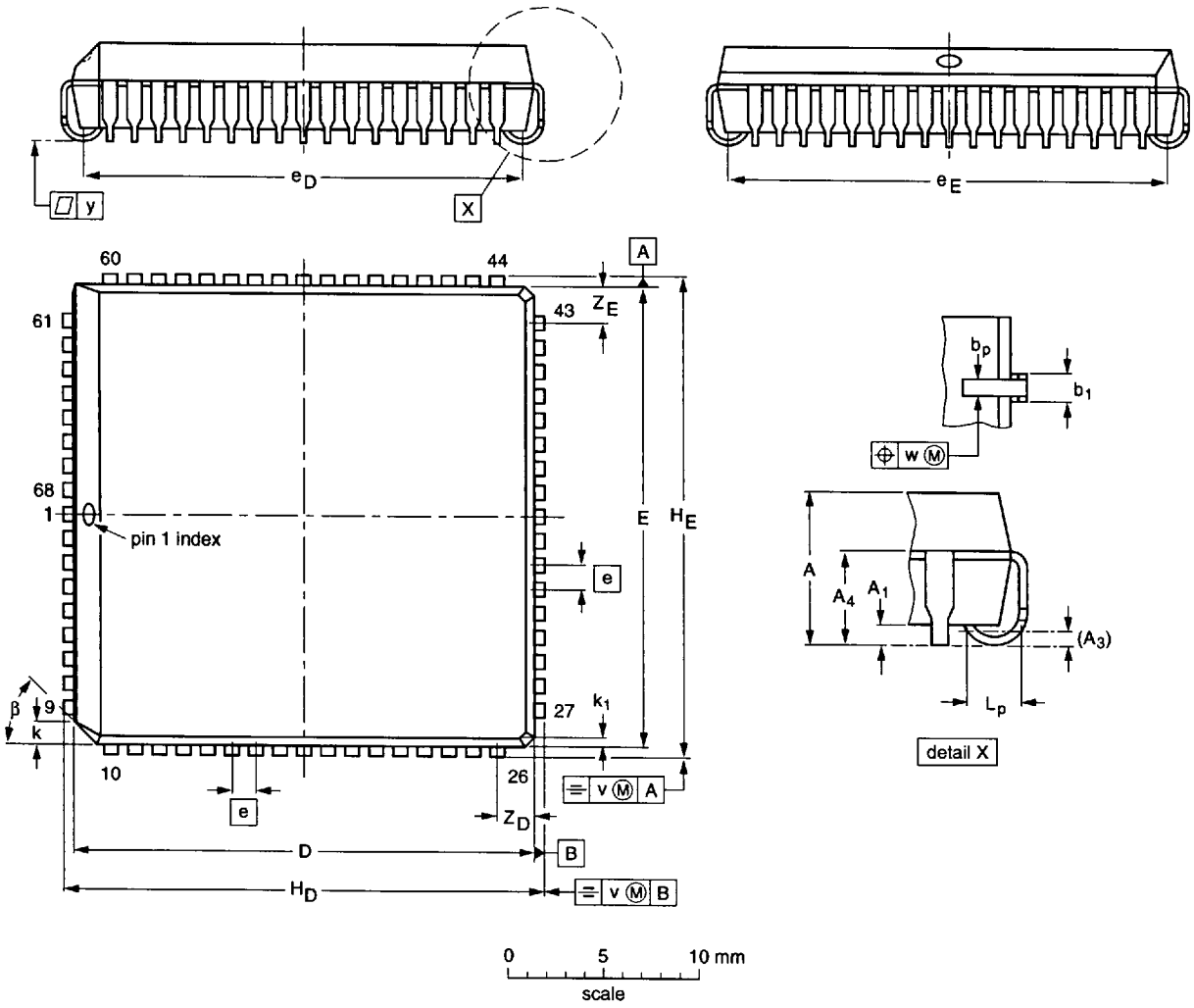


$\overline{\text{VLUTBYPASS}}$ must be supplied one clock pulse in advance of the desired DATAOUT lines reaction.

Fig.25 Timing diagram $\overline{\text{VLUTBYPASS}}$.

11 PACKAGE OUTLINE

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

12 SOLDERING

12.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

12.2 Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

12.3 Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.