



STD100N03L-1 STD100N03L

N-CHANNEL 30V - 0.0045Ω - 80A - DPAK - IPAK
Planar STripFET™ MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STD100N03L	30 V	<0.0055 Ω	80 A(1)	110 W
STD100N03L-1	30 V	<0.0055 Ω	80 A(1)	110 W

- 100% AVALANCHE TESTED
- SURFACE-MOUNTING DPAK (TO-252)
- LOGIC LEVEL THRESHOLD

Description

This MOSFET is the latest refinement of STMicroelectronic unique "Single Feature Size™" strippased process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics, low gate charge and less critical alignment steps therefore a remarkable manufacturing reproducibility. This new improved device has been specifically designed for Automotive application and DC-DC converters.

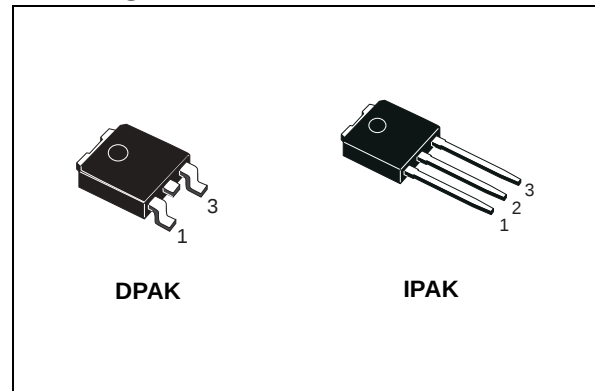
Applications

- HIGH CURRENT, HIGH SWITCHING DC-DC CONVERTER
- AUTOMOTIVE

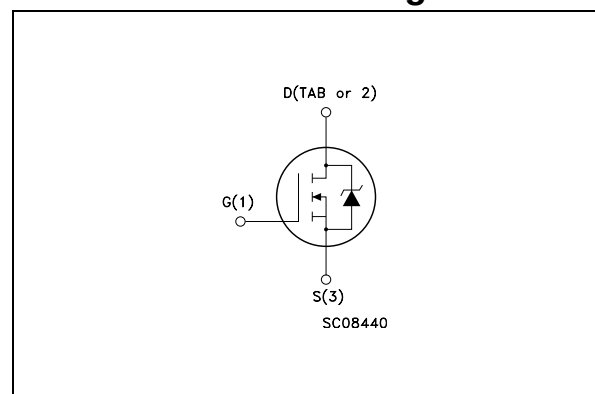
Order codes

Sales Type	Marking	Package	Packaging
STD100N03LT4	D100N03L	DPAK	TAPE & REEL
STD100N03L-1	D100N03L-1	IPAK	TUBE

Package



Internal schematic diagram



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D <i>Note 1</i>	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	70	A
I_{DM} <i>Note 2</i>	Drain Current (pulsed)	320	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating Factor	0.73	W/ $^\circ\text{C}$
dv/dt <i>Note 3</i>	Peak Diode Recovery Voltage Slope	3.9	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	$^\circ\text{C}$

Table 2. Thermal Data

$R_{thj-case}$	Thermal Resistance Junction-case Max	1.36	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	$^\circ\text{C/W}$
T_I	Maximum Lead Temperature For Soldering Purpose (for 10sec. 1.6 mm from case)	275	$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Not-Repetitive Avalanche Current (pulse width limited by T_j max)	40	A
E_{AS}	Single pulsed avalanche Energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AV}$, $V_{DD} = 24\text{V}$)	500	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/Off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, V _{DS} = Max Rating, T _C = 125°C			10 100	μA μA
I _{GSS}	Gate Body Leakage Current (V _{DS} = 0)	V _{DS} = ± 20 V			±200	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 40 A V _{GS} = 5 V, I _D = 20 A		0.0045 0.008	0.0055 0.01	Ω Ω
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 40 A @125°C V _{GS} = 5 V, I _D = 20 A @125°C		0.0068 0.0146		Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} <i>Note 4</i>	Forward Transconductance	V _{DS} = 10 V, I _D = 15 A		31		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2060 728 67		pF pF pF
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 24 V, I _D = 80 A, V _{GS} = 5V (see Figure 15)		20 7 7.5	27	nC nC nC
R _G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.9		Ω

Table 6. Switching time

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 15 V, I _D = 40 A R _G = 4.7 Ω, V _{GS} = 10V, (see Figure 14)		9 205		ns ns
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 15 V, I _D = 40 A R _G = 4.7 Ω, V _{GS} = 10V, (see Figure 14)		31 35		ns ns

Table 7. Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-Drain Current				80	A
I_{SDM} Note 2	Source-Drain Current (pulsed)				320	A
V_{SD} Note 4	Forward On Voltage	$I_{SD} = 40\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		40		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 25\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$		40		nC
I_{RRM}	Reverse Recovery Current	(see Figure 16)		2		A

(1) Current limited by package.

(2) Pulse width limited by safe operating area

(3) $I_{SD} \leq 80\text{ A}$, $di/dt \leq 360\text{ A}/\mu\text{s}$, $V_{DS} \leq V_{(BR)DSS}$, $T_j \leq T_{jMAX}$

(4) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe Operating Area

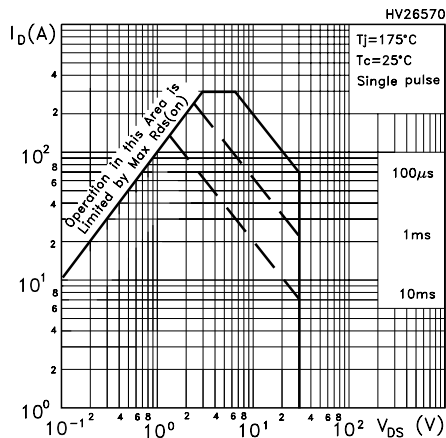


Figure 2. Thermal Impedance

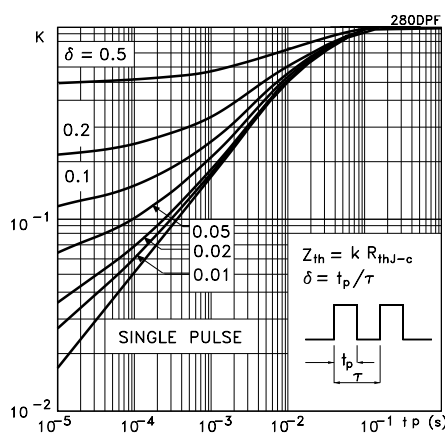


Figure 3. Output Characteristics

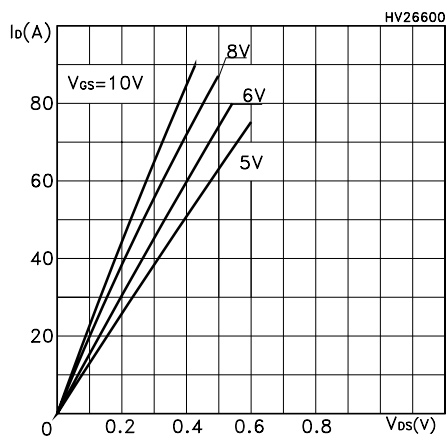


Figure 4. Transfer Characteristics

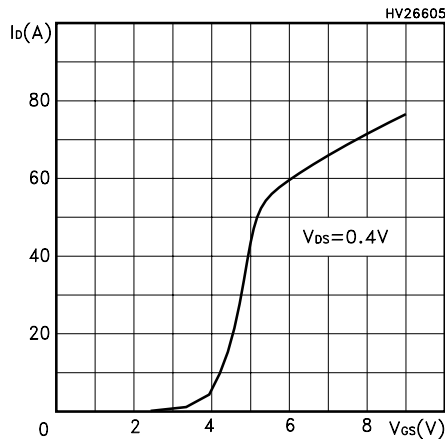


Figure 5. Transconductance

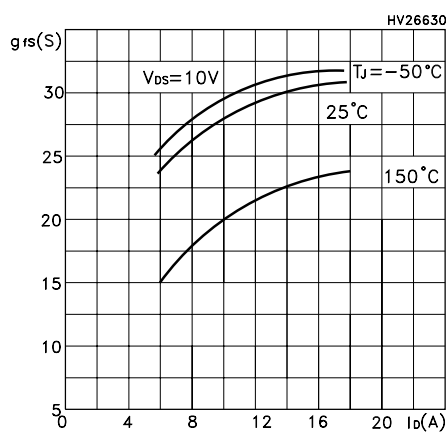


Figure 6. Static Drain-source on Resistance

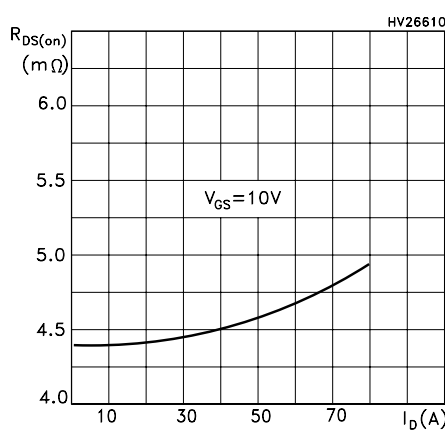


Figure 7. Gate Charge vs Gate-source Voltage

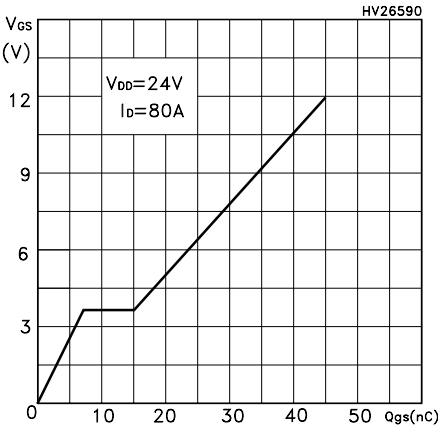


Figure 8. Capacitance Variation

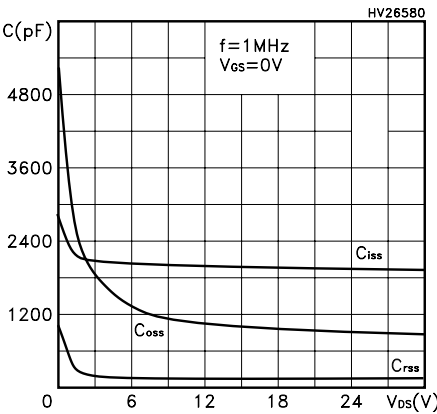


Figure 9. Normalized Gate Threshold Voltage vs Temperature

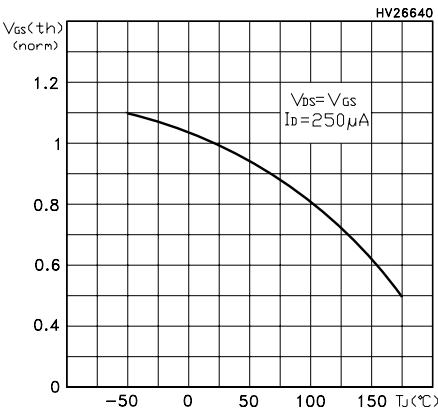


Figure 10. Normalized BVDSS vs Temperature

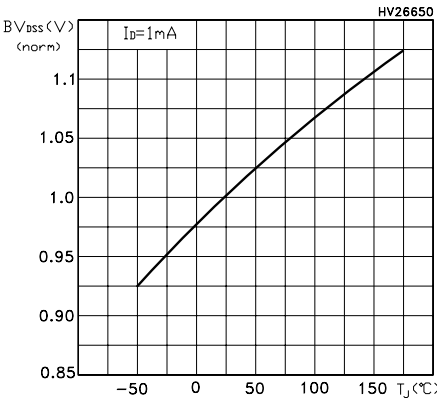


Figure 11. Normalized on Resistance vs Temperature

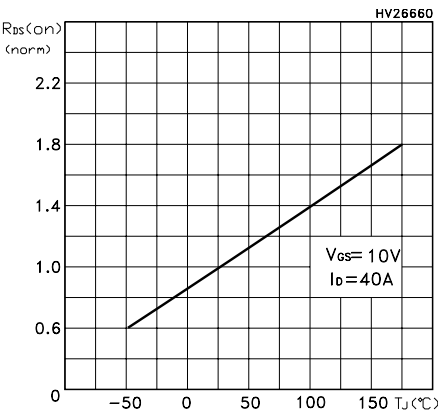


Figure 12. Source-Drain Diode Forward Characteristics

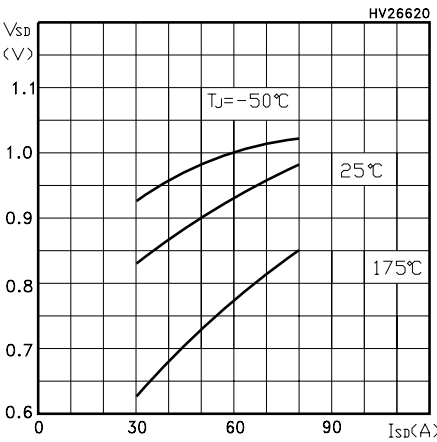
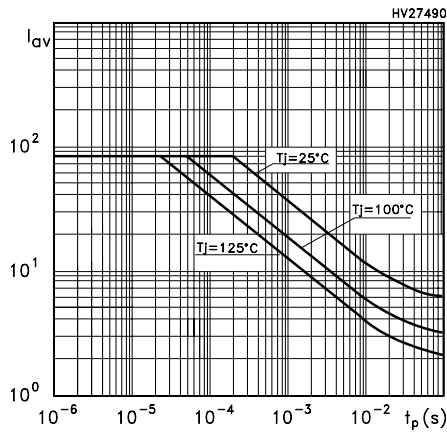


Figure 13. Allowable I_{AV} vs. Time in Avalanche

The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot BV_{DSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

3 Test Circuits

Figure 14. Switching Times Test Circuit For Resistive Load

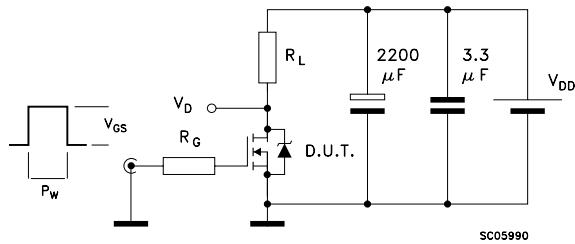


Figure 15. Gate Charge Test Circuit

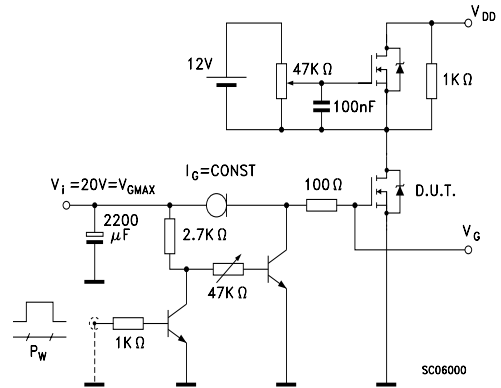
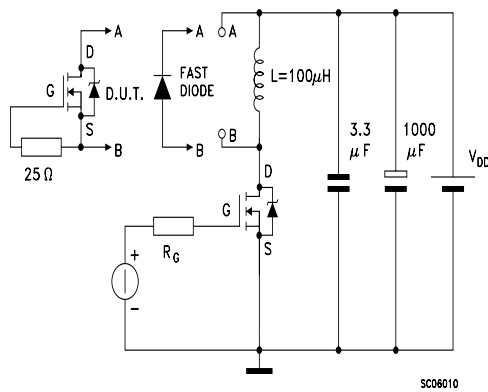


Figure 16. Test Circuit For Inductive Load Switching and Diode Recovery Times

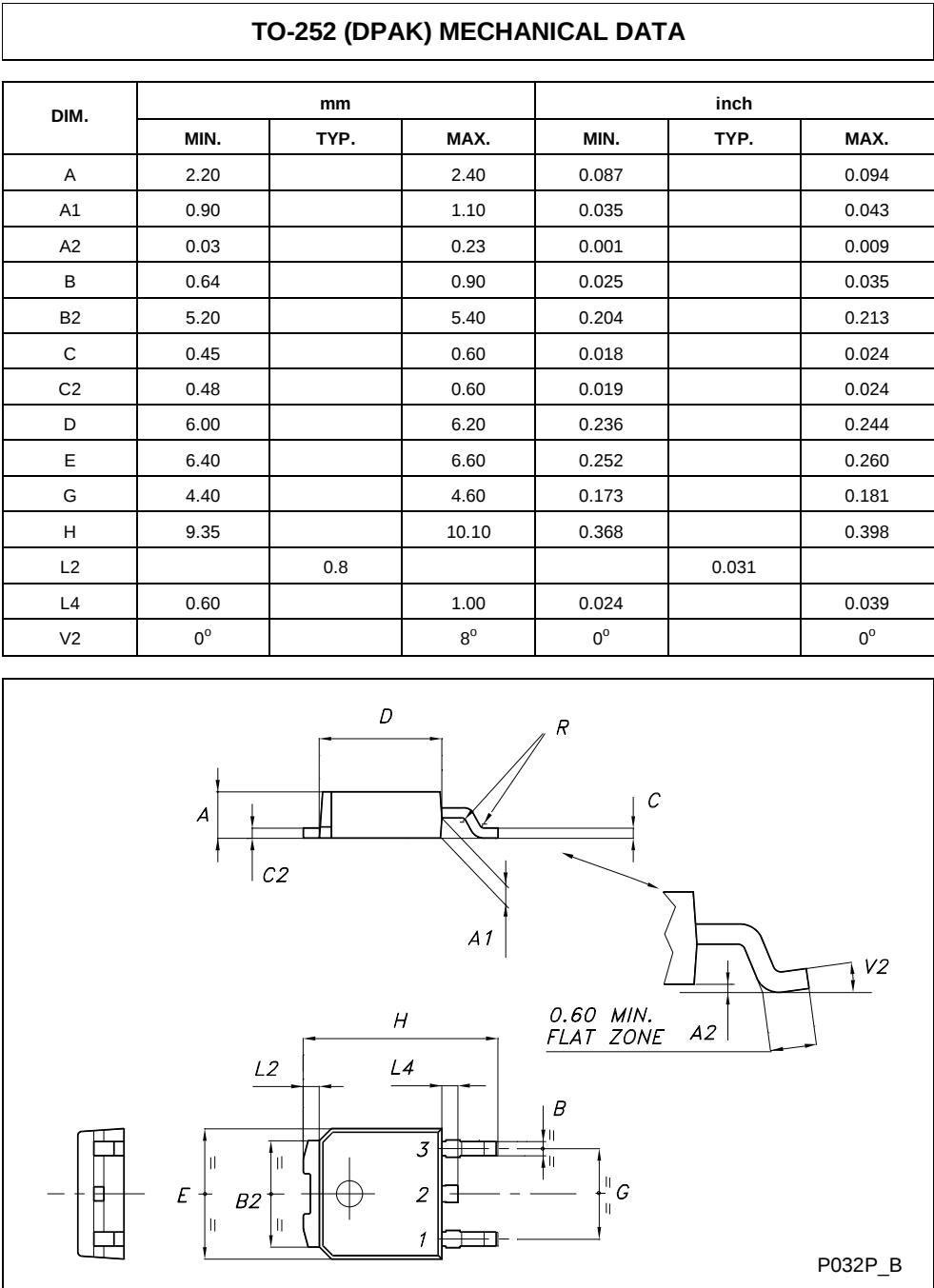


4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

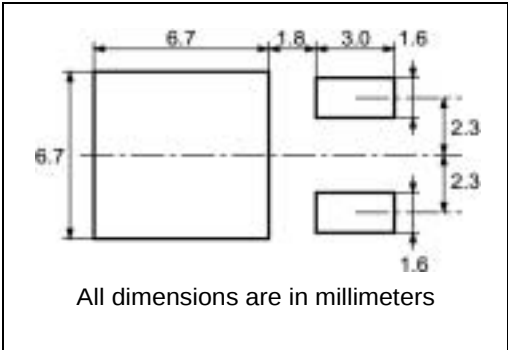
TO-251 (IPAK) MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

0068771-E

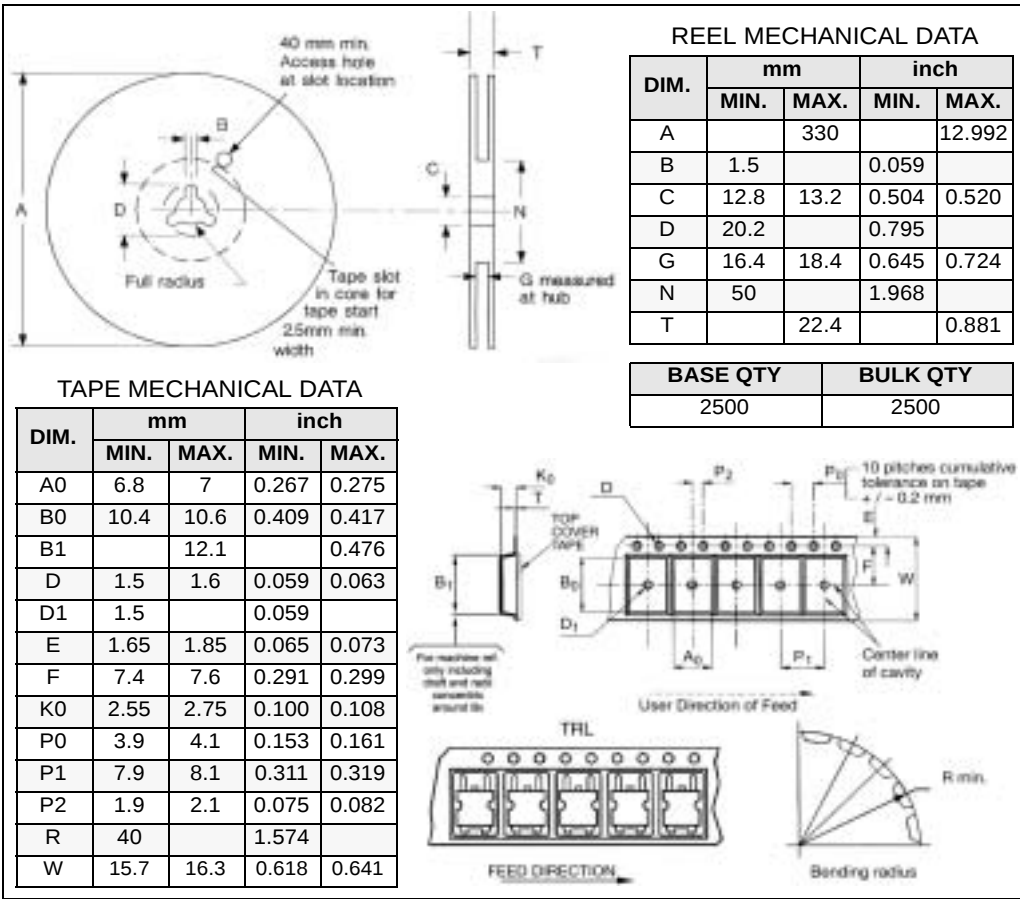


5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision History

Date	Revision	Changes
01-Sep-2005	1	Initial release.
14-Sep-2005	2	Value changed on Figure 1

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