DEMO CIRCUIT 1459A
QUICK START GUIDE

LTC3588EMSE-1
Piezoelectric Energy Harvesting Power Supply

DESCRIPTION

Demonstration Circuit 1459A is an energy harvesting power supply featuring the LTC3588-1. The LTC3588-1 integrates a low-loss full-wave bridge with a high efficiency buck converter to form a complete energy harvesting solution optimized for high output impedance energy sources such as piezoelectric transducers. An ultralow quiescent current undervoltage lockout mode with a wide hysteresis window allows charge to accumulate on an input capacitor until the buck converter can efficiently transfer a portion of the stored charge to the output. Four output voltages are pin selectable with up to 100mA of continuous output current. A power good comparator produces a logic high referenced to VOUT on the PGOOD pin when the converter reaches the programmed VOUT, signaling that the output is in regulation.

The LTC3588EMSE-1 is available in a 10-lead (3mm × 2mm) MSE surface mount package with exposed pad.

TABLE 1
PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN		MAX	UNITS
VIN	Input Voltage Range				18.0	V
VOUT 1.8V	Output Voltage Range	D0 = 0, D1=0	1.71	to	1.89	V
VOUT 2.5V	Output Voltage Range	D0 = 1, D1=0	2.425	to	2.575	V
VOUT 3.3V	Output Voltage Range	D0 = 0, D1=1	3.201	to	3.399	V
VOUT 3.6V	Output Voltage Range	D0 = 1, D1=1	3.491	to	3.708	V

OPERATING PRINCIPLE

Refer to the block diagram within the LTC3588-1 data sheet for its operating principle.

The LTC3588-1 is an ultralow quiescent current power supply designed specifically for energy harvesting and/or low current step-down applications. The part is designed to interface directly to a piezoelectric or alternative A/C energy source, rectify and store the harvested energy on an external capacitor, bleed off any excess energy via an internal shunt regulator, and maintain a regulated output voltage by means of a nano-power high efficiency synchronous buck regulator.

The LTC3588-1 has an internal full-wave bridge rectifier accessible via PZ1 and PZ2 that rectifies AC inputs such as those from a piezoelectric element. The rectified output is stored on a capacitor at the VIN pin and can be used as an energy reservoir for the buck converter. The bridge is capable of carrying up to 50mA.

When the voltage on VIN crosses the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. A wide (~1V) UVLO hysteresis window is employed with a lower threshold approximately 200mV above the selected regulated output voltage to prevent short cycling during buck power-up. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled.

Two internal rails, CAP and VIN2, are generated from VIN and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the VIN2 rail serves as logic high for output voltage select bits D0 and D1. The VIN2 rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below VIN. These are not intended to be used as external rails. Capacitors should be connected to the CAP and VIN2 pins to serve as energy reservoirs for driving the buck switches.

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the VOUT sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 250mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the buck output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA average load current when it is switching.

A power good comparator produces a logic high referenced to VOUT on the PGOOD pin the first time the converter reaches the programmed VOUT, signaling that the output is in regulation. The PGOOD pin will remain high until VOUT falls to 92% of the desired regulated voltage.

QUICK START PROCEDURE

Using short twisted pair leads for any power connections, with all loads and power supplies off, refer to Figure 1 for the proper measurement and equipment setup.

Follow the procedure below:

1. Before connecting PS1 to the DC1459A, PS1 must have its current limit set to 50mA. For most power supplies with a current limit adjustment feature the procedure to set the current limit is as follows. Turn the voltage and current adjustment to minimum. Short the outputs terminals and turn the voltage adjustment to maximum. Adjust the current limit to 50mA. Turn the voltage adjustment to minimum. The power supply is now current limited to 50mA.
2. Initial Jumper, PS and LOAD 1settings:
   JP1 = 0 **PS1** = OFF
   JP2 = 0 **LOAD1** = OFF
3. Connect PS1 to the VIN Terminals, then turn on PS1 and slowly increase voltage to 2.0V

while monitoring the input current. If the current remains less than 5mA, increase PS1 until output turns on. Verify input voltage, VIN, UVLO of 3.77V to 4.30V.

4. Increase PS1 to 12V and set LOAD1 to 100mA. Verify voltage on VOUT is within the VOUT 1.8V range in Table 1. Verify that the output ripple voltage is between 40mV and 70mV. Verify that PGOOD is high (VOUT). Decrease LOAD1 to 5mA.
5. Decrease PS1 to 0V and move the connection for PS1 from VIN to PZ1. Slowly increase PS1 voltage to 2.0V while monitoring the input current. If the current remains less than 5mA, increase PS1 to 12V. Verify voltage on VOUT is within the VOUT 1.8V range in Table 1.Decrease PS1 to 0V, swap the PZ1 move the lead connections to PZ2 and repeat the test. Decrease PS1 to 0V and move the connection for PS1 from PZ2 to VIN.
6. Set JP1 to 1. Increase PS1 to 12V and set LOAD1 to 100mA. Verify voltage on VOUT is within the VOUT 2.5V range in Table 1. Verify that the output ripple voltage is between 40mV to 70mV.
7. Set JP1 to 0 and JP2 to 1. Set LOAD1 to 100mA. Verify voltage on VOUT is within the VOUT 3.3V range in Table 1. Verify that the output ripple voltage is between 50mV and 80mV.
8. Set JP1 to 1 and JP2 to 1. Set LOAD1 to 100mA. Verify voltage on VOUT is within the VOUT 3.6V range in Table 1. Verify that the output ripple voltage is between 60mV and 90mV.
9. Increase PS1 to 18V and set LOAD1 to 100mA. Verify voltage on VOUT is within the VOUT 3.6V range in Table 1. Verify that the output ripple voltage is between 60mV and 90mV.
10. Decrease LOAD1 to 1mA. Turn off PS1 and insert a 1K ohm resistor between the positive lead of the PS1 and the VIN turret. Turn on PS1 and while monitoring the voltage on VIN, increase PS1 until the voltage on VIN is 3V below the voltage on PS1. Verify input voltage, VIN, V_{SHUNT} of 19.0V to 21.0V.
11. Turn off PS1 and LOAD1.

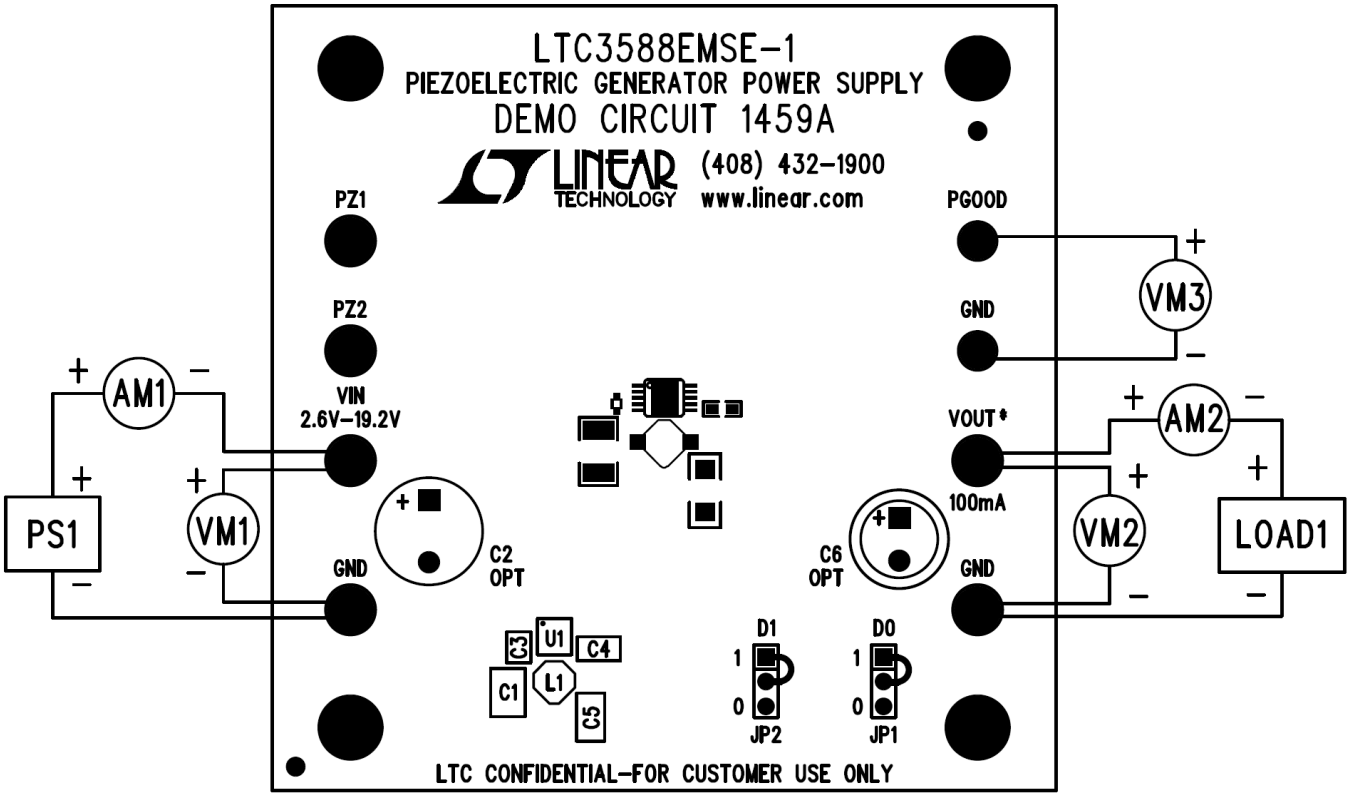

Figure 1. Proper Measurement Equipment Setup

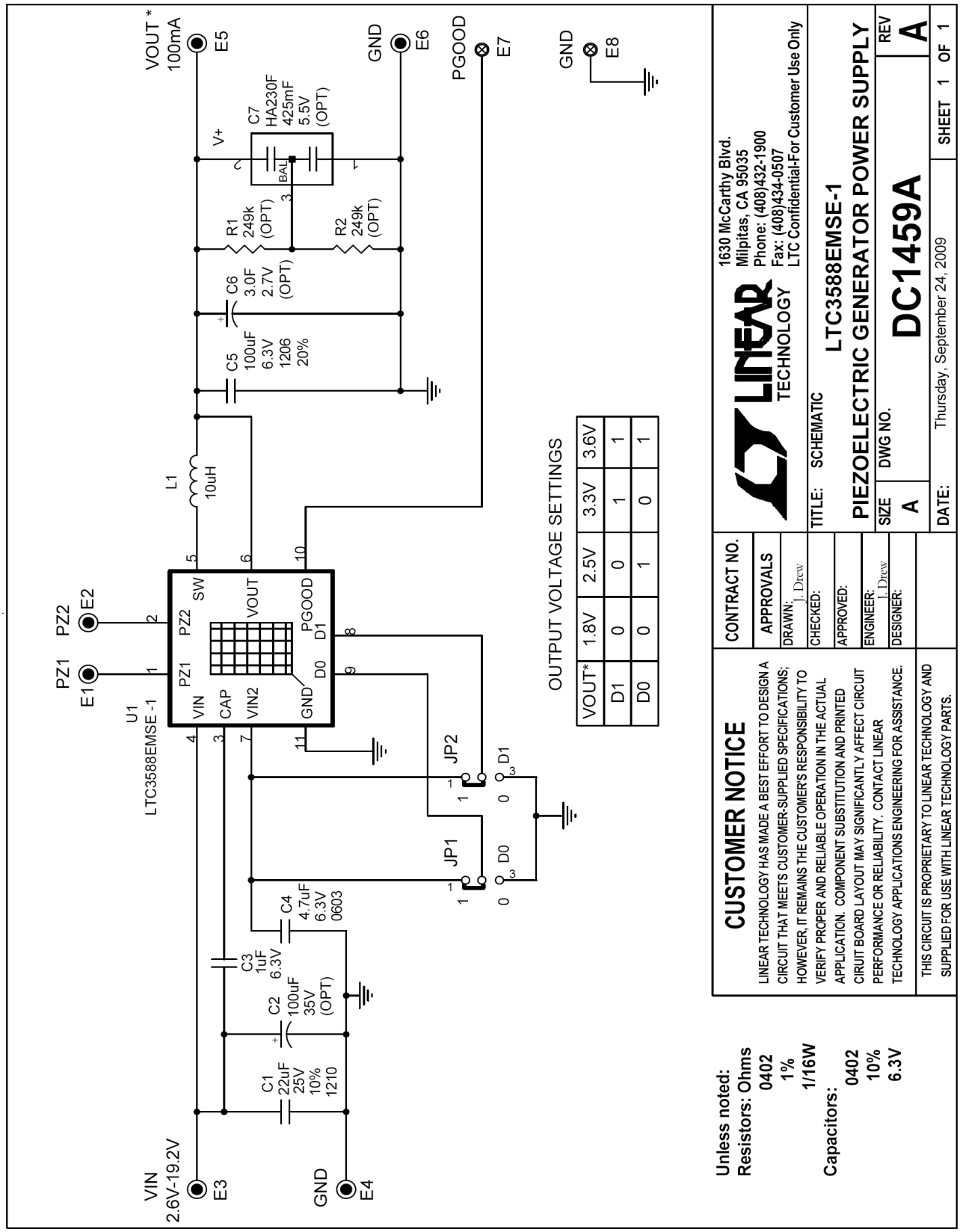

Figure 2: Schematic diagram

Item	Qty	Reference - Des	Part Description	Manufacturer, Part #
		REQUIRED CIRCUIT COMPONENTS:		
1	1	C1	CAP, CHIP, X5R, 22uF, 10%, 25V, 1210	AVX, 12103D226KAT1A
2	1	C3	CAP, CHIP, X5R, 1uF, 10%, 6.3V, 0402	TDK, C1005X5R0J105KT
3	1	C4	CAP, CHIP, X5R, 4.7uF, 10%, 6.3V, 0603	TDK, C1608X5R0J475KT
4	1	C5	CAP, CHIP, X5R, 100uF, 20%, 6.3V, 1206	Taiyo Yuden, JMK316BJ107ML-T
5	1	L1	INDUCTOR, 10UH , 0.43A, 180mΩ, 3mm x 3mm	Sumida, CDRH2D18/LDNP-100N
6	1	U1	Piezoelectric Generator Power Supply	Linear Tech.,LTC3588EMSE-1
		ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS:		
1	0	C2 (OPT)	AL ELECT, 100uF, 35V, 20%, 8.2mm x 11.mm	VISHAY, MAL291355101E3
2	0	C6 (OPT)	SUPERCAP, 3.0F, 2.7V, 8mm x 20mm	NESS, ESHSR-0003C0-002R7
3	0	C7 (OPT)	SUPERCAP, 0.43F, 5.5V, 20mm x 18mm	CAP-XX, HA230F
4	0	R1,R2 (OPT)	RES., CHIP, 249K, 1/16W, 1%, 0402	VISHAY, CRCW0402249KFKED
		HARDWARE FOR DEMO BOARD ONLY:		
1	6	E1,E2,E3,E4,E5,E6	TURRET, 0.09 DIA	MILL-MAX, 2501-2
2	2	E7,E8	TURRET, 0.061 DIA	MILL-MAX, 2308-2
3	2	JP1,JP2	HEADER, 3 PINS, 2mm	SAMTEC, TMM-103-02-L-S
4	2	JP1,JP2	SHUNT, 2MM	SAMTEC, 2SN-BK-G

Bill of Materials