E32D1EEC2K-76.800M TR

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REGULATORY COMPLIANCE (Data Sheet downloaded on Jan 9, 2018)

Lead Free COMPLIANT | EU RoHS 2011/65 + 2015/863 COMPLIANT | China RoHS COMPLIANT | REACH 163 SVHC COMPLIANT

Click badges to download compliance docs

Regulatory Compliance standards are subject to updates by governing bodies. Click the badges to download the latest compliance docs for this part number directly from Ecliptek.

DRC CONFLICT FREE

ITEM DESCRIPTION

Voltage Controlled Quartz Crystal Clock Oscillators VCXO LVPECL (PECL) 3.3Vdc 6 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 76.800MHz ±25ppm Maximum over 0°C to +70°C ±75ppm Minimum 10% Maximum

ELECTRICAL SPECIFICATIONS

Nominal Frequency	76.800MHz
Frequency Tolerance/Stability	±25ppm Maximum over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Supply Voltage	3.3Vdc ±5%
Input Current	100mA Maximum (With Load)
Output Voltage Logic High (Voh)	Vdd-1.025Vdc Minimum, 2.35Vdc Typical, Vdd-0.88Vdc Maximum
Output Voltage Logic Low (Vol)	Vdd-1.81Vdc Minimum, 1.60Vdc Typical, Vdd-1.62Vdc Maximum
Rise/Fall Time	1.5nSec Maximum (Measured over 20% to 80% of waveform)
Duty Cycle	50 ±5(%) (Measured at 50% of waveform)
Load Drive Capability	50 Ohms into Vdd-2.0Vdc
Output Logic Type	LVPECL
Control Voltage	1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)
Control Voltage Range	0.0Vdc to Vdd +0.5Vdc
Frequency Deviation	±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)
Linearity	10% Maximum
Transfer Function	Positive Transfer Characteristic
Modulation Bandwidth	10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)
Input Impedance	50kOhms Typical
Phase Noise	-55dBc/Hz at offset of 10Hz, -90dBc/Hz at offset of 100Hz, -120dBc/Hz at offset of 1kHz, -140dBc/Hz at offset of 10kHz, -145dBc/Hz at offset of 100kHz, -148dBc/Hz at offset of 1MHz (All Values are Typical)
Logic Control / Additional Output	Tri-State (Enable High) / Complementary Output
Tri-State Input Voltage (Vih and Vil)	Vih of 70% of Vdd Minimum or No Connect to Enable Output and Complementary Output, Vil of 30% of Vdd Maximum to Disable (High Impedance) Output and Complementary Output
RMS Phase Jitter	0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz; Random)
Accumulated Period Jitter (tacc)	4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution
Period Jitter (trj)	3pSec Typical, 5pSec Maximum Sigma of Random Jitter
Period Jitter (trms)	3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution
Period Jitter (tdj)	4pSec Typical, 10pSec Maximum Deterministic Jitter
Period Jitter (tp-p)	27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A
Gross Leak Test	MIL-STD-883, Method 1014 Condition C
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215

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ENVIRONMENTAL & MECHANICAL SPECIFICATIONS CONTINUED

Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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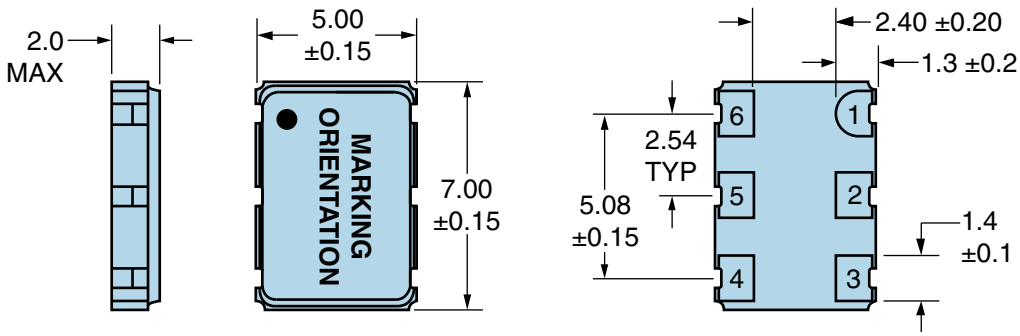
MECHANICAL DIMENSIONS (all dimensions in millimeters)

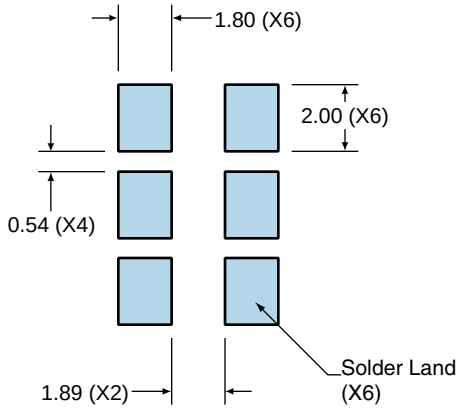


PIN	CONNECTION
1	Control Voltage
2	Tri-State
3	Case/Ground
4	Output
5	Complementary Output
6	Supply Voltage

LINE	MARKING
1	**ECLIPTEK**
2	**76.800M**
3	**XXXXX** *XXXXX=Ecliptek Manufacturing Identifier*

Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are ±0.1

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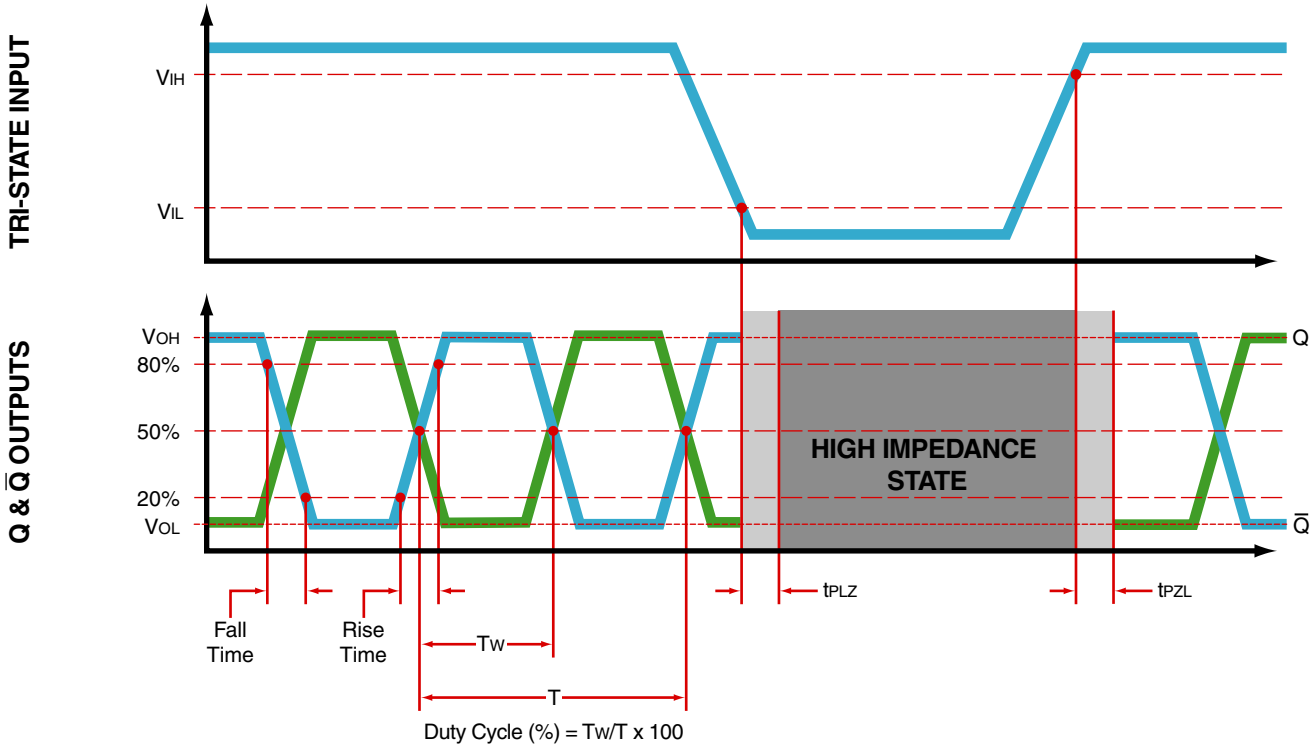
OUTPUT WAVEFORM & TIMING DIAGRAM



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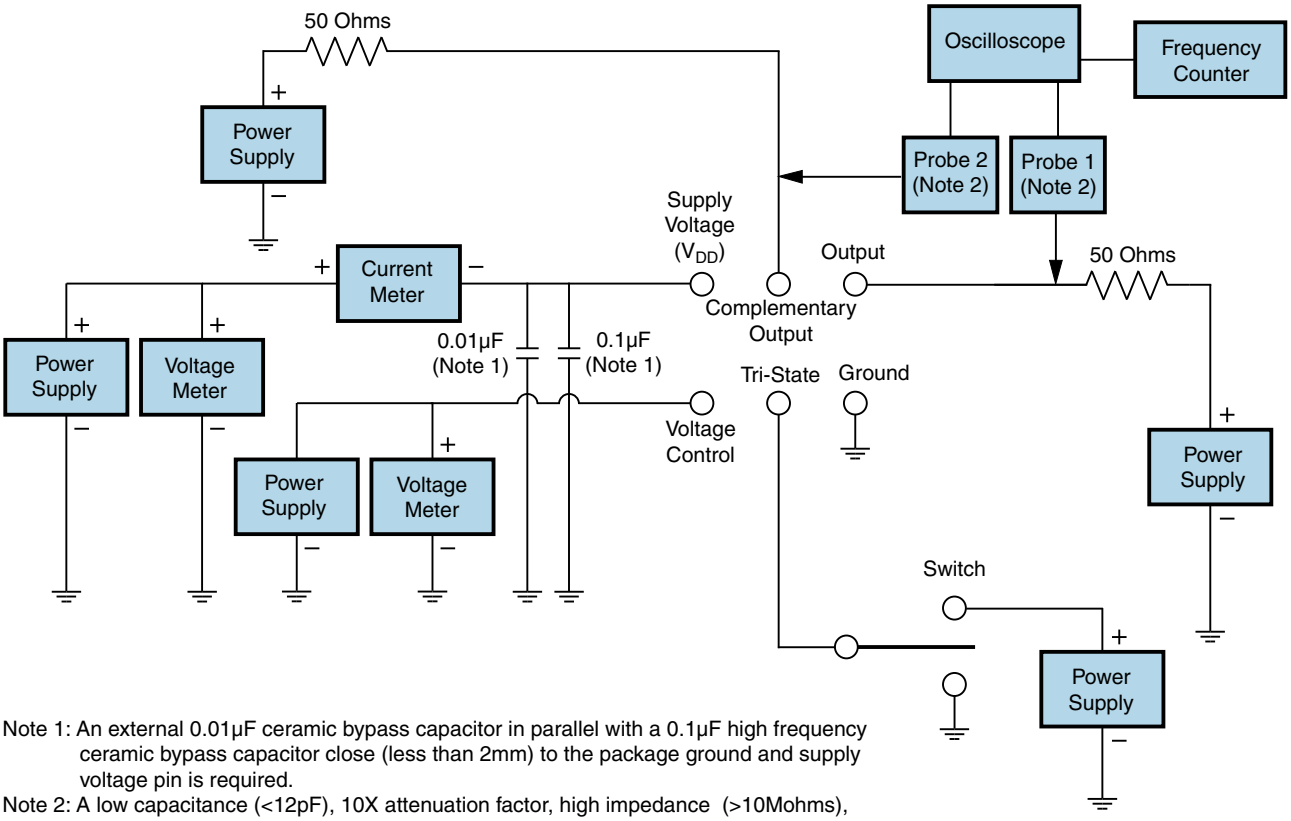
Test Circuit for Tri-State and Complementary Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>500MHz) passive probe is recommended.

Note 3: Test circuit PCB traces need to be designed for a characteristic line impedance of 50 ohms.

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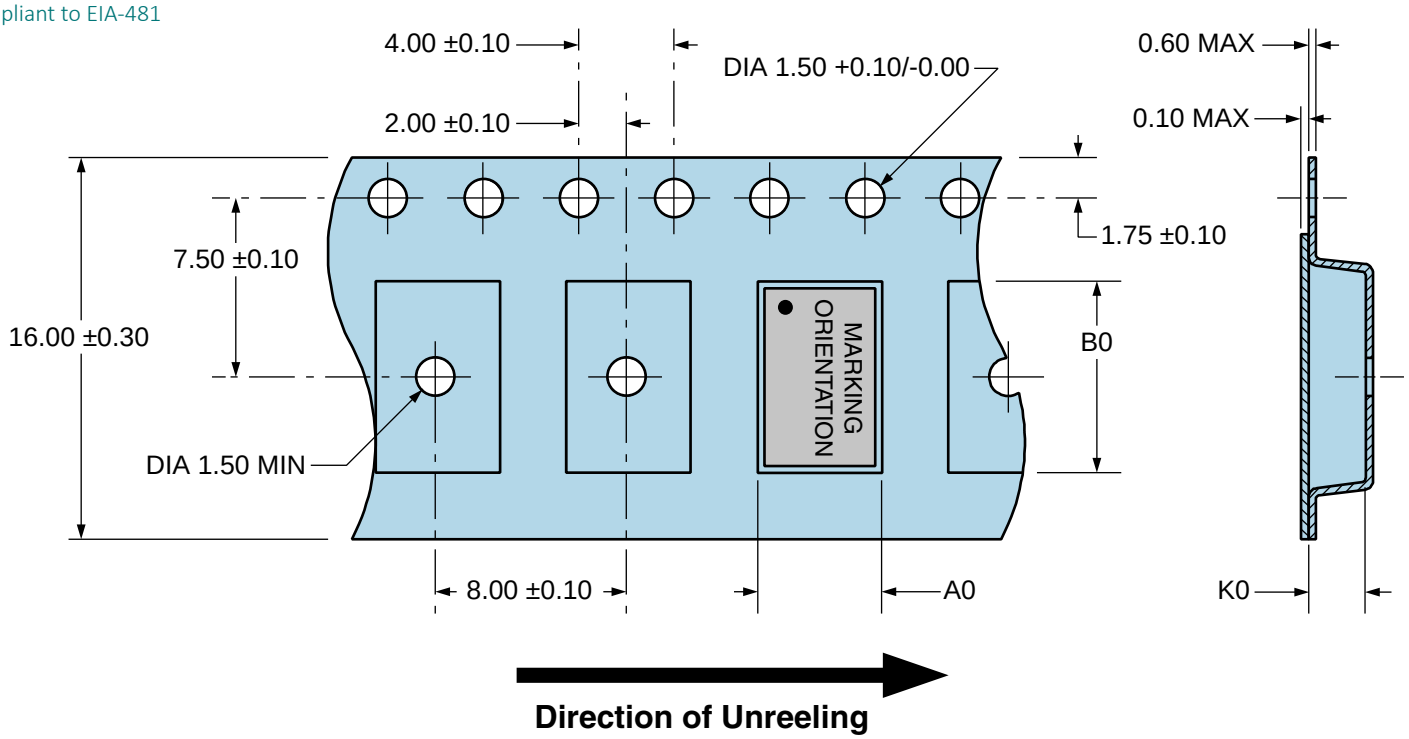
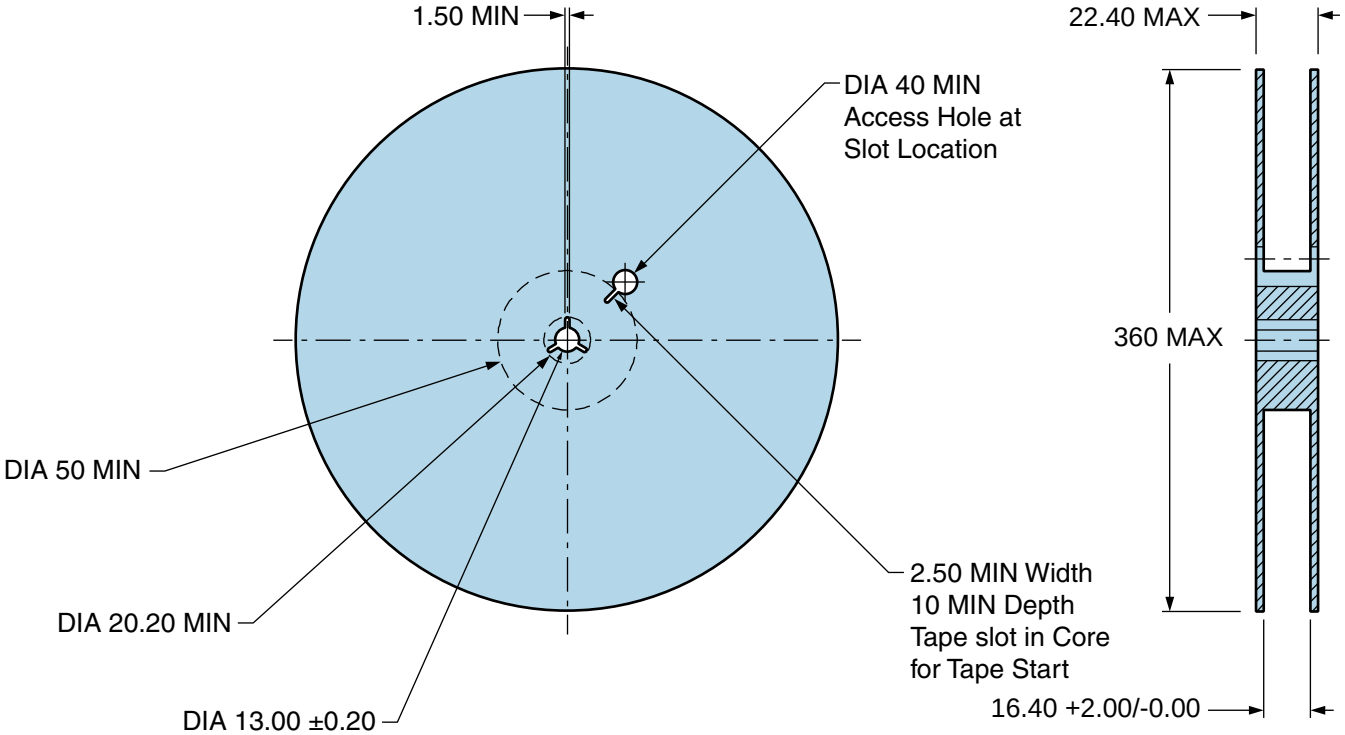
Tape & Reel Dimensions

Quantity Per Reel: 1,000 units

All Dimensions in Millimeters

Compliant to EIA-481





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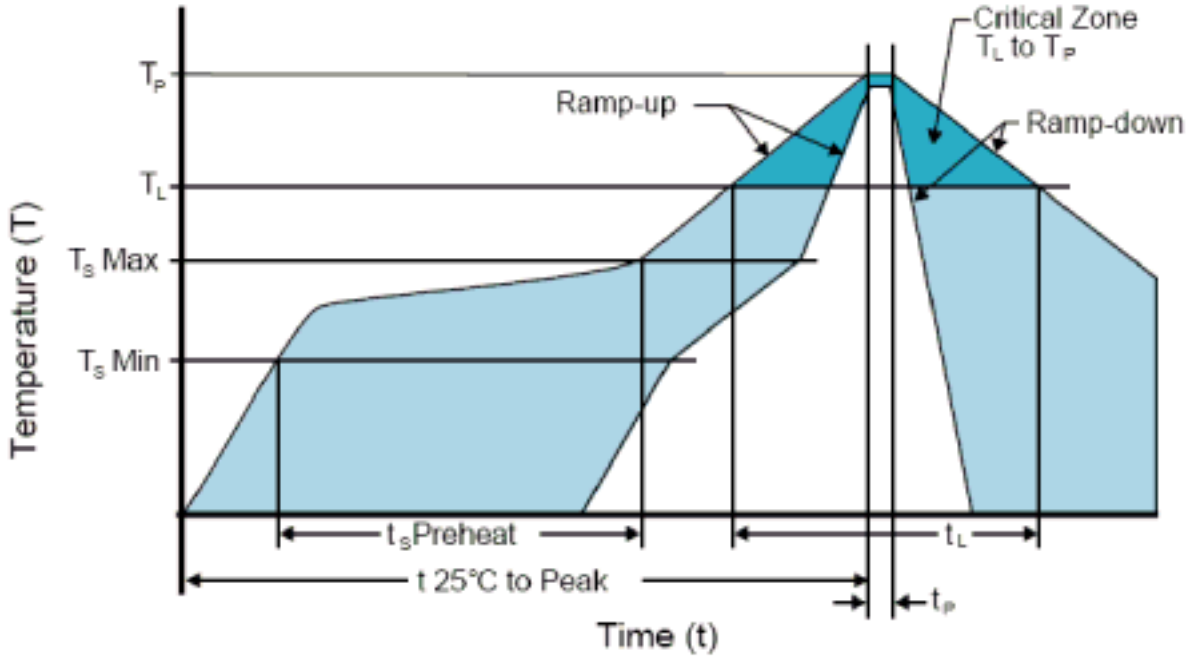
Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T_S MAX to T_L (Ramp-up Rate)	3°C/Second Maximum
Preheat	
- Temperature Minimum (T_S MIN)	150°C
- Temperature Typical (T_S TYP)	175°C
- Temperature Maximum (T_S MAX)	200°C
- Time (t_S MIN)	60 - 180 Seconds
Ramp-up Rate (T_L to T_P)	3°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	217°C
- Time (t_L)	60 - 150 Seconds
Peak Temperature (T_P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T_P Target)	250°C +0/-5°C
Time within 5°C of actual peak (t_p)	20 - 40 Seconds
Ramp-down Rate	6°C/Second Maximum
Time 25°C to Peak Temperature (t)	8 Minutes Maximum
Moisture Sensitivity Level	Level 1

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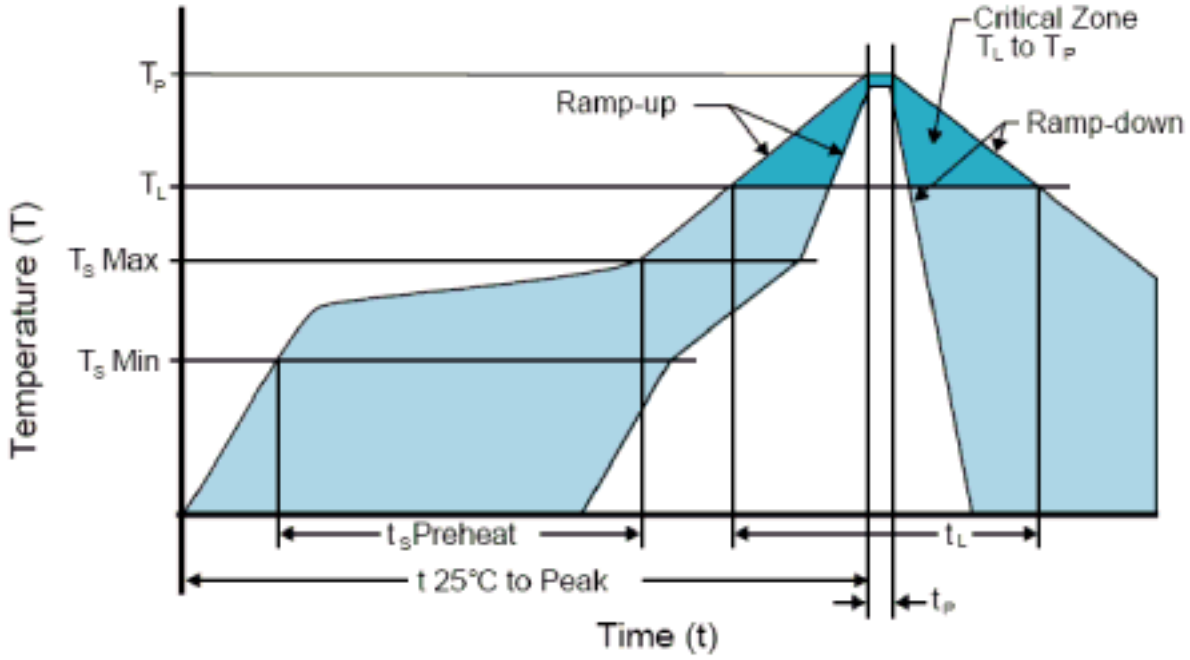
Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T_S MAX to T_L (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (T_S MIN)	N/A
- Temperature Typical (T_S TYP)	150°C
- Temperature Maximum (T_S MAX)	N/A
- Time (t_S MIN)	60 - 120 Seconds
Ramp-up Rate (T_L to T_P)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	150°C
- Time (t_L)	200 Seconds Maximum
Peak Temperature (T_P)	240°C Maximum
Target Peak Temperature (T_P Target)	240°C Maximum 2 Times / 230°C Maximum 1 Time
Time within 5°C of actual peak (t_p)	10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.

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