

2K I²C™ Serial EEPROM with Software Write Protect

Features

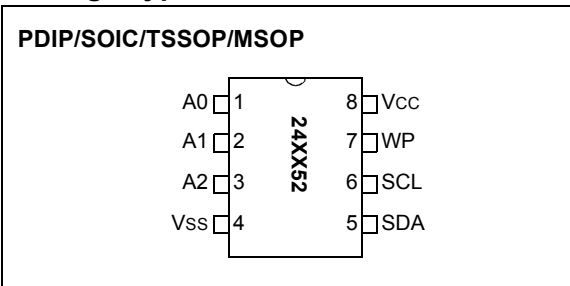
- Single supply with operation down to 1.8V
- Low power CMOS technology
 - 1 mA active current typical
 - 1 μ A standby current typical (I-temp)
- Organized as 1 block of 256 bytes (256 x 8)
- Software write protection for lower 128 bytes
- Hardware write protection for entire array
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA52) and 400 kHz (24LCS52) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 3.5 ms typical write cycle time for page-write
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP package
- Available for extended temperature ranges:
 - Industrial (I): -40°C to +85°C

Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA52	1.8-5.5	400 kHz ⁽¹⁾	I
24LCS52	2.5-5.5	400 kHz	I

Note 1: 100 kHz for Vcc < 2.5V

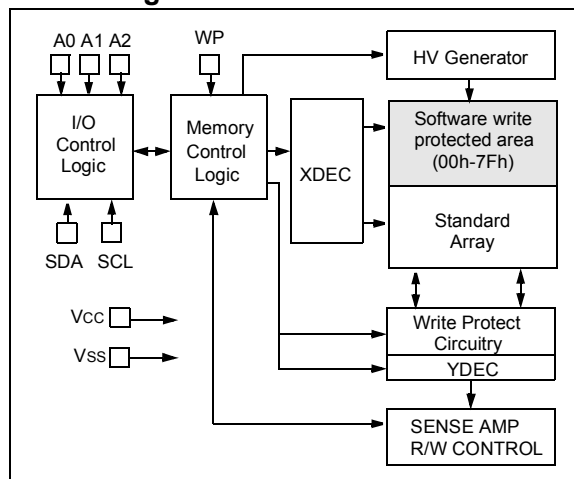
Package Types



Description

The Microchip Technology Inc. 24AA52/24LCS52 (24XX52*) is a 2 Kbit Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 5.5V). This device has a software write protect feature for the lower half of the array, as well as an external pin that can be used to write protect the entire array. The software write protect feature is enabled by sending the device a special command. Once this feature has been enabled, it cannot be reversed. In addition to the software protect feature, there is a WP pin that can be used to write protect the entire array, regardless of whether the software write protect register has been written or not. This allows the system designer to protect none, half or all of the array, depending on the application. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 1.8V, with standby and active currents of only 1 μ A and 1 mA respectively. The 24XX52 also has a page-write capability for up to 16 bytes of data. The 24XX52 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP and MSOP packages.

Block Diagram



*24XX52 is used in this document as a generic part number for the 24AA52/24LCS52 devices.

24AA52/24LCS52

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VCC.....	6.5V
All inputs and outputs w.r.t. VSS	-0.3V to VCC +1.0V
Storage temperature	-65°C to +150°C
Ambient temp. with power applied	-40°C to +125°C
ESD protection on all pins	≥ 4 kV

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC SPECIFICATIONS

DC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TAMB = -40°C to +85°C				
Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D1	VIH	A0, A1, A2, SCL, SDA and WP pins	—	—	—	—	—
D2	—	High level input voltage	0.7 VCC	—	—	V	—
D3	VIL	Low level input voltage	—	—	0.3 VCC	V	0.2 VCC for VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt trigger inputs	0.05 VCC	—	—	V	(Note)
D5	VOL	Low level output voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D6	ILI	Input leakage current	—	—	±10	mA	VIN = 0.1V to VCC
D7	ILO	Output leakage current	—	—	±10	µA	VOUT = 0.1V to VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.0V (Note) TAMB = 25°C, FCLK = 1 MHz
D9	ICC write	Operating current	—	1.0	3.0	mA	VCC = 5.5V, SCL = 400 kHz
D10	ICC read		—	0.20	1.0	mA	—
D11	ICCS	Standby current	—	0.36	1.0	µA	Industrial SDA = SCL = VCC A0, A1, A2, WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC SPECIFICATIONS

AC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TAMB = -40°C to +85°C				
Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
1	FCLK	Clock frequency	— —	— —	400 100	kHz	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
2	THIGH	Clock high time	600 4000	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
3	TLOW	Clock low time	1300 4700	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
4	TR	SDA and SCL rise time (Note 1)	— —	— —	300 1000	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
5	TF	SDA and SCL fall time	—	— —	300	ns	(Note 1)
6	THD:STA	START condition hold time	600 4000	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
7	TSU:STA	START condition setup time	600 4700	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
8	THD:DAT	Data input hold time	0	— —	—	ns	(Note 2)
9	TSU:DAT	Data input setup time	100 250	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
10	TSU:STO	STOP condition setup time	600 4000	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
11	TAA	Output valid from clock (Note 2)	— —	— —	900 3500	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	— —	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
13	TOF	Output fall time from VIH minimum to VIL maximum	20+0.1CB —	— —	250 250	ns	2.5V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
14	TSP	Input filter spike suppression (SDA and SCL pins)	—	—	50	ns	(Note 1 and Note 3)
15	TWC	Write cycle time (byte or page)	—	—	5	ms	—
16	—	Endurance	1M	—	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website: www.microchip.com.

24AA52/24LCS52

FIGURE 1-1: BUS TIMING DATA

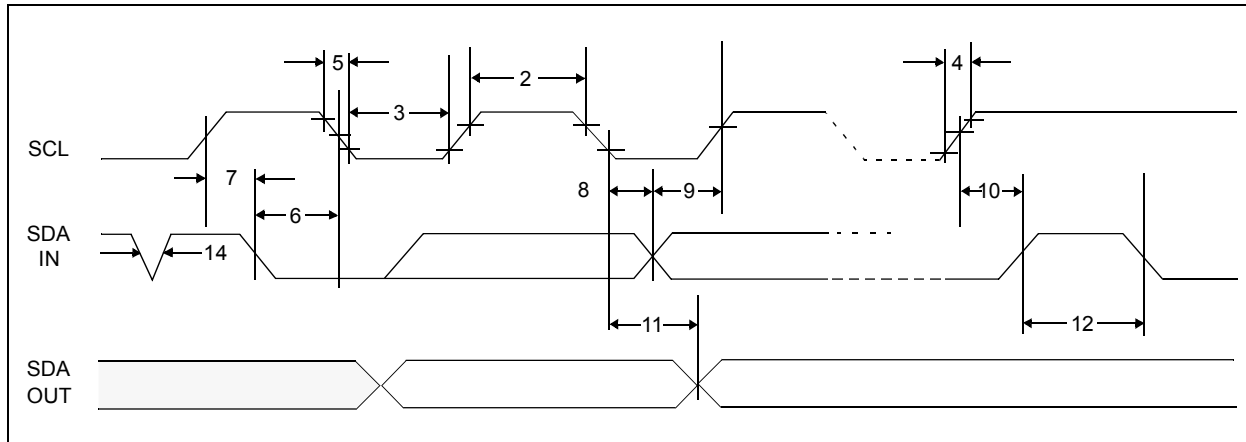
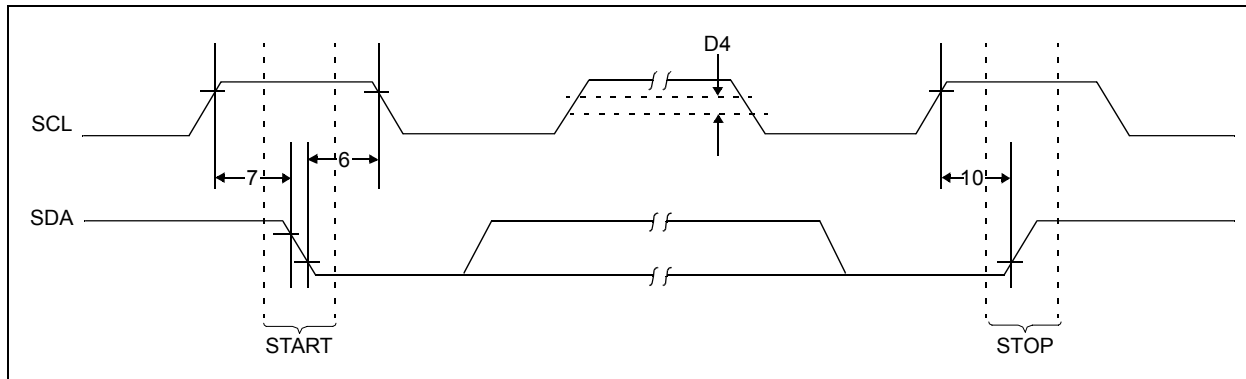


FIGURE 1-2: BUS TIMING START/STOP



2.0 FUNCTIONAL DESCRIPTION

The 24XX52 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus has to be controlled by a master device, which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions, while the 24XX52 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus Not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is determined by the master device and is, theoretically, unlimited; although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in, first-out (FIFO) fashion.

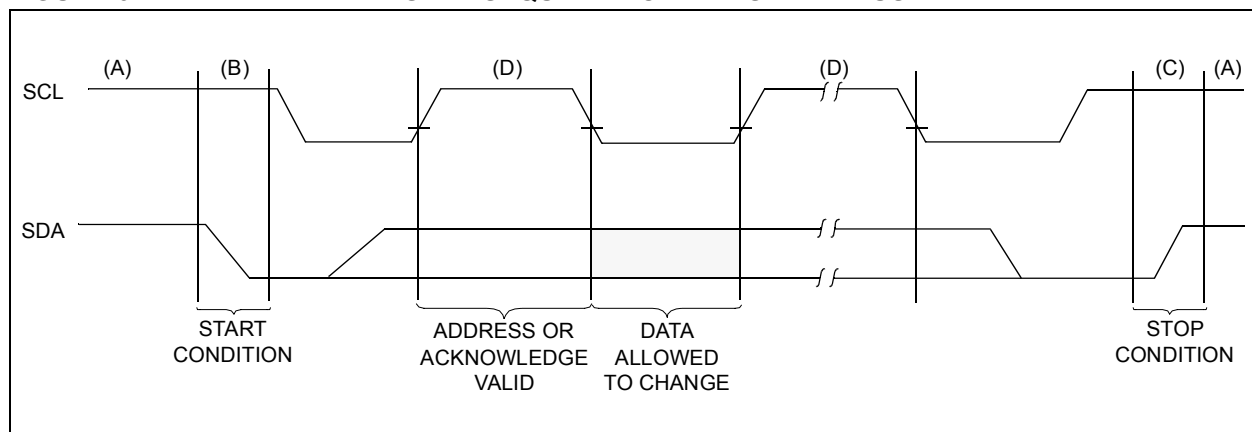
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

Note: The 24XX52 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX52) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



24AA52/24LCS52

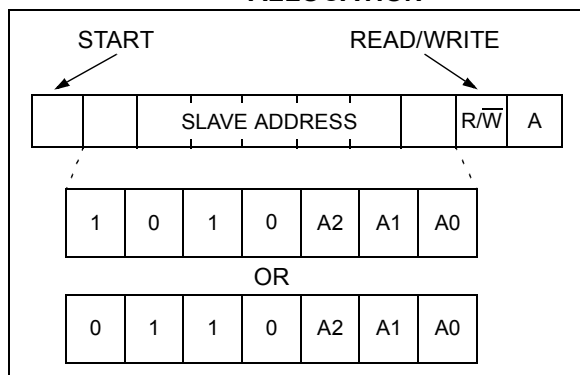
3.6 Device Addressing

A control byte is the first byte received following the START condition from the master device. The first part of the control byte consists of a 4-bit control code which is set to 1010 for normal read and write operations and 0110 for writing to the write protect register. The control byte is followed by three chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24XX52 devices on the same bus and are used to determine which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. The device will not acknowledge if you attempt a read command with the control code set to 0110.

The eighth bit of slave address determines if the master device wants to read or write to the 24XX52 (Figure 3-2). When set to a one, a read operation is selected. When set to a zero, a write operation is selected.

Operation	Control Code	Chip Select	R/W
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0
Set Write Protect Register	0110	A2 A1 A0	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATIONS

4.1 Byte Write

Following the start signal from the master, the device code (4 bits), the chip select bits (3 bits) and the R/W bit, which is a logic low, are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow once it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24XX52. After receiving another

acknowledge signal from the 24XX52, the master device will transmit the data word to be written into the addressed memory location. The 24XX52 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, which means that, during this time, the 24XX52 will not generate acknowledge signals (Figure 4-1). If an attempt is made to write to the array when the software or hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX52 in the same way as in a byte write. Instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24XX52, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. Upon receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 4-2). If an attempt is made to write to the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

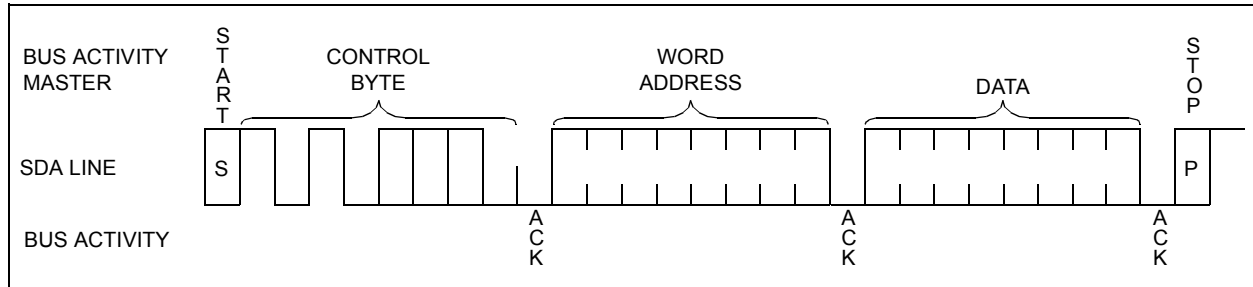
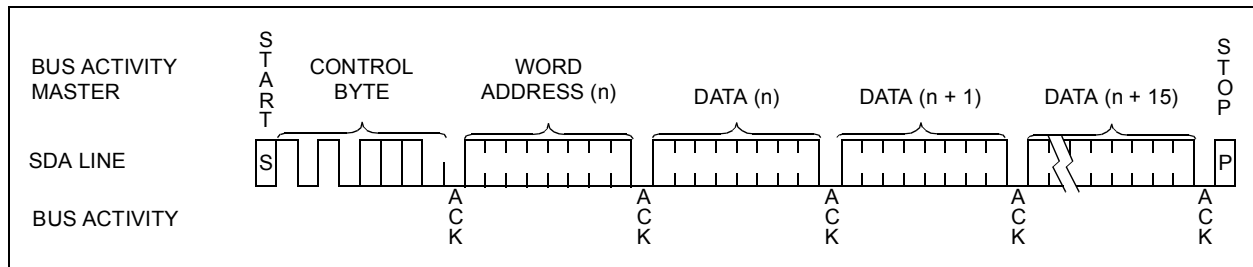


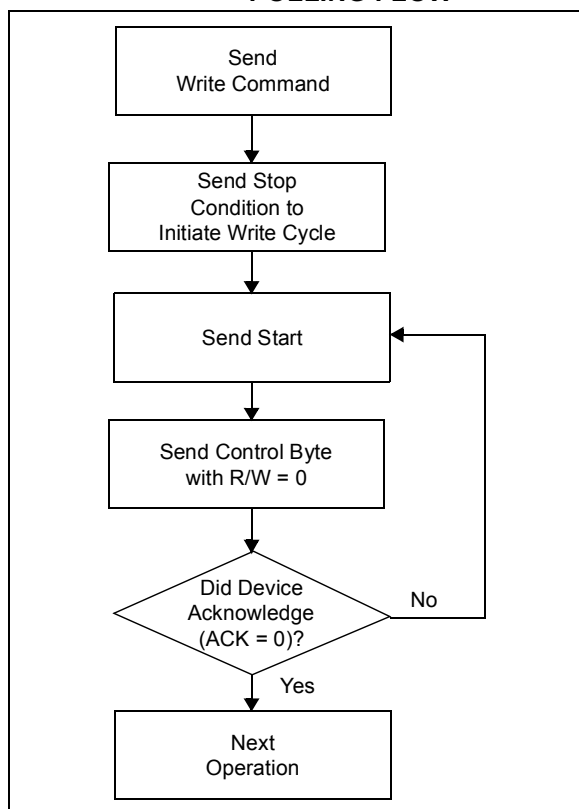
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24XX52 has a software write protect feature that allows the lower half of the array (addresses 00h - 7Fh) to be permanently write protected, as well as a WP pin that can be used to protect the entire array.

6.1 Software Write Protect

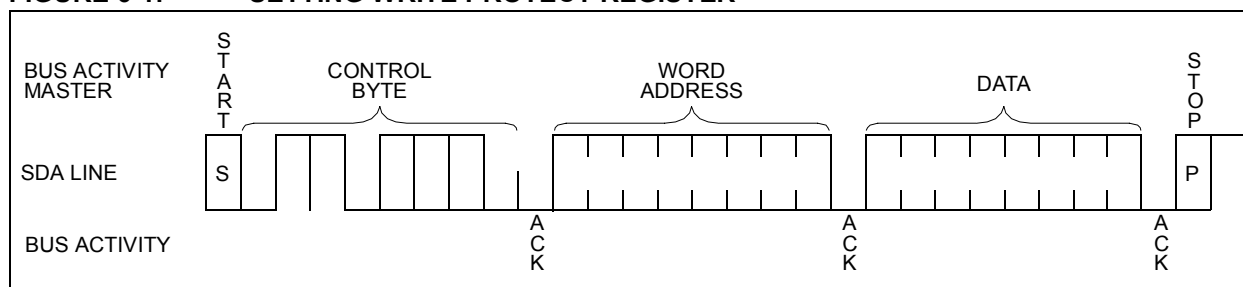
The software write protect feature is invoked by writing to the write protect register. This is done by sending a command similar to a normal write command. As shown in Figure 6-1, the write protect register is written by sending a write command with the slave address set to 0110 instead of 1010 and the address bits and data bits are don't cares. Once the software write protect register has been written, the device will not acknowledge the 0110 control byte.

Note: Once the software write protect register has been written, the write protection is enabled and cannot be reversed, even if the device is powered down.

6.2 Hardware Write Protect

The WP pin can be tied to VCC, VSS or can be left floating. If tied to VCC, the entire array will be write protected, regardless of whether the software write protect register has been written or not. If the WP pin is set to VCC, it will prevent the software write protect register from being written. If the WP is tied to VSS or left floating, then write protection is determined by the status of the software write protect register.

FIGURE 6-1: SETTING WRITE PROTECT REGISTER



7.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the $\overline{R/\overline{W}}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24XX52 contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous access (either a read or write operation) was to address n , the next current address read operation would access data from address $n+1$. Upon receipt of the slave address with $\overline{R/\overline{W}}$ bit set to '1', the 24XX52 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24XX52 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24XX52 as part of a write operation. Once the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the $\overline{R/\overline{W}}$ bit set to a '1'. The 24XX52 then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the 24XX52 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read, with the exception that after the 24XX52 transmits the first data byte, the master issues an acknowledge, as opposed to a STOP condition in a random read. This directs the 24XX52 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads, the 24XX52 contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Contiguous Addressing Across Multiple Devices

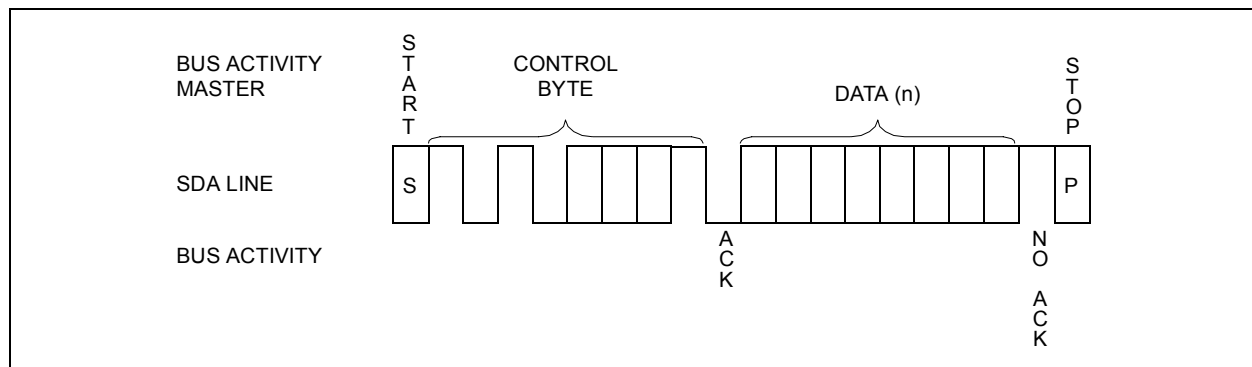
The chip select bits (A2, A1, A0) can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24XX52 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9 and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

7.5 Noise Protection and Brown Out

The 24XX52 employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5V at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ



24AA52/24LCS52

FIGURE 7-2: RANDOM READ

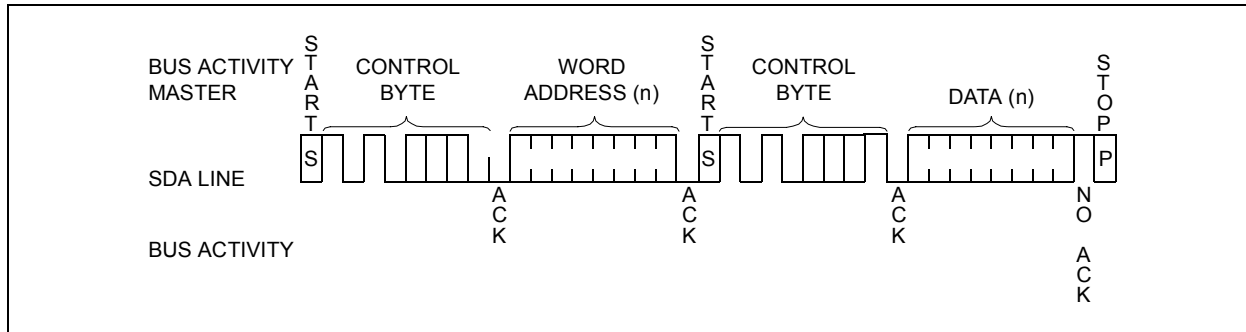
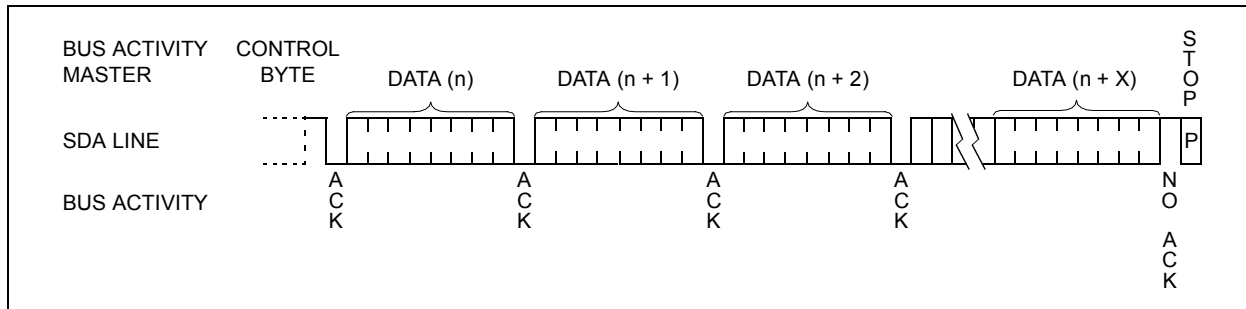


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 8-1.

TABLE 8-1: PIN FUNCTION TABLE

Symbol	PDIP	SOIC	TSSOP	MSOP	Description
A0	1	1	1	1	Chip Address Input
A1	2	2	2	2	Chip Address Input
A2	3	3	3	3	Chip Address Input
Vss	4	4	4	4	Ground
SDA	5	5	5	5	Serial Address/Data I/O
SCL	6	6	6	6	Serial Clock
WP	7	7	7	7	Write Protect Input
Vcc	8	8	8	8	+1.8V to 5.5V Power Supply

8.1 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24XX52 devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vss or Vcc.

8.2 Serial Address/Data Input/Output (SDA)

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 k Ω for 100 kHz, 2 k Ω for 400 kHz).

For normal data transfer, SDA, is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

8.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

8.4 Write-Protect (WP)

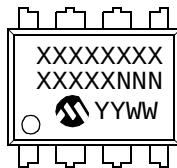
This is the hardware write protect pin. It can be tied to Vcc, Vss or be left floating. If tied to Vcc, the hardware write protection is enabled. If the WP pin is tied to Vss, the hardware write protection is disabled. If the WP pin is left floating, an internal pull down logic will pull the WP pin to Vss and the hardware write protection will be disabled.

24AA52/24LCS52

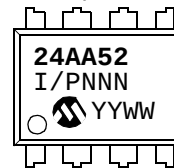
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

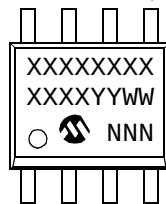
8-Lead PDIP (300 mil)



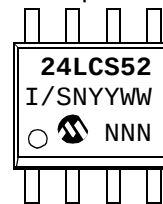
Example:



8-Lead SOIC (150 mil)



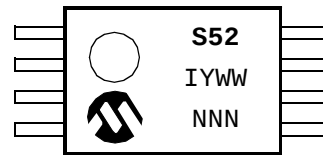
Example:



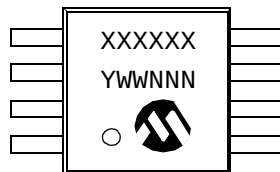
8-Lead TSSOP



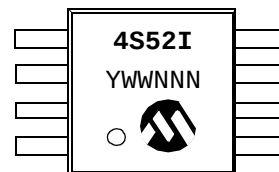
Example:



8-Lead MSOP



Example:

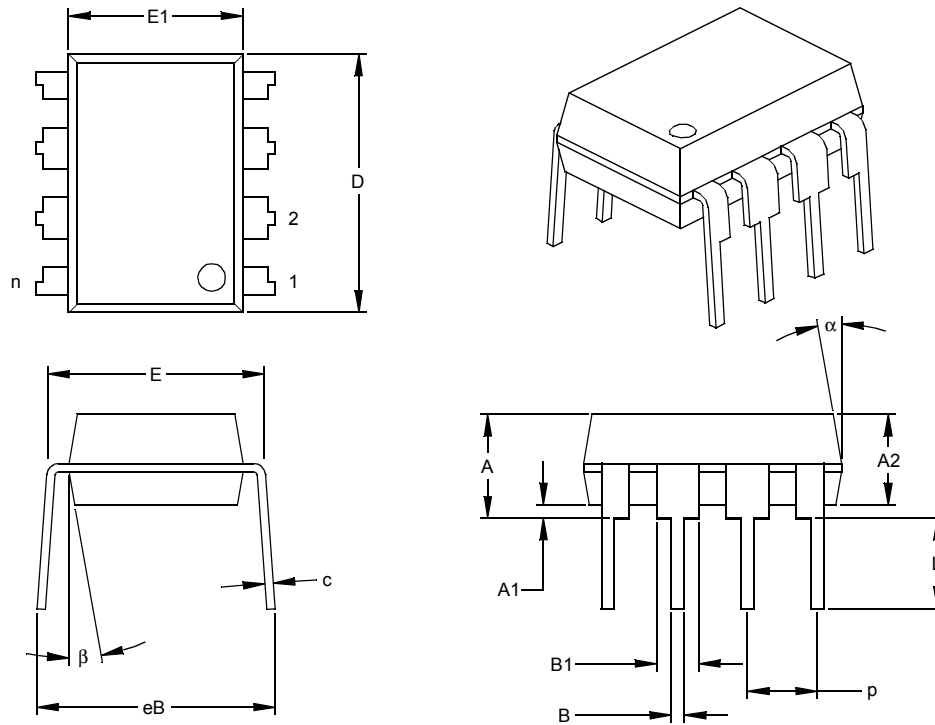


Legend: XX...X Customer specific information*
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

*Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

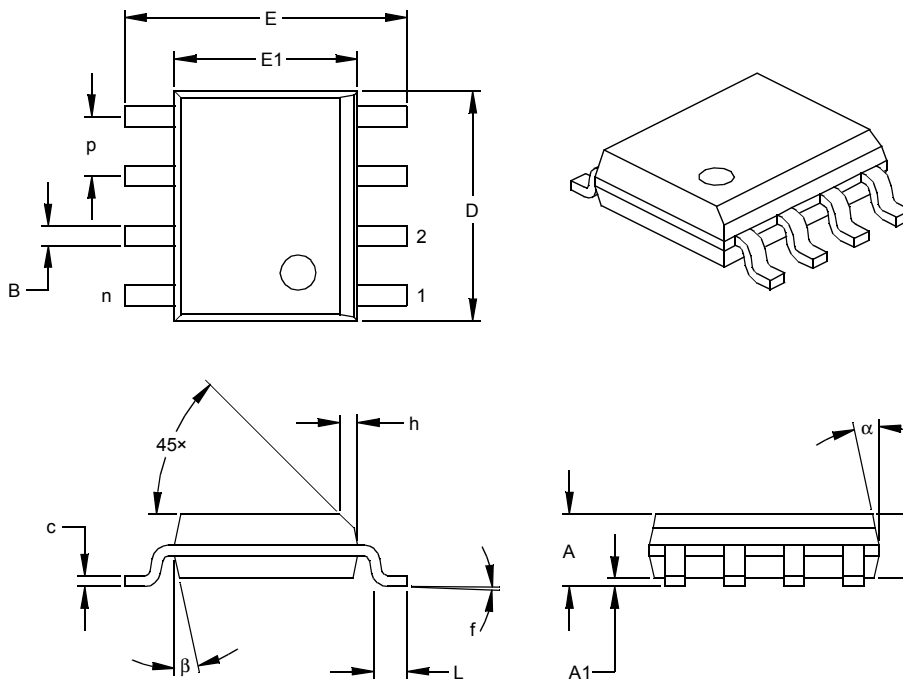
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

24AA52/24LCS52

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

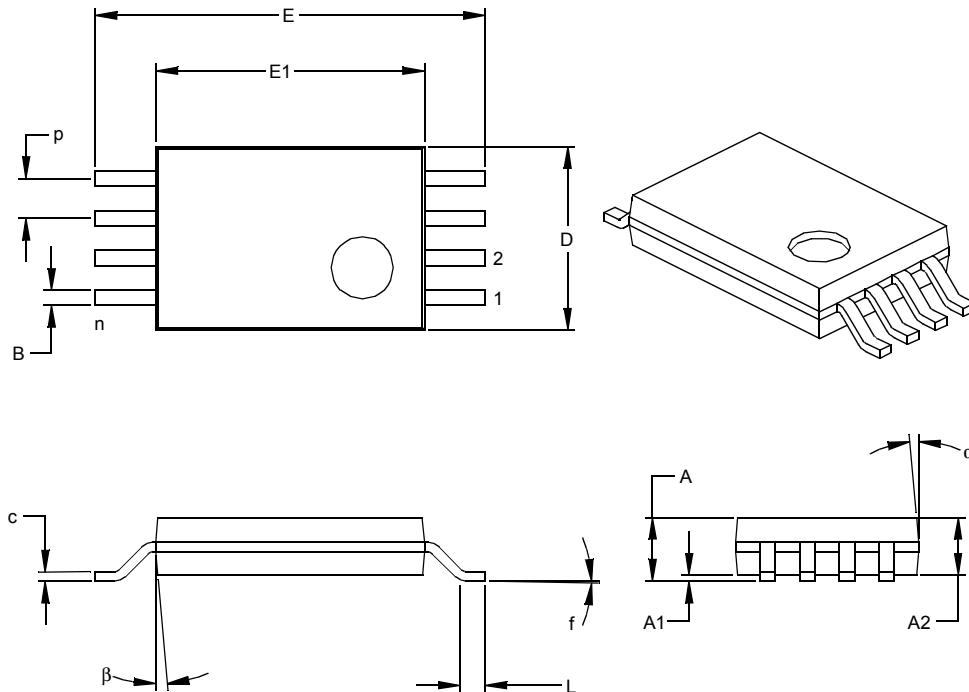
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

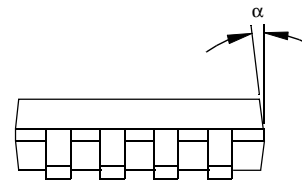
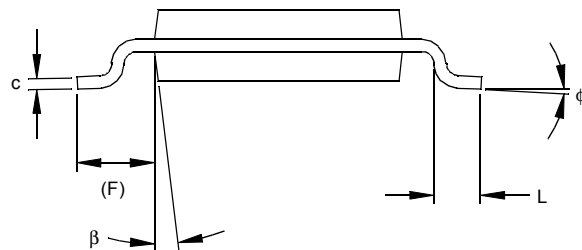
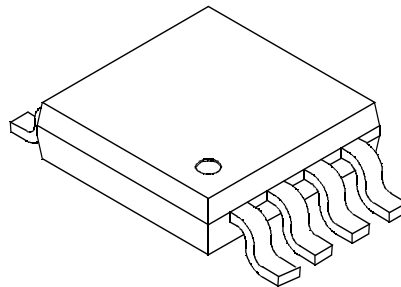
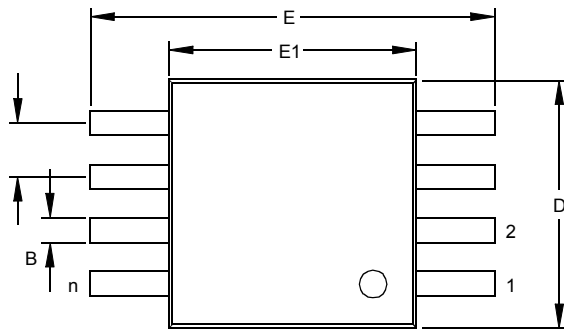
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-086

24AA52/24LCS52

8-Lead Plastic Micro Small Outline Package (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p	.026			0.65		
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

<ftp://ftp.microchip.com>

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

013001

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager
RE: Reader Response
From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (____) _____ - _____ FAX: (____) _____ - _____

Application (optional):

Would you like a reply? ____Y ____N

Device: **24AA52/24LCS52** Literature Number: **DS21166F**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.		X	/XX
Device	Temperature Range		Package
Device: 24AA52: = 1.8V, 2 Kbit I²C Serial EEPROM 24AA52T: = 1.8V, 2 Kbit I²C Serial EEPROM (Tape and Reel) 24LCS52: = 2.5V, 2 Kbit I²C Serial EEPROM 24LCS52T: = 2.5V, 2 Kbit I²C Serial EEPROM (Tape and Reel)			
Temperature Range:		= -40°C to +85°C	
Package:		- P = Plastic DIP (300 mil body), 8-lead - SN = Plastic SOIC (150 mil body), 8-lead - ST = Plastic TSSOP (4.4 mm), 8-lead - MS = Plastic Micro Small Outline (MSOP), 8-lead	
		Examples: a) 24AA52-I/P: Industrial Temperature, PDIP package b) 24AA52-I/SN: Industrial Temperature, SOIC package c) 24AA52T-I/MS: Tape and Reel, Industrial Temperature, MSOP package a) 24LCS52-I/P: Industrial Temperature, PDIP package b) 24LCS52-I/SN: Industrial Temperature, SOIC package c) 24LCS52T-I/MS: Tape and Reel, Industrial Temperature, MSOP package	

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

24AA52/24LCS52

NOTES:

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

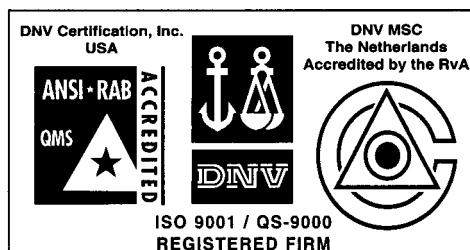
dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hof 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

05/01/02

