

Product Summary

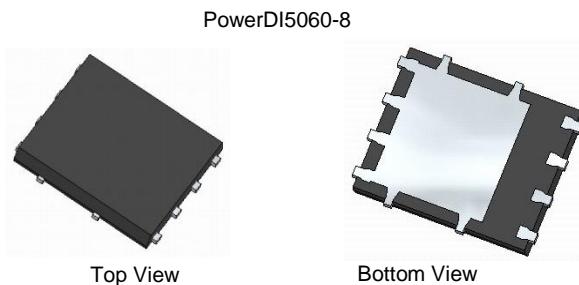
BV_{DSS}	$R_{DS(ON)}$	I_D $T_c = +25^\circ C$
$-20V$	$2.2m\Omega$ @ $V_{GS} = -10V$	-150A
	$2.55m\Omega$ @ $V_{GS} = -4.5V$	-120A
	$4.0m\Omega$ @ $V_{GS} = -2.5V$	-90A

Description

This new generation MOSFET is designed to minimize $R_{DS(ON)}$ and yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

Applications

- Switch

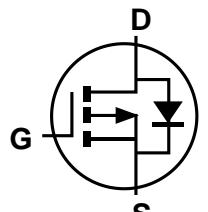


Features

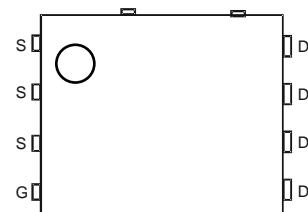
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- $<1.1mm$ Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

- Case: PowerDI® 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208③
- Weight: 0.097 grams (Approximate)



Internal Schematic



Top View
Pin Configuration

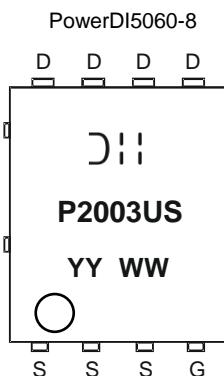
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2003UPS-13	PowerDI5060-8	2,500 / Tape & Reel

Notes:

1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



DII = Manufacturer's Marking
 P2003US = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 17 = 2017)
 WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	± 12	V
Continuous Drain Current, $V_{GS} = -10\text{V}$ (Note 7)	$T_C = +25^\circ\text{C}$ $T_C = +70^\circ\text{C}$	I_D	-150 -120	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)		I_{DM}	-350	A
Maximum Continuous Body Diode Forward Current (Note 7)		I_S	-120	A
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)		I_{SM}	-350	A
Avalanche Current, $L = 0.1\text{mH}$ (Note 8)		I_{AS}	-32	A
Avalanche Energy, $L = 0.1\text{mH}$ (Note 8)		E_{AS}	67	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.4	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	90	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 6)		P_D	2.7	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	46	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 7)		P_D	80	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	1.5	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	-0.5	—	-1.4	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	1.7	2.2	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -25\text{A}$
		—	1.9	2.55		$V_{GS} = -4.5\text{V}, I_D = -20\text{A}$
		—	2.5	4.0		$V_{GS} = -2.5\text{V}, I_D = -15\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.6	-1.1	V	$V_{GS} = 0\text{V}, I_S = -5\text{A}$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	8352	—	pF	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	1406	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	599	—	pF	
Gate Resistance	R_g	—	13.2	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_g	—	79	—	nC	$V_{DS} = -10\text{V}, I_D = -20\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_g	—	177	—	nC	
Gate-Source Charge	Q_{gs}	—	14.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	19.8	—	nC	
Turn-On Delay Time	$t_{D(\text{ON})}$	—	7.8	—	ns	
Turn-On Rise Time	t_R	—	4.9	—	ns	$V_{DD} = -10\text{V}, V_{GEN} = -4.5\text{V}, R_{GEN} = 1\Omega, I_D = -10\text{A}$
Turn-Off Delay Time	$t_{D(\text{OFF})}$	—	377	—	ns	
Turn-Off Fall Time	t_F	—	189	—	ns	
Reverse Recovery Time	t_{RR}	—	49	—	ns	$I_F = -10\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	39	—	nC	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

7. Thermal resistance from junction to soldering point (on the exposed drain pad).

8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.

9. Short duration pulse test used to minimize self-heating effect.

10. Guaranteed by design. Not subject to product testing.

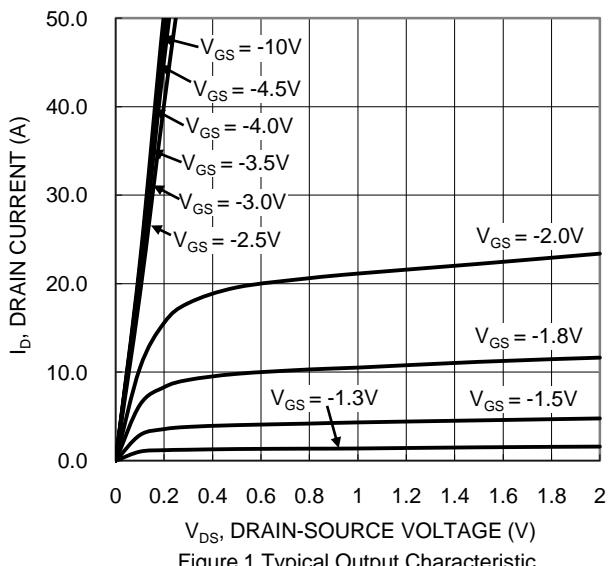


Figure 1. Typical Output Characteristic

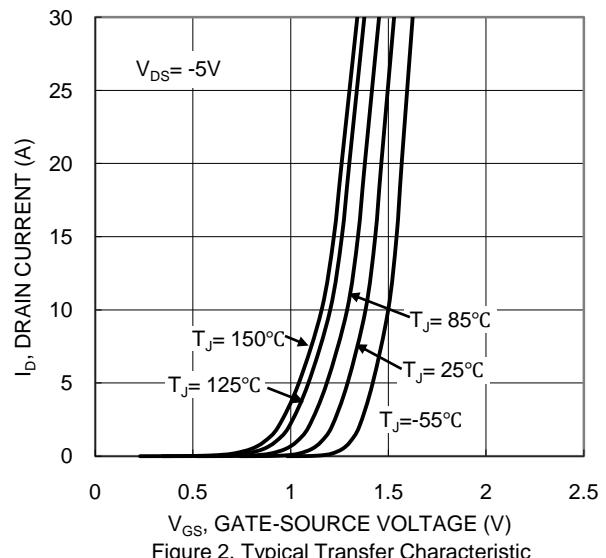


Figure 2. Typical Transfer Characteristic

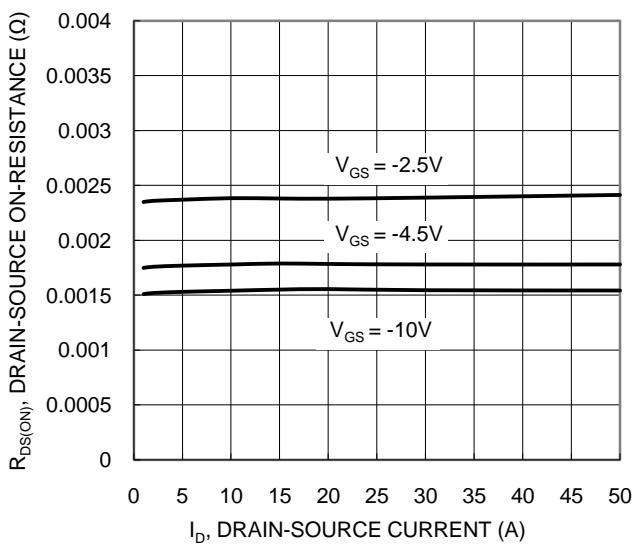


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

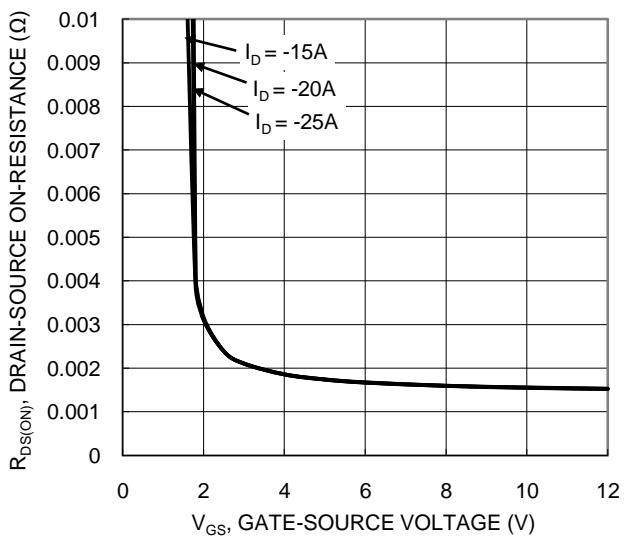


Figure 4. Typical Transfer Characteristic

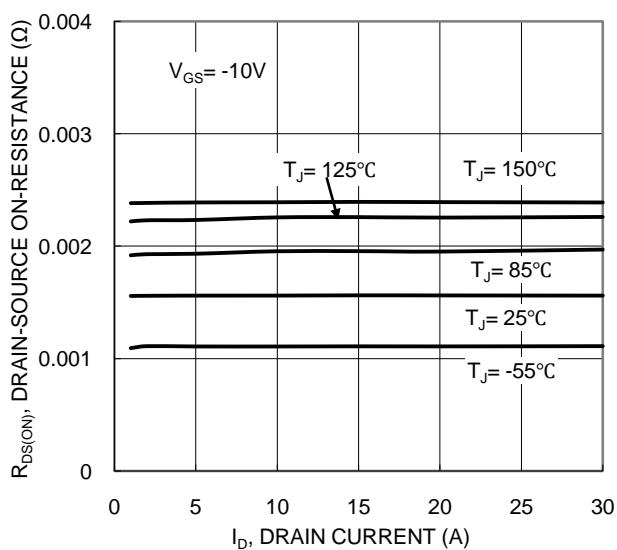


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

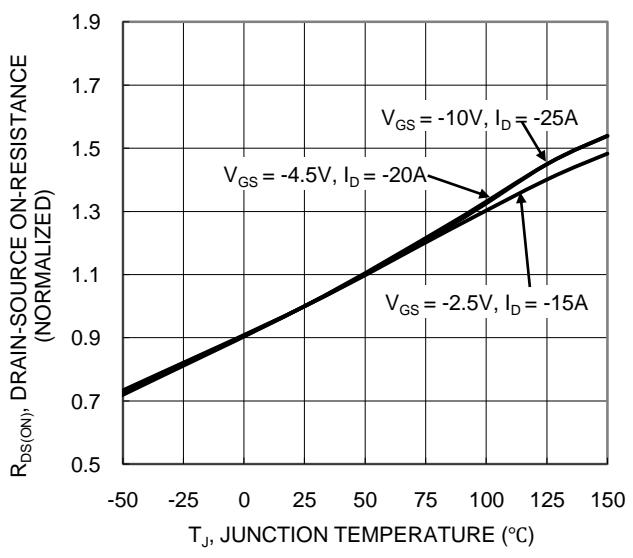


Figure 6. On-Resistance Variation with Junction Temperature

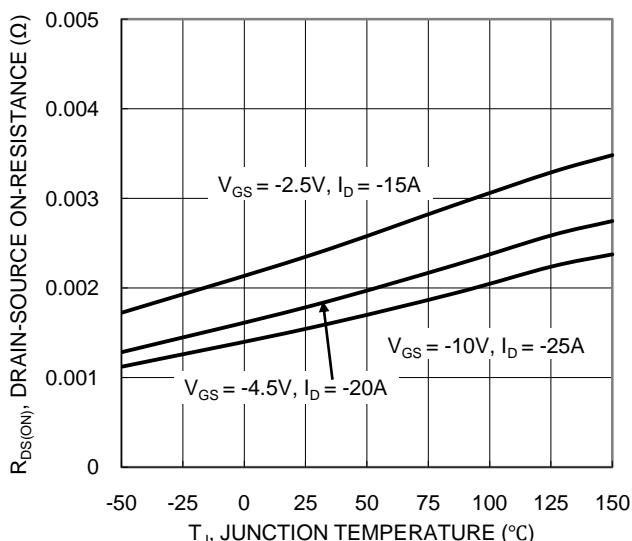


Figure 7. On-Resistance Variation with Junction Temperature

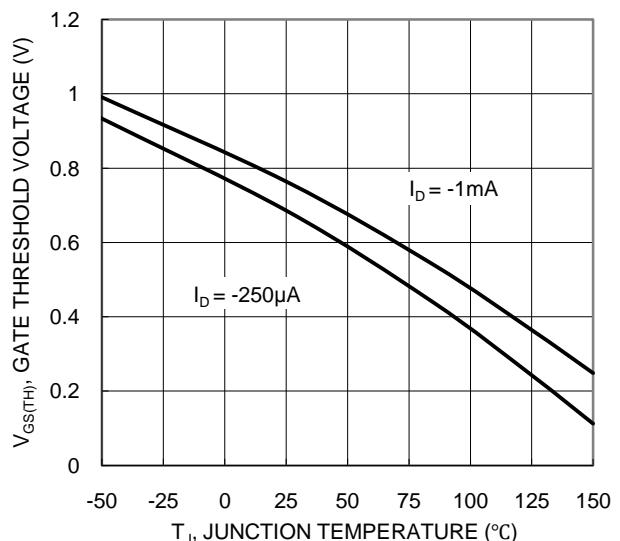


Figure 8. Gate Threshold Variation vs. Junction Temperature

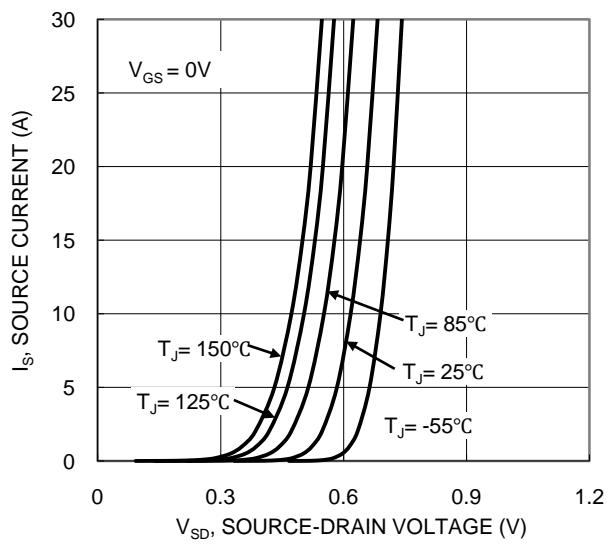


Figure 9. Diode Forward Voltage vs. Current

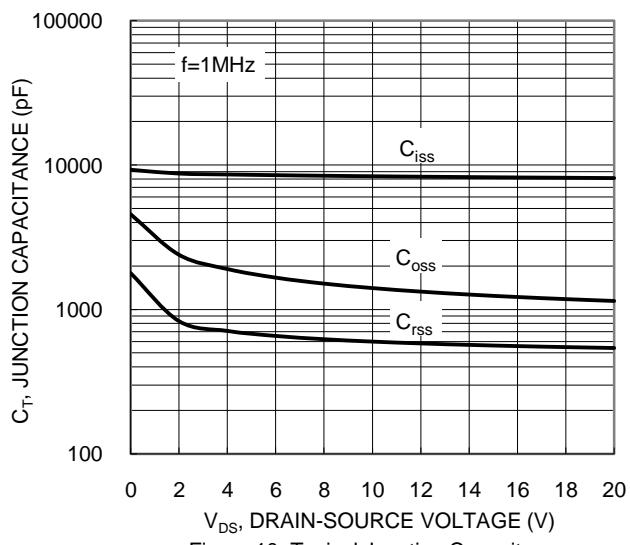


Figure 10. Typical Junction Capacitance

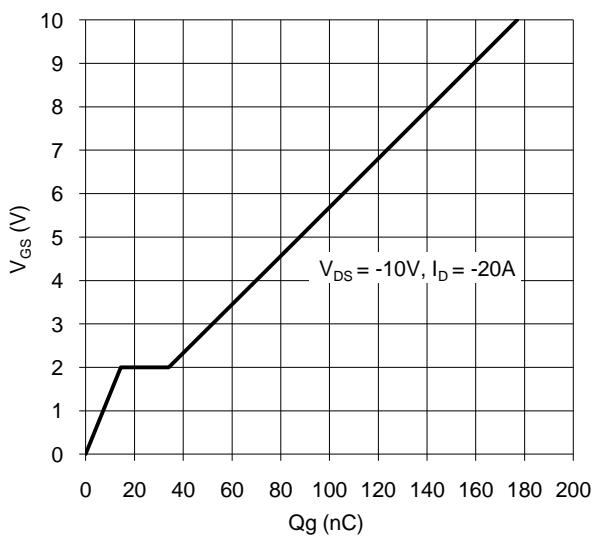


Figure 11. Gate Charge

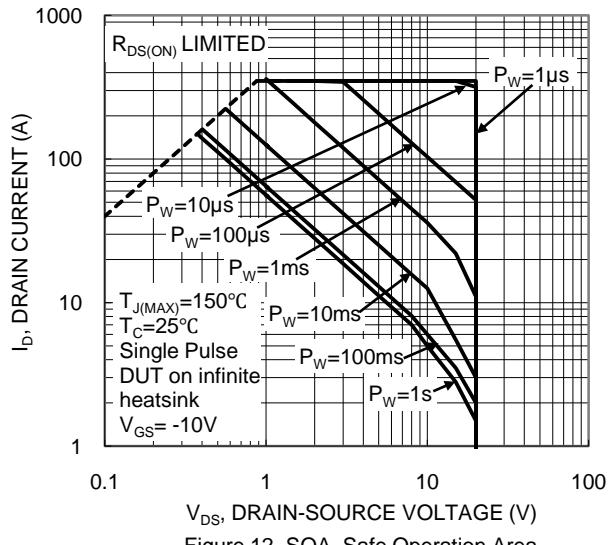


Figure 12. SOA, Safe Operation Area

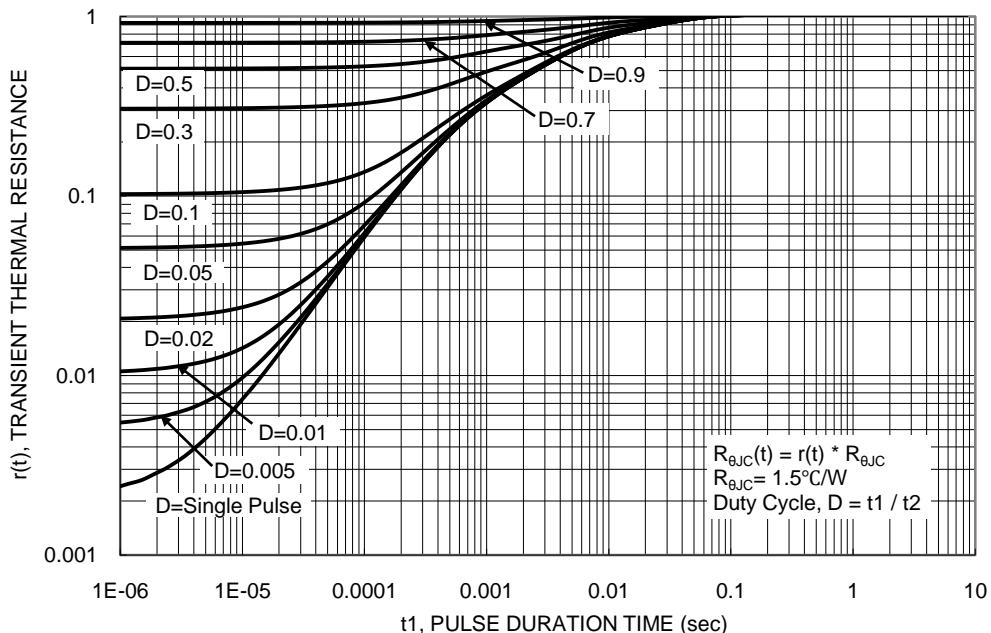
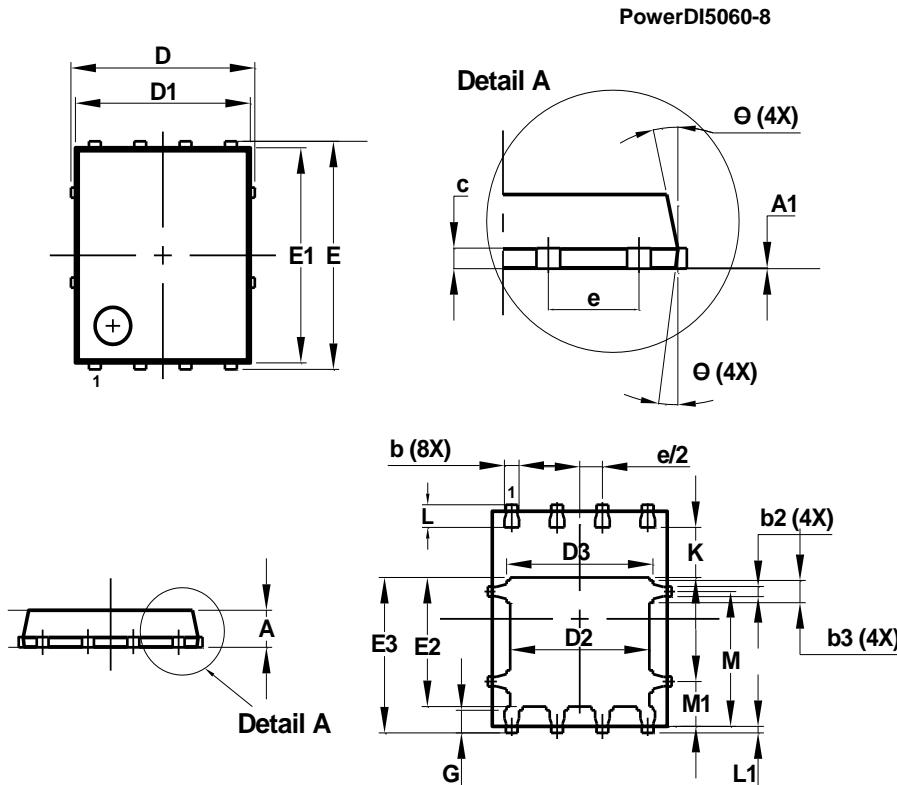


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

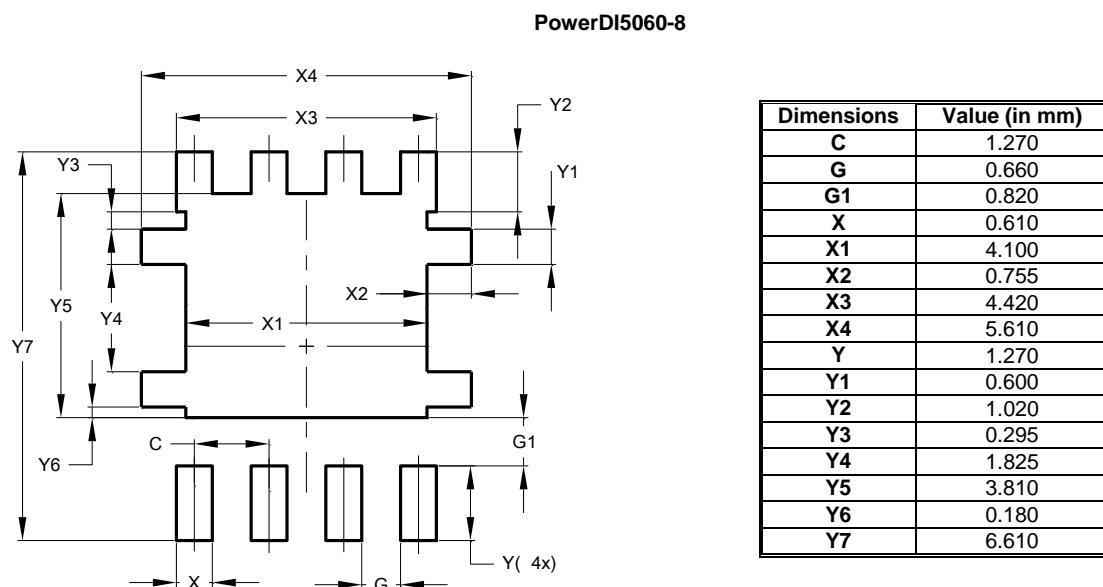
Please see <http://www.diodes.com/package-outlines.html> for the latest version.



PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	—
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	—	—
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



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