

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM6J06FU

Power Management Switch

High-Speed Switching Applications

- Small package
- Low ON-resistance: $R_{DS(ON)} = 0.5 \Omega$ max ($V_{GS} = -4$ V)
: $R_{DS(ON)} = 0.7 \Omega$ max ($V_{GS} = -2.5$ V)
- Low gate threshold voltage

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	-20	V
Gate-source voltage	V_{GSS}	± 12	V
Drain current	DC	I_D	mA
	Pulse	I_{DP}	-1300
Power dissipation	P_D (Note 1)	300	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

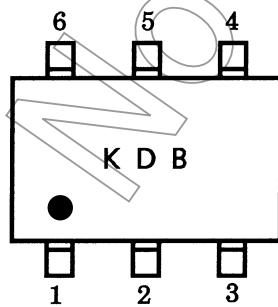
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Mounted on FR4 board.

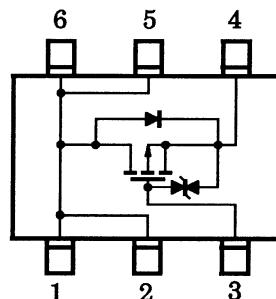
(25.4 mm \times 25.4 mm \times 1.6 mm, Cu pad: 0.32 mm 2 \times 6)

Please refer to Figure 1.

Marking



Equivalent Circuit



Handling Precaution

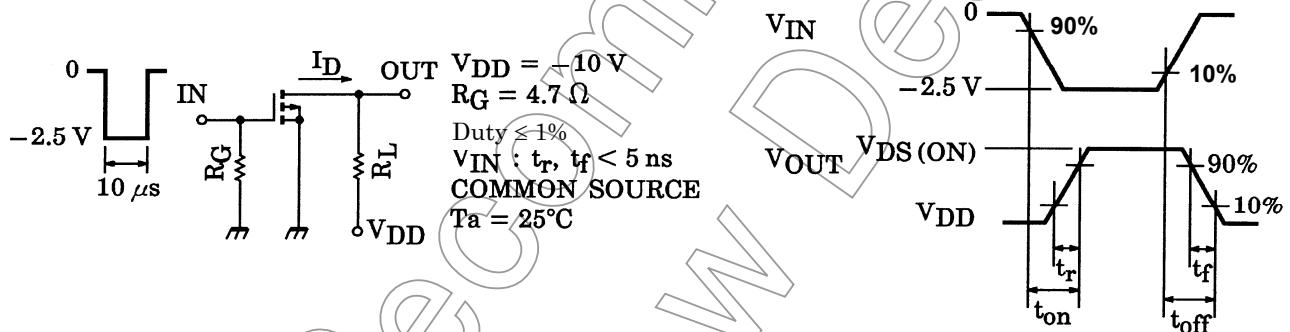
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I _{GSS}	V _{GS} = ±12 V, V _{DS} = 0	—	—	±1	μA
Drain-source breakdown voltage	V _{(BR) DSS}	I _D = -1 mA, V _{GS} = 0	-20	—	—	V
Drain cut-off current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0	—	—	-1	μA
Gate threshold voltage	V _{th}	V _{DS} = -3 V, I _D = -0.1 mA	-0.6	—	-1.1	V
Forward transfer admittance	Y _{fs}	V _{DS} = -3 V, I _D = -0.3 A (Note 2)	0.6	—	—	S
Drain-source ON-resistance	R _{DSS} (ON)	I _D = -0.3 A, V _{GS} = -4 V (Note 2)	—	0.4	0.5	Ω
		I _D = -0.3 A, V _{GS} = -2.5 V (Note 2)	—	0.55	0.7	Ω
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz	—	160	—	pF
Reverse transfer capacitance	C _{rss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz	—	25	—	pF
Output capacitance	C _{oss}	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz	—	90	—	pF
Switching time	Turn-on time	t _{on}	V _{DD} = -10 V, I _D = -0.3 A, V _{GS} = 0 to -2.5 V, R _G = 4.7 Ω	—	27	ns
	Turn-off time	t _{off}		—	43	

Note 2: Pulse test

Switching Time Test Circuit

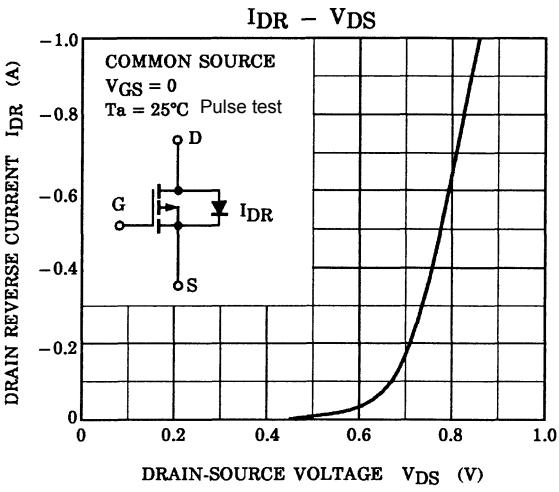
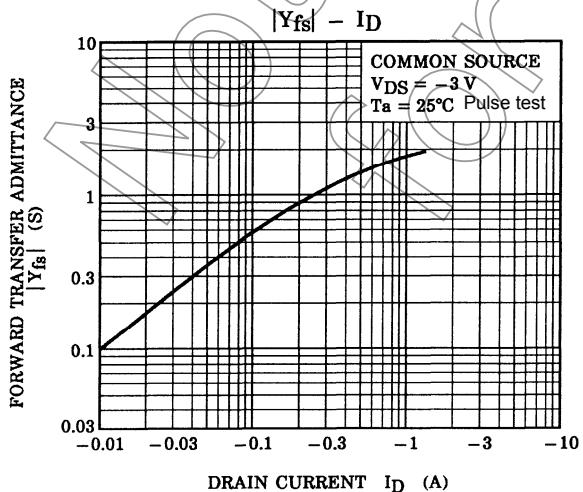
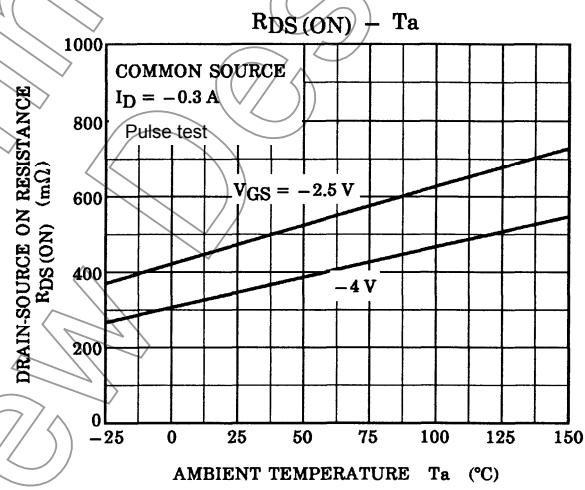
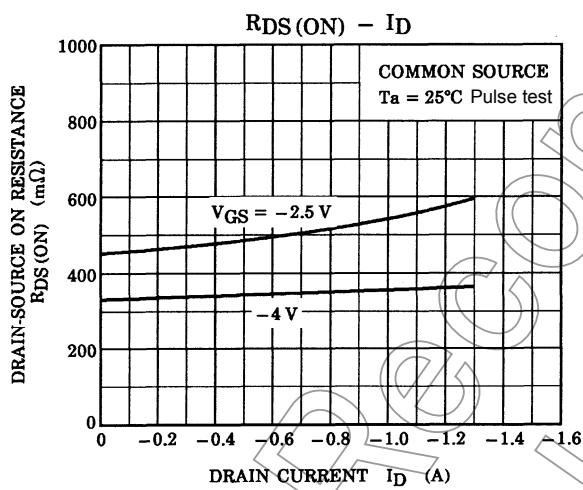
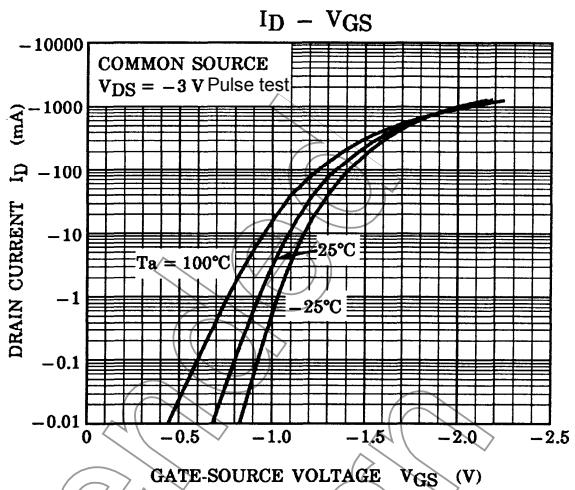
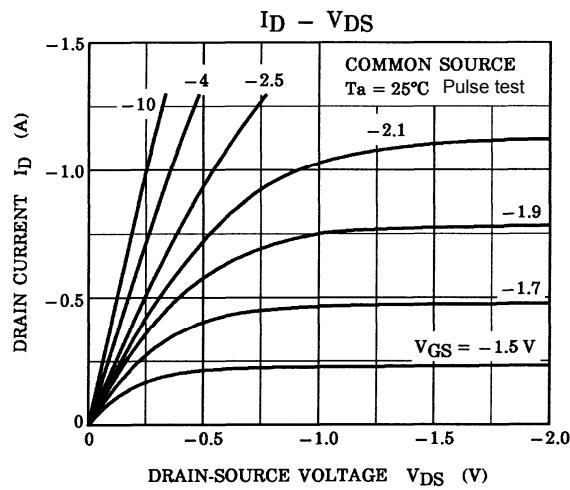


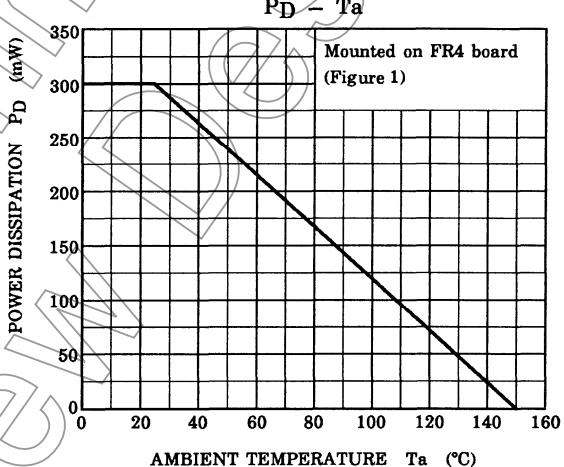
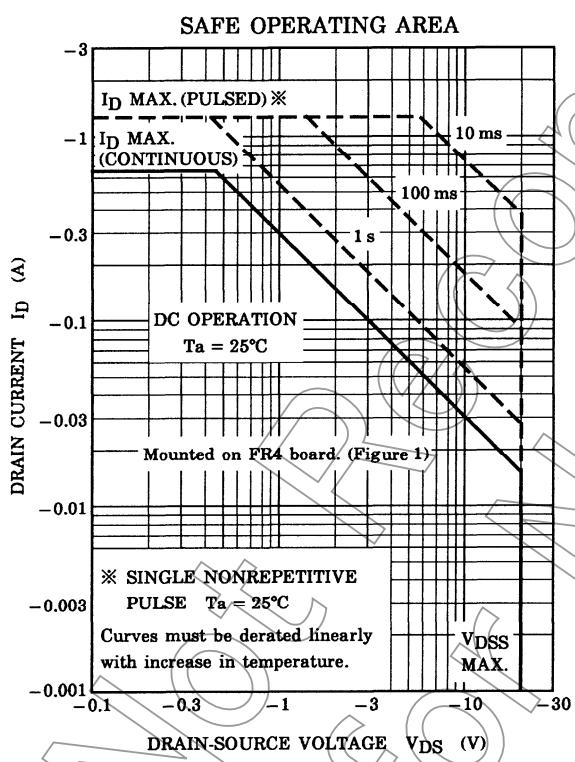
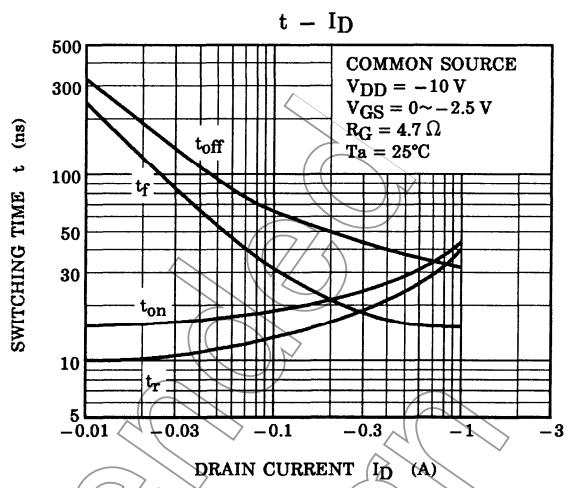
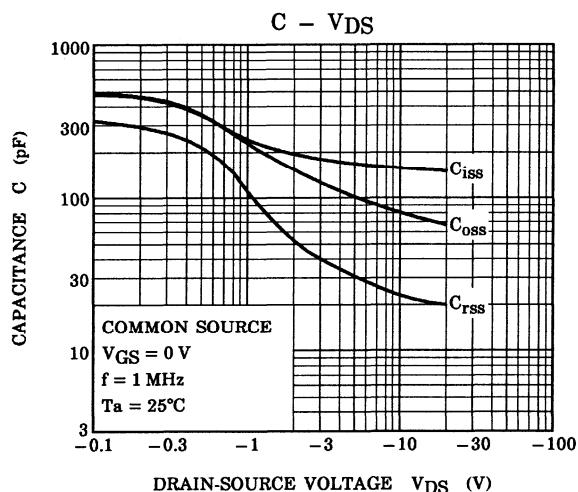
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = -100 μA for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th}.

(Relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on))

Please take this into consideration for using the device.





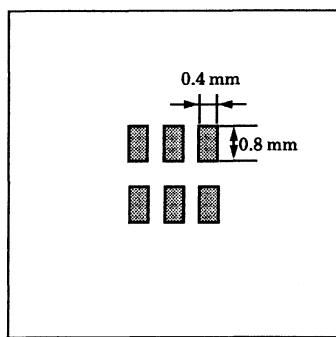


Figure 1 25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.32 mm² × 6

Not Recommended
for New Design

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