

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM6J06FU

Power Management Switch

High-Speed Switching Applications

- Small package
- Low ON-resistance: $R_{DS(ON)} = 0.5 \Omega$ max ($V_{GS} = -4$ V)
: $R_{DS(ON)} = 0.7 \Omega$ max ($V_{GS} = -2.5$ V)
- Low gate threshold voltage

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	-650	mA
	Pulse	I_{DP}	-1300	
Power dissipation		P_D (Note 1)	300	mW
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$

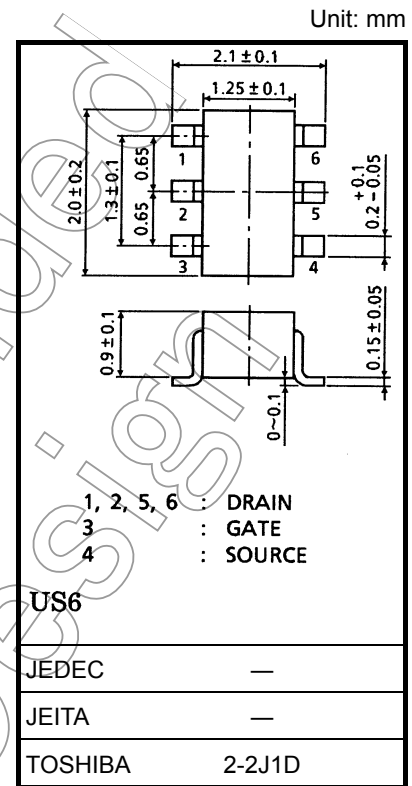
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Mounted on FR4 board.

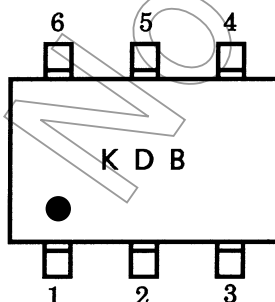
(25.4 mm \times 25.4 mm \times 1.6 mm, Cu pad: 0.32 mm² \times 6)

Please refer to Figure 1.

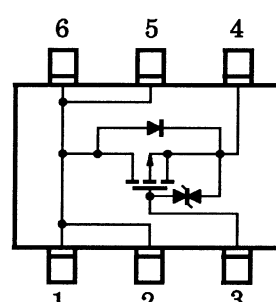


Weight: 6.8 mg (typ.)

Marking



Equivalent Circuit



Handling Precaution

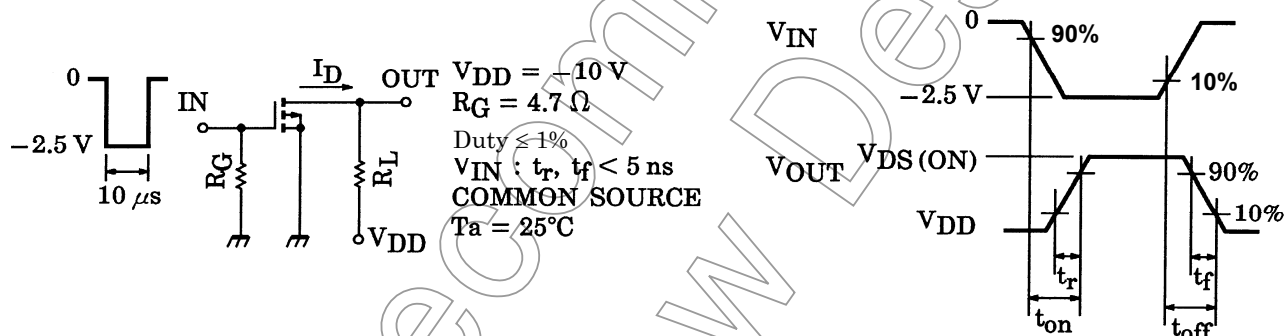
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0$	-20	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0$	—	—	-1	μA
Gate threshold voltage		V_{th}	$V_{DS} = -3\text{ V}, I_D = -0.1\text{ mA}$	-0.6	—	-1.1	V
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -3\text{ V}, I_D = -0.3\text{ A}$ (Note 2)	0.6	—	—	S
Drain-source ON-resistance		$R_{DS(ON)}$	$I_D = -0.3\text{ A}, V_{GS} = -4\text{ V}$ (Note 2)	—	0.4	0.5	Ω
			$I_D = -0.3\text{ A}, V_{GS} = -2.5\text{ V}$ (Note 2)	—	0.55	0.7	
Input capacitance		C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	160	—	pF
Reverse transfer capacitance		C_{rss}	$V_{DS} = -10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	25	—	pF
Output capacitance		C_{oss}	$V_{DS} = -10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	90	—	pF
Switching time	Turn-on time	t_{on}	$V_{DD} = -10\text{ V}, I_D = -0.3\text{ A},$ $V_{GS} = 0\text{ to }-2.5\text{ V}, R_G = 4.7\text{ }\Omega$	—	27	—	ns
	Turn-off time	t_{off}		—	43	—	

Note 2: Pulse test

Switching Time Test Circuit

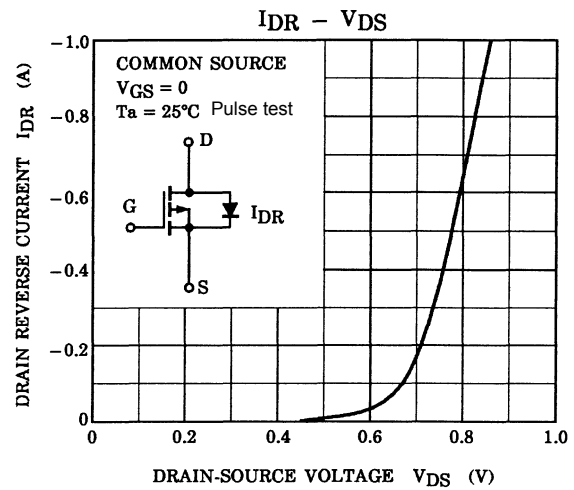
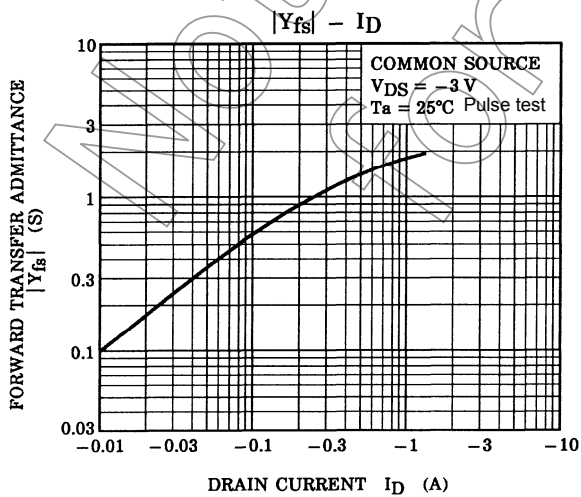
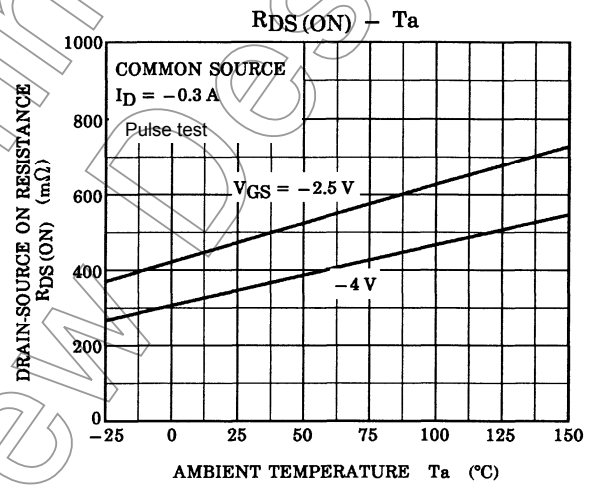
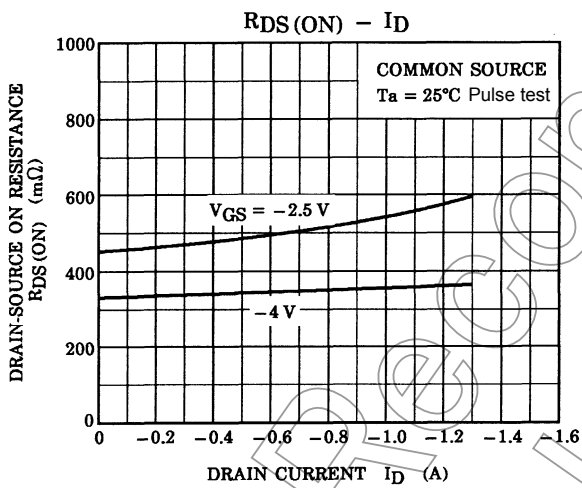
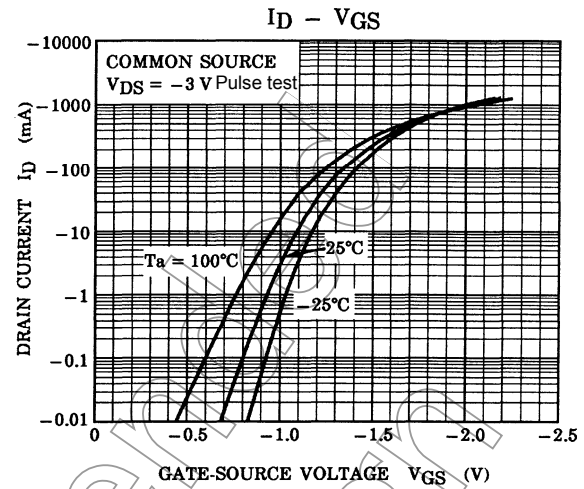
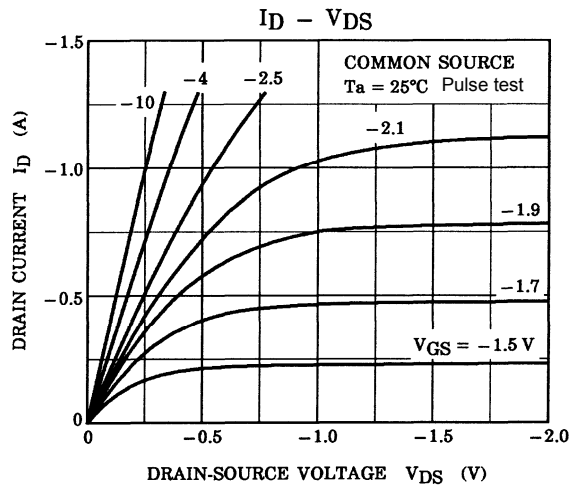


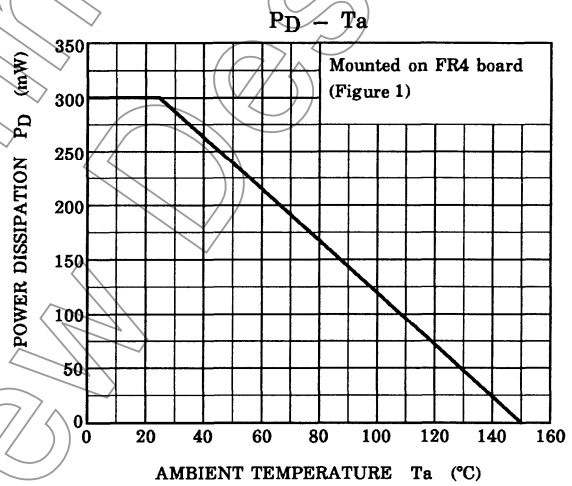
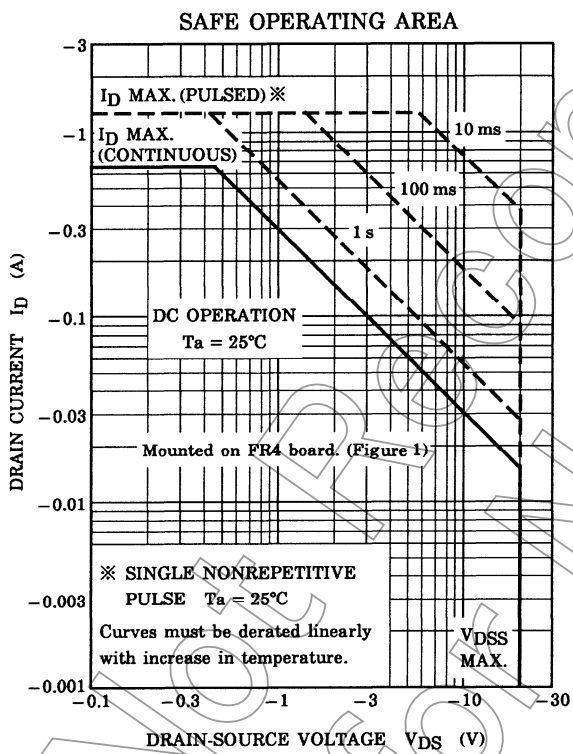
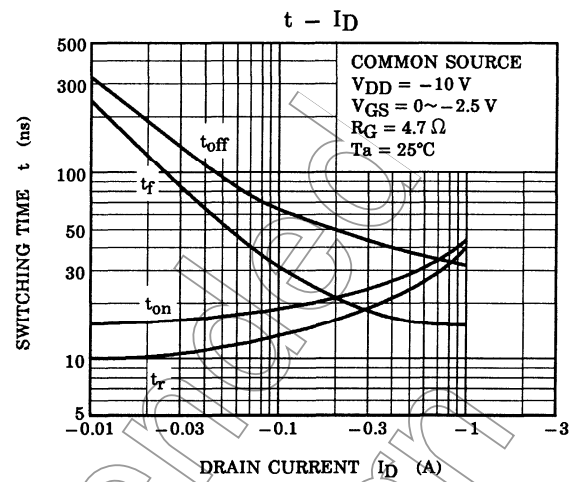
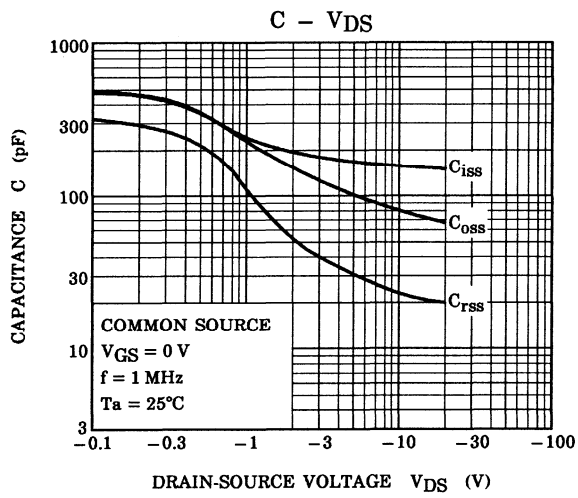
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = -100\text{ }\mu\text{A}$ for this product. For normal switching operation, $V_{GS(on)}$ requires higher voltage than V_{th} and $V_{GS(off)}$ requires lower voltage than V_{th} .

(Relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$)

Please take this into consideration for using the device.





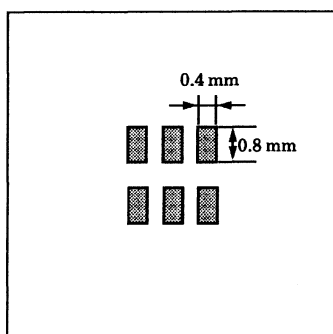


Figure 1 25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.32 mm² × 6

Not Recommended
for New Design

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