

# Self-Protected Low Side Driver with Temperature and Current Limit

42 V, 10 A, Single N-Channel, DPAK

## NCV8408, NCV8408B

NCV8408/B is a single channel protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. Thermal protection includes a latch which can be reset by toggling the input. This device is suitable for harsh automotive environments.

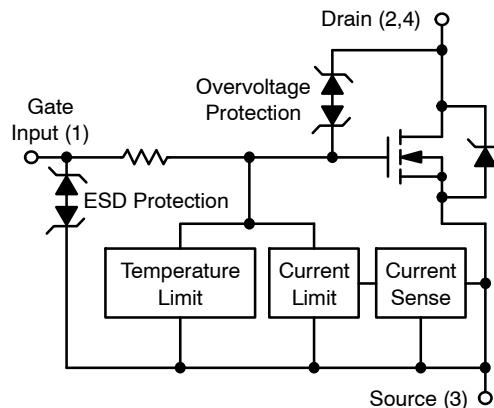
### Features

- Short Circuit Protection
- Thermal Shutdown with Latched Reset
- Gate Input Current Flag During Latched Fault Condition
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- $dV/dt$  Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

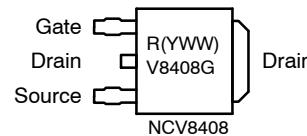
### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

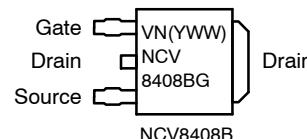
$V_{DSS}$ (Clamped)	$R_{DS(on)}$ TYP	$I_D$ MAX (Limited)
42 V	55 m $\Omega$ @ 5 V	10 A



### MARKING DIAGRAMS



R = Site Code  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package



VN = Site Code  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NCV8408BDTRKG	DPAK (Pb-Free)	2500/Tape & Reel

### DISCONTINUED (Note 1)

NCV8408DTRKG	DPAK (Pb-Free)	2500/Tape & Reel
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<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).

# NCV8408, NCV8408B

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	Vdc
Drain-to-Gate Voltage Internally Clamped ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	42	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 14$	Vdc
Continuous Drain Current	$I_D$	Internally Limited	
Gate Input Current ( $V_{GS} = \pm 14 \text{ V}_{\text{DC}}$ )	$I_{GS}$	$\pm 10$	mA
Source to Drain Current	$I_{SD}$	4.0	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	$P_D$	1.8 2.3	W
Thermal Resistance Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Tab Steady State (Note 3)	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JT}$	70 55 2.1	$^\circ\text{C}/\text{W}$
Single Pulse Inductive Load Switching Energy ( $V_{DD} = 20 \text{ Vdc}$ , $V_{GS} = 5.0 \text{ V}$ , $I_L = 8.0 \text{ A}$ )	$E_{AS}$	185	mJ
Repetitive Pulse Inductive Load Switching Energy ( $V_{DD} = 20 \text{ Vdc}$ , $V_{GS} = 5.0 \text{ V}$ , $I_L = 8.0 \text{ A}$ , $T_J = 25^\circ\text{C}$ )	$E_{AR}$	128	
Repetitive Pulse Inductive Load Switching Energy ( $V_{DD} = 20 \text{ Vdc}$ , $V_{GS} = 5.0 \text{ V}$ , $I_L = 6.8 \text{ A}$ , $T_J = 105^\circ\text{C}$ )	$E_{AR}$	92	
Load Dump Voltage ( $V_{GS} = 0$ and $10 \text{ V}$ , $R_I = 2.0 \Omega$ , $R_L = 4.5 \Omega$ , $t_d = 400 \text{ ms}$ , $T_J = 25^\circ\text{C}$ )	$V_{LD}$	63	V
Operating Junction Temperature	$T_J$	-40 to 150	$^\circ\text{C}$
Storage Temperature	$T_{\text{stg}}$	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted onto minimum pad FR4 PCB (1 oz Cu, 0.06" thick).
2. Surface-mounted onto 2" square FR4 PCB, (1" square, 1 oz Cu, 0.06" thick).
3. Surface-mounted onto minimum pad FR4 PCB (2 oz Cu, 0.06" thick).

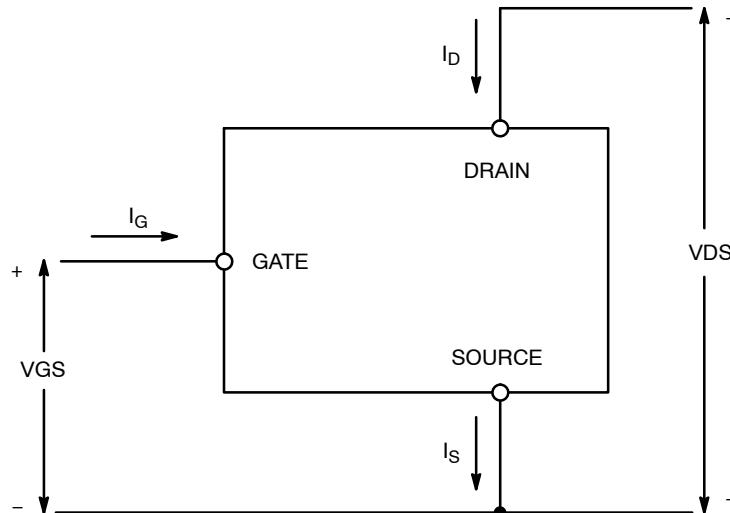


Figure 1. Voltage and Current Convention

# NCV8408, NCV8408B

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Clamped Breakdown Voltage (Note 4) ( $V_{GS} = 0 \text{ V}$ , $I_D = 10 \text{ mA}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{GS} = 0 \text{ V}$ , $I_D = 10 \text{ mA}$ , $T_J = 150^\circ\text{C}$ ) (Note 6) ( $V_{GS} = 0 \text{ V}$ , $I_D = 10 \text{ mA}$ , $T_J = -40^\circ\text{C}$ ) (Note 6)	$V_{(BR)DSS}$	42 40 43	46 45 47	51 51 51	V	
Zero Gate Voltage Drain Current ( $V_{GS} = 0 \text{ V}$ , $V_{DS} = 32 \text{ V}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{GS} = 0 \text{ V}$ , $V_{DS} = 32 \text{ V}$ , $T_J = 150^\circ\text{C}$ ) (Note 6)	$I_{DSS}$	— —	0.6 2.5	5.0 10	$\mu\text{A}$	
<b>INPUT CHARACTERISTICS</b> (Note 4)						
Gate Input Current – Normal Operation ( $V_{GS} = 5.0 \text{ V}$ )	$I_{GSSF}$	—	25	50	$\mu\text{A}$	
Gate Input Current – Protection Latched ( $V_{GS} = 5.0 \text{ V}$ ) (Note 6)	$I_{GSSL}$	—	440	—	$\mu\text{A}$	
Gate Threshold Voltage ( $V_{GS} = V_{DS}$ , $I_D = 1 \text{ mA}$ )	$V_{GS(\text{th})}$	1.0	1.7	2.2	V	
Gate Threshold Temperature Coefficient	$V_{GS(\text{th})}/T_J$	—	5.0	—	$-\text{mV/}^\circ\text{C}$	
Latched Reset Voltage	(Note 6)	$V_{LR}$	0.8	1.4	1.9	V
Latched Reset Time	( $V_{GS} = 5.0 \text{ V}$ to $V_{GS} < 1 \text{ V}$ ) (Note 6)	$t_{LR}$	10	40	100	$\mu\text{s}$
Internal Gate Input Resistance		—	25.5	—	k $\Omega$	
<b>ON CHARACTERISTICS</b> (Note 4)						
Static Drain-to-Source On-Resistance ( $V_{GS} = 5.0 \text{ V}$ , $I_D = 3.0 \text{ A}$ , $T_J @ 25^\circ\text{C}$ ) ( $V_{GS} = 5.0 \text{ V}$ , $I_D = 3.0 \text{ A}$ , $T_J @ 150^\circ\text{C}$ ) (Note 6)	$R_{DS(\text{on})}$	— —	55 100	60 120	m $\Omega$	
Source-Drain Forward On Voltage	( $V_{GS} = 0 \text{ V}$ , $I_S = 7.0 \text{ A}$ )	$V_{SD}$	—	0.95	—	V
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-OFF/ON Slew Rate Matching	$V_{GS} = 5.0 \text{ V}$ , $V_{DS} = 13 \text{ V}$ , $R_L = 4 \Omega$ ; $T_J = -40^\circ\text{C}$ $T_J = 150^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $-40^\circ\text{C} < T_J < 150^\circ\text{C}$	$T_{\text{Match}}$	-15 -15 -5 -20	— — — —	15 15 5 20	%
Turn-ON Delay Time	$V_{GS} = 5 \text{ V}$ , $V_{DS} = 13 \text{ V}$ $R_L = 4 \Omega$ , $-40^\circ\text{C} < T_J < 150^\circ\text{C}$	$t_{d(\text{ON})}$		10	20	$\mu\text{s}$
Rise Time (10% $I_D$ to 90% $I_D$ )		$t_r$		20	40	
Turn-OFF Delay Time		$t_{d(\text{OFF})}$		30	60	
Fall Time (90% $I_D$ to 10% $I_D$ )		$t_f$		20	40	
Slew-Rate ON (90% $V_D$ to 10% $V_D$ )		$-dV_{DS}/dt_{\text{ON}}$		0.5		$\text{V}/\mu\text{s}$
Slew-Rate OFF (10% $V_D$ to 90% $V_D$ )		$dV_{DS}/dt_{\text{OFF}}$		0.5		
<b>SELF PROTECTION CHARACTERISTICS</b> ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 5)						
Current Limit $V_{GS} = 5.0 \text{ V}$ , $V_{DS} = 10 \text{ V}$ , $T_J @ 25^\circ\text{C}$ (Note 7) $V_{GS} = 5.0 \text{ V}$ , $V_{DS} = 10 \text{ V}$ , $T_J = 150^\circ\text{C}$ (Notes 6, 7) $V_{GS} = 5.0 \text{ V}$ , $V_{DS} = 10 \text{ V}$ , $T_J = -40^\circ\text{C}$ (Notes 6, 7)	$I_{\text{LIM}}$	10 10 9	13 — —	16 18 16	A	
Temperature Limit (Turn-off)	$V_{GS} = 5.0 \text{ V}$ $V_{GS} = 10 \text{ V}$	$T_{\text{LIM}(\text{off})}$	150 150	175 165	200 185	°C
<b>ESD ELECTRICAL CHARACTERISTICS</b> ( $T_J = 25^\circ\text{C}$ unless otherwise noted)						
Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000	—	—	V
Electro-Static Discharge Capability	Machine Model (MM)	ESD	400	—	—	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.
5. Fault conditions are viewed as beyond the normal operating range of the part.
6. Not subject to production testing.
7. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

# NCV8408, NCV8408B

## TEST CIRCUITS AND WAVEFORMS

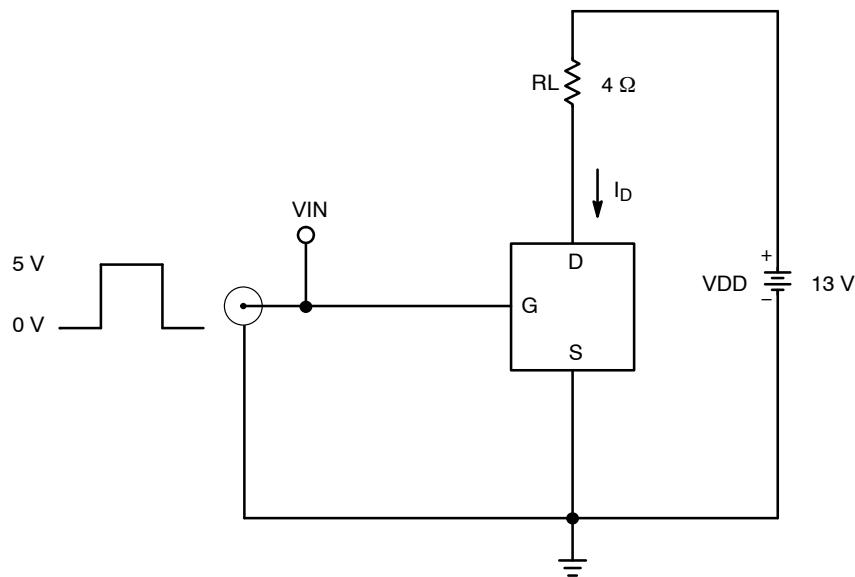


Figure 2. Resistive Load Switching Test Circuit

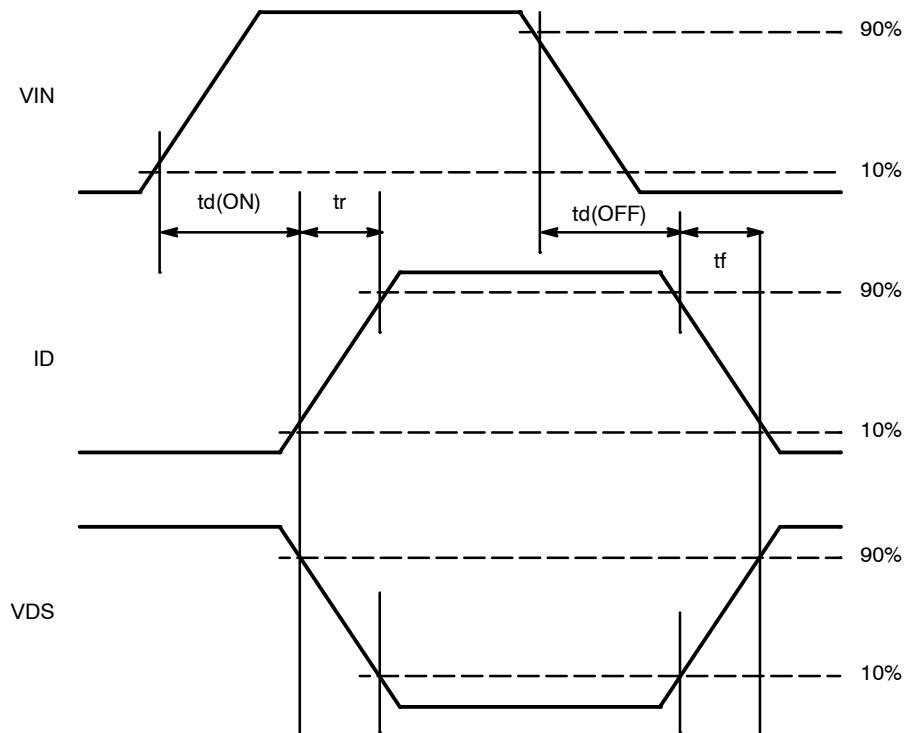
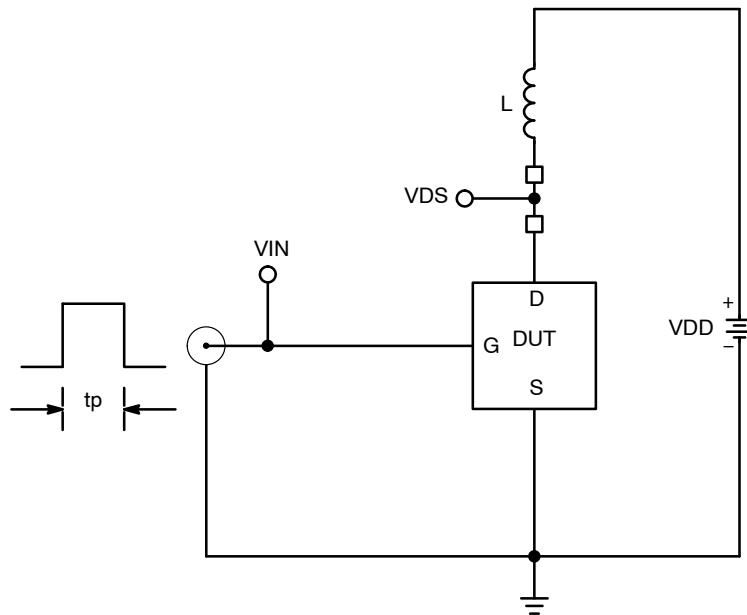


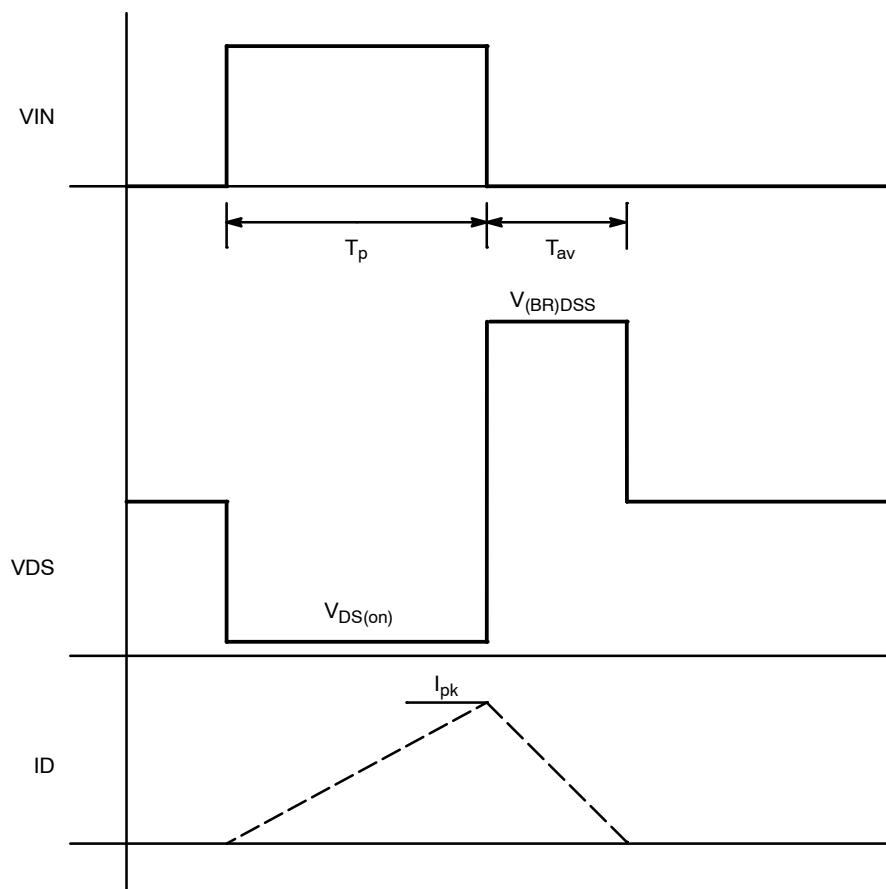
Figure 3. Resistive Load Switching Waveforms

## NCV8408, NCV8408B

## TEST CIRCUITS AND WAVEFORMS



**Figure 4. Inductive Load Switching Test Circuit**



**Figure 5. Inductive Load Switching Waveforms**

## NCV8408, NCV8408B

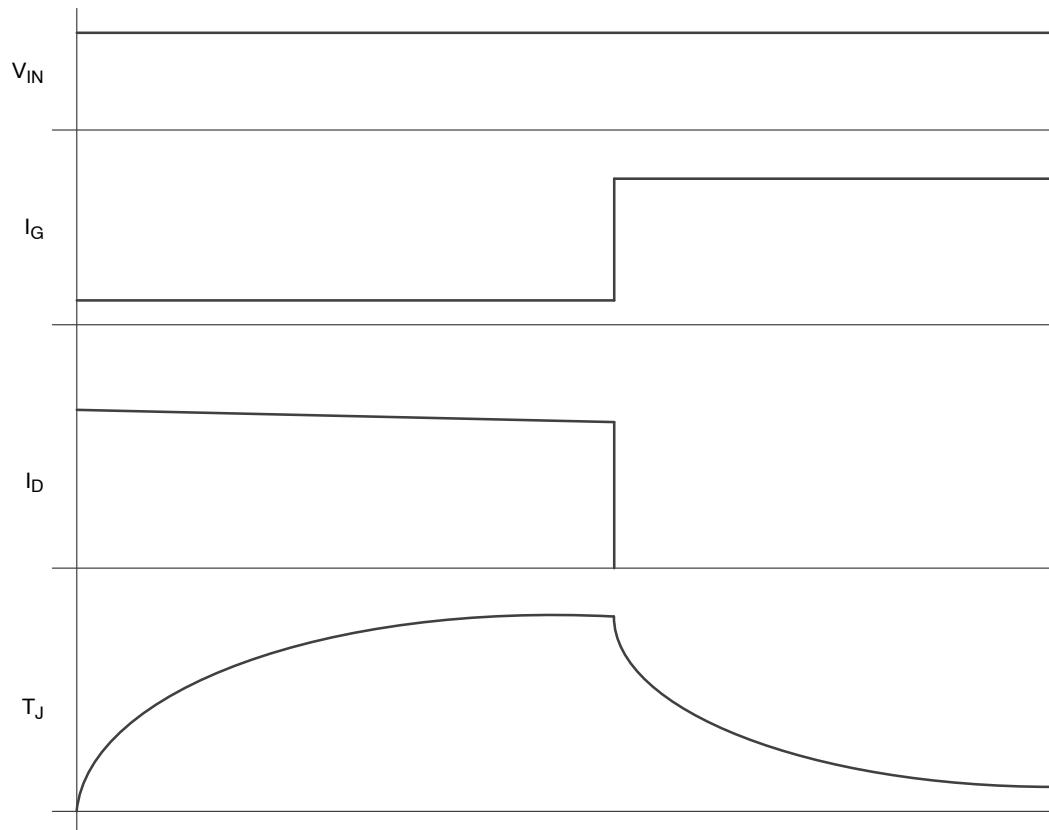


Figure 6. Short-Circuit Protection Behavior

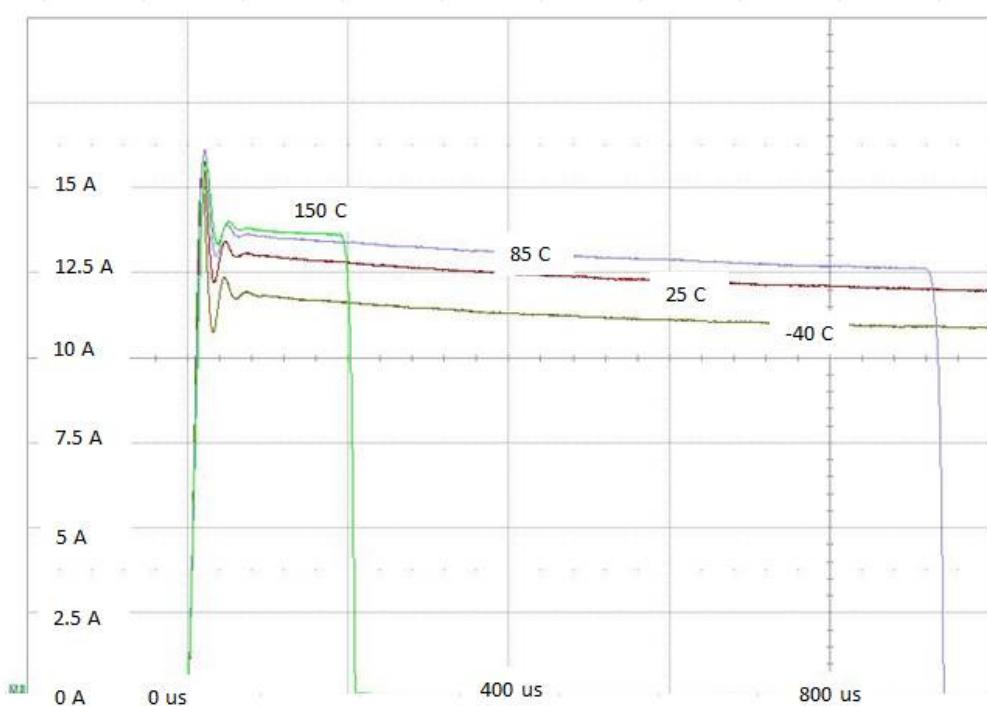


Figure 7. Turn on into Short Circuit Device Response

# NCV8408, NCV8408B

## TYPICAL CHARACTERISTICS

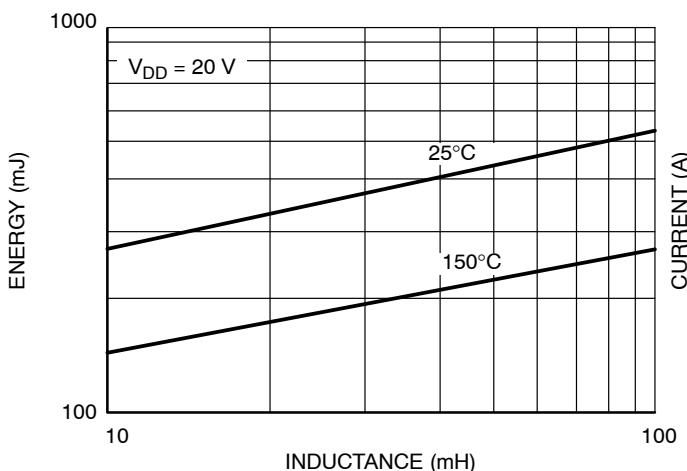


Figure 8. NCV8408 Maximum Switch Off Energy vs Inductance

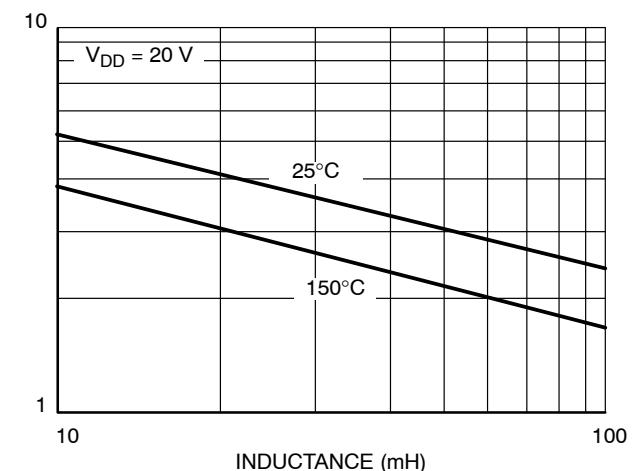


Figure 9. NCV8408 Maximum Switch Off Current vs Inductance

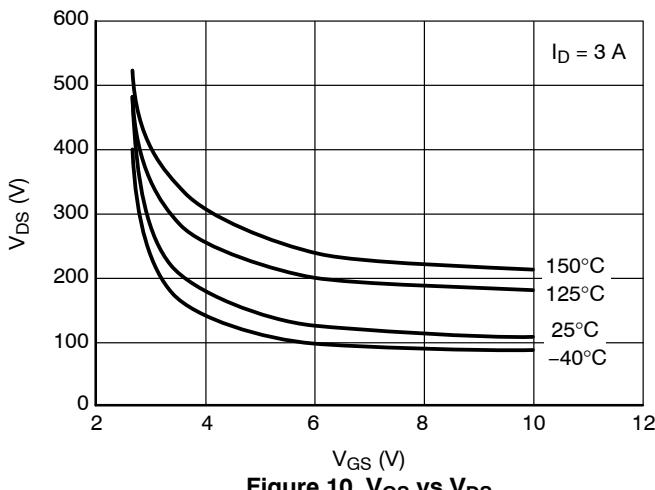


Figure 10.  $V_{GS}$  vs  $V_{DS}$

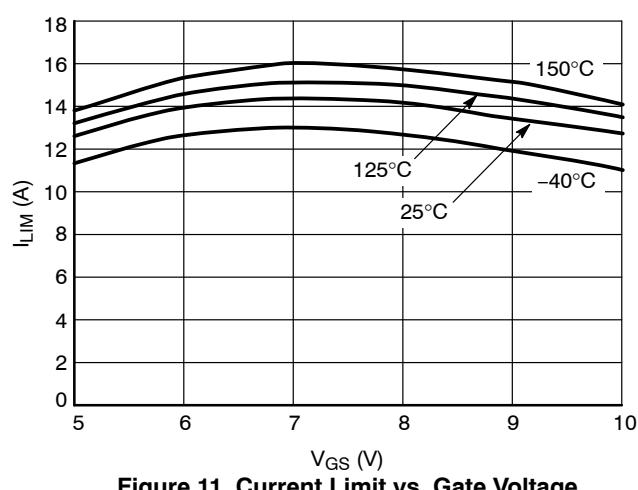


Figure 11. Current Limit vs. Gate Voltage

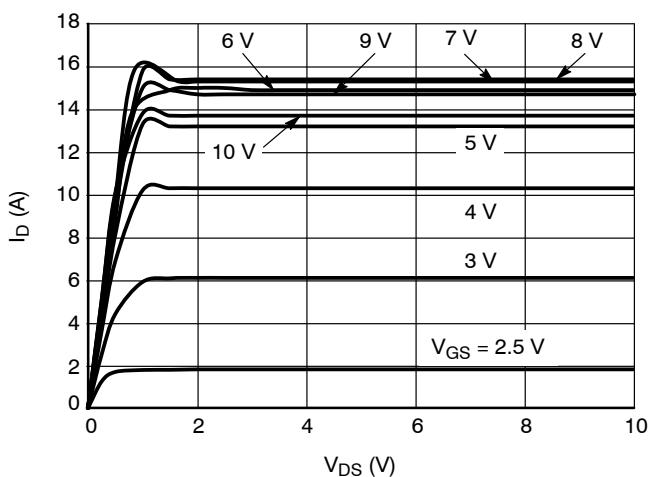


Figure 12. Drain Current vs. Drain Voltage

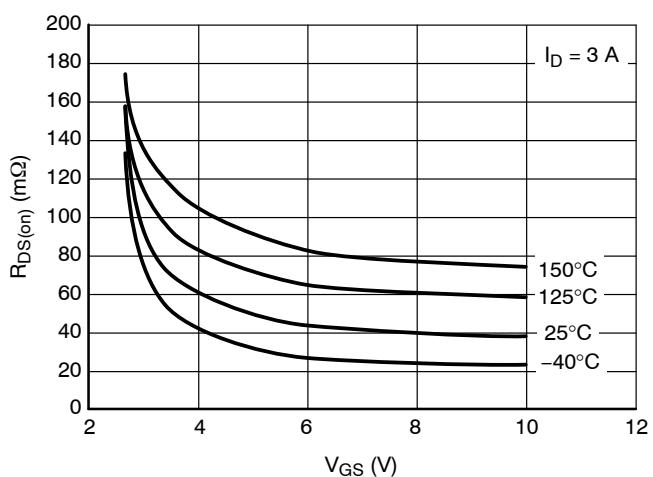


Figure 13.  $R_{DS(on)}$  vs. Gate Voltage

# NCV8408, NCV8408B

## TYPICAL CHARACTERISTICS

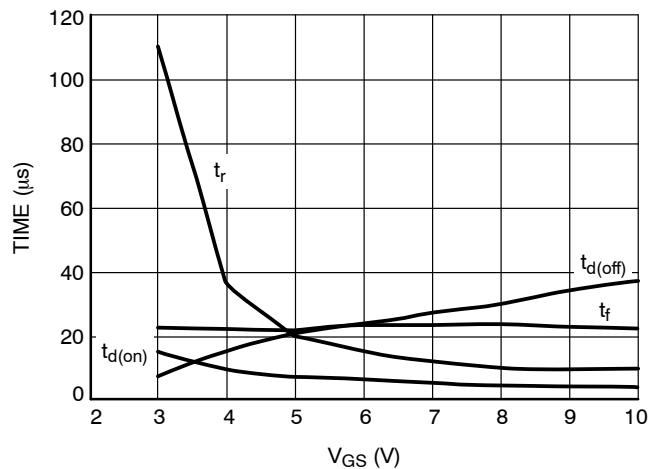


Figure 14. Resistive Switching

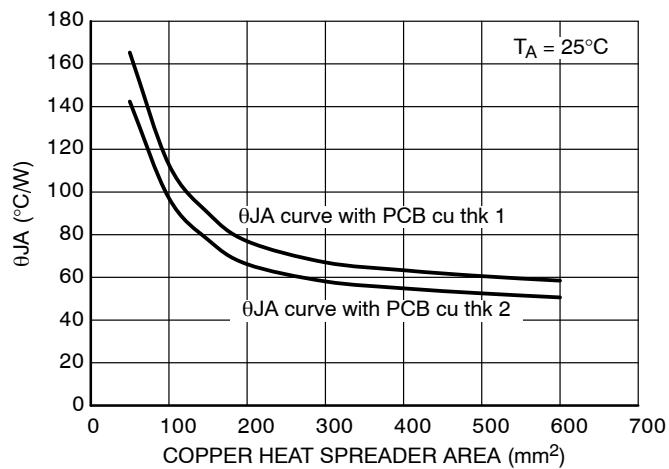


Figure 15.  $R_{\theta JA}$  vs. Copper Area

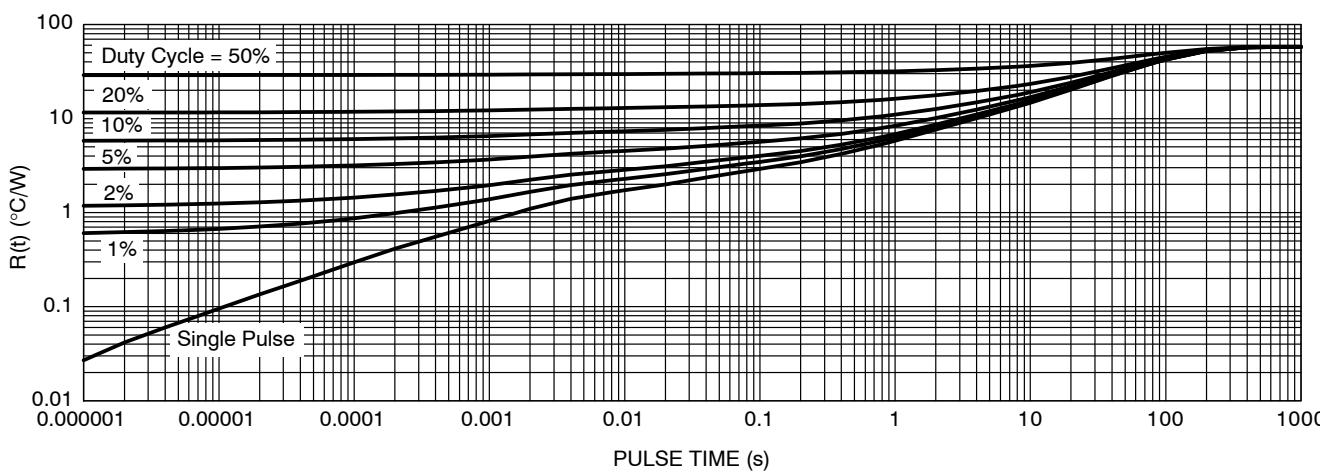
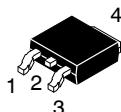
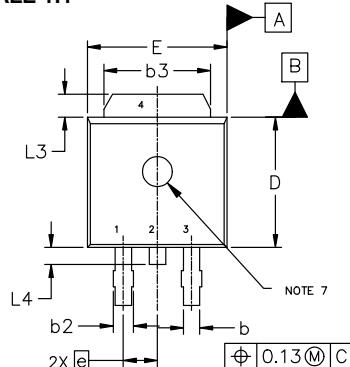


Figure 16. Transient Thermal Resistance



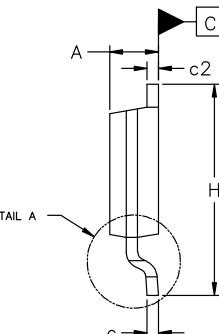
SCALE 1:1



TOP VIEW

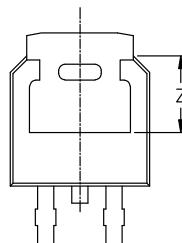
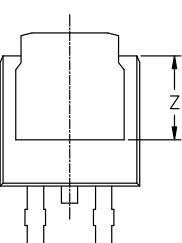
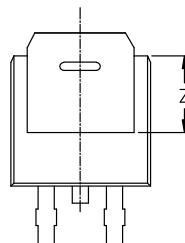
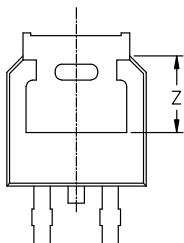
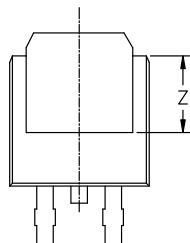
**DPAK3 6.10x6.54x2.28, 2.29P**  
CASE 369C  
ISSUE J

DATE 12 AUG 2025



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29	2.29 BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

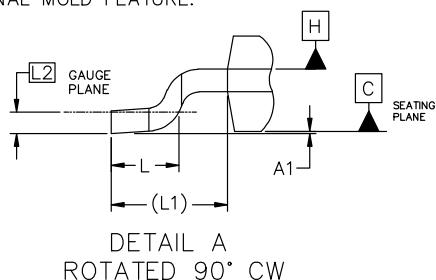
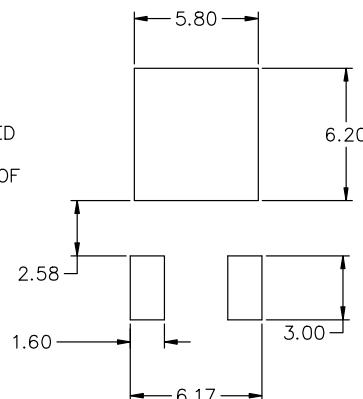


BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

## NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DETAIL A  
ROTATED 90° CW

RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

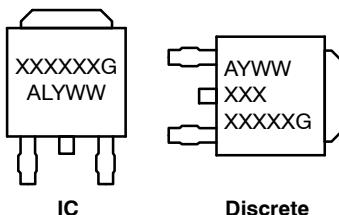
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
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**DPAK3 6.10x6.54x2.28, 2.29P**  
**CASE 369C**  
**ISSUE J**

DATE 12 AUG 2025

## GENERIC MARKING DIAGRAM\*



XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot ">", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE	STYLE 2: PIN 1. GATE	STYLE 3: PIN 1. ANODE	STYLE 4: PIN 1. CATHODE	STYLE 5: PIN 1. GATE
2. COLLECTOR	2. DRAIN	2. CATHODE	2. ANODE	2. ANODE
3. Emitter	3. SOURCE	3. ANODE	3. GATE	3. CATHODE
4. COLLECTOR	4. DRAIN	4. CATHODE	4. ANODE	4. ANODE

STYLE 6: PIN 1. MT1	STYLE 7: PIN 1. GATE	STYLE 8: PIN 1. N/C	STYLE 9: PIN 1. ANODE	STYLE 10: PIN 1. CATHODE
2. MT2	2. COLLECTOR	2. CATHODE	2. CATHODE	2. ANODE
3. GATE	3. Emitter	3. ANODE	3. RESISTOR ADJUST	3. CATHODE
4. MT2	4. COLLECTOR	4. CATHODE	4. CATHODE	4. ANODE

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<b>DESCRIPTION:</b>	<b>DPAK3 6.10x6.54x2.28, 2.29P</b>	<b>PAGE 2 OF 2</b>

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