

### 18-Bit Registers

#### Features

- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5V \pm 10\%$

#### CY74FCT16823T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162823T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}\text{C}$

#### Functional Description

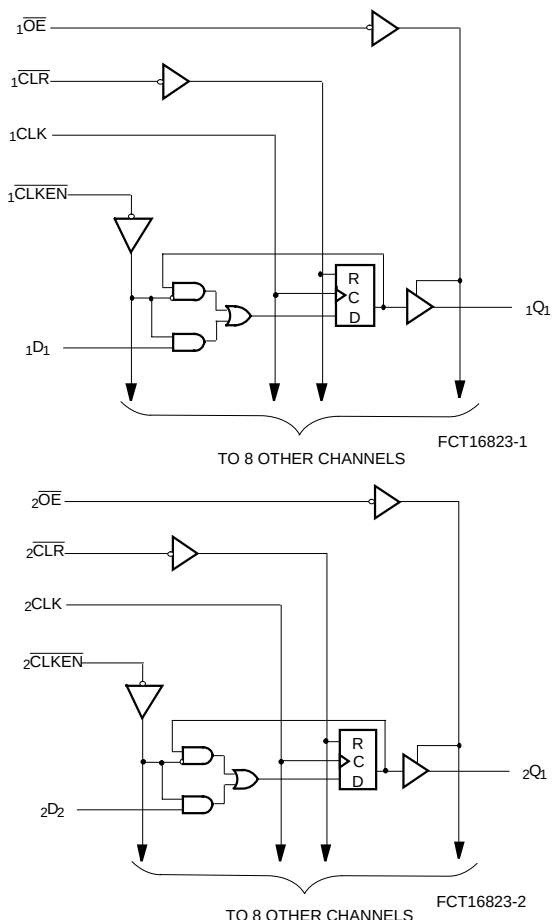
The CY74FCT16823T and the CY74FCT162823T 18-bit bus interface registers are designed for use in high-speed, low-power systems needing wide registers and parity. 18-bit operation is achieved by connecting the control lines of the two 9-bit registers. Flow-through pinout and small shrink packaging aids in simplifying board layout.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16823T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

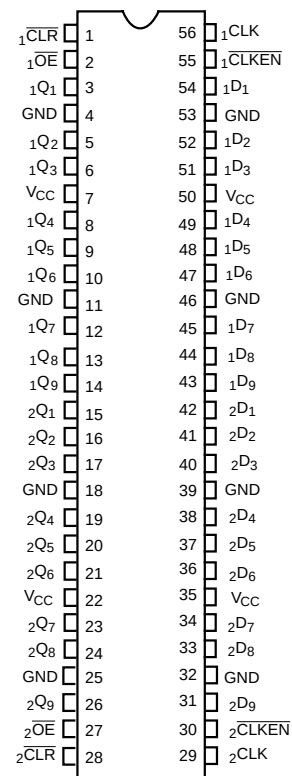
The CY74FCT162823T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162823T is ideal for driving transmission lines.

#### Logic Block Diagrams



#### Pin Configuration SSOP/TSSOP

##### Top View



FCT16823-3

**Pin Description**

| Name                      | Description                            |
|---------------------------|----------------------------------------|
| D                         | Data Inputs                            |
| CLK                       | Clock Inputs                           |
| $\overline{\text{CLKEN}}$ | Clock Enable Inputs (Active LOW)       |
| $\overline{\text{CLR}}$   | Asynchronous Clear Inputs (Active LOW) |
| $\overline{\text{OE}}$    | Output Enable Inputs (Active LOW)      |
| Q                         | Three-State Outputs                    |

**Function Table<sup>[1]</sup>**

| Inputs |     |       |              |   |                  | Outputs  |
|--------|-----|-------|--------------|---|------------------|----------|
| OE     | CLR | CLKEN | CLK          | D | Q                | Function |
| H      | X   | X     | X            | X | Z                | High Z   |
| L      | L   | X     | X            | X | L                | Clear    |
| L      | H   | H     | X            | X | Q <sup>[2]</sup> | Hold     |
| H      | H   | L     | $\downarrow$ | L | Z                | Load     |
| H      | H   | L     | $\downarrow$ | H | Z                |          |
| L      | H   | L     | $\downarrow$ | L | L                |          |
| L      | H   | L     | $\downarrow$ | H | H                |          |

**Maximum Ratings<sup>[3, 4]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage ..... -0.5V to +7.0V

DC Output Current  
(Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Industrial | -40°C to +85°C      | 5V ± 10%        |

**Notes:**

1. H = HIGH Voltage Level.  
L = LOW Voltage Level.  
X = Don't Care.  
Z = HIGH Impedance.  
 $\downarrow$  = LOW-to-HIGH transition.
2. Output level before indicated steady-state input conditions were established.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

**Electrical Characteristics** Over the Operating Range

| Parameter        | Description                                             | Test Conditions                                            | Min. | Typ. <sup>[5]</sup> | Max. | Unit |
|------------------|---------------------------------------------------------|------------------------------------------------------------|------|---------------------|------|------|
| V <sub>IH</sub>  | Input HIGH Voltage                                      |                                                            | 2.0  |                     |      | V    |
| V <sub>IL</sub>  | Input LOW Voltage                                       |                                                            |      |                     | 0.8  | V    |
| V <sub>H</sub>   | Input Hysteresis <sup>[6]</sup>                         |                                                            |      | 100                 |      | mV   |
| V <sub>IK</sub>  | Input Clamp Diode Voltage                               | V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA             |      | -0.7                | -1.2 | V    |
| I <sub>IH</sub>  | Input HIGH Current                                      | V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>     |      |                     | ±1   | μA   |
| I <sub>IL</sub>  | Input LOW Current                                       | V <sub>CC</sub> =Max., V <sub>I</sub> =GND                 |      |                     | ±1   | μA   |
| I <sub>OZH</sub> | High Impedance Output Current (Three-State Output pins) | V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V              |      |                     | ±1   | μA   |
| I <sub>OZL</sub> | High Impedance Output Current (Three-State Output pins) | V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V              |      |                     | ±1   | μA   |
| I <sub>OS</sub>  | Short Circuit Current <sup>[7]</sup>                    | V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND               | -80  | -140                | -200 | mA   |
| I <sub>O</sub>   | Output Drive Current <sup>[7]</sup>                     | V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V              | -50  |                     | -180 | mA   |
| I <sub>OFF</sub> | Power-Off Disable                                       | V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[8]</sup> |      |                     | 1    | μA   |

**Output Drive Characteristics for CY74FCT16823T**

| Parameter       | Description         | Test Conditions                                | Min. | Typ. <sup>[5]</sup> | Max. | Unit |
|-----------------|---------------------|------------------------------------------------|------|---------------------|------|------|
| V <sub>OH</sub> | Output HIGH Voltage | V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA  | 2.5  | 3.5                 |      | V    |
|                 |                     | V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA | 2.4  | 3.5                 |      |      |
|                 |                     | V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA | 2.0  | 3.0                 |      |      |
| V <sub>OL</sub> | Output LOW Voltage  | V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA  |      | 0.2                 | 0.55 | V    |

**Output Drive Characteristics for CY74FCT162823T**

| Parameter        | Description                        | Test Conditions                                                                                   | Min. | Typ. <sup>[5]</sup> | Max. | Unit |
|------------------|------------------------------------|---------------------------------------------------------------------------------------------------|------|---------------------|------|------|
| I <sub>ODL</sub> | Output LOW Voltage <sup>[7]</sup>  | V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V | 60   | 115                 | 150  | mA   |
| I <sub>ODH</sub> | Output HIGH Voltage <sup>[7]</sup> | V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V | -60  | -115                | -150 | mA   |
| V <sub>OH</sub>  | Output HIGH Voltage                | V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA                                                    | 2.4  | 3.3                 |      | V    |
| V <sub>OL</sub>  | Output LOW Voltage                 | V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA                                                     |      | 0.3                 | 0.55 | V    |

**Capacitance<sup>[9]</sup>** (T<sub>A</sub> = +25°C, f = 1.0 MHz)

| Parameter        | Description        | Test Conditions       | Typ. <sup>[5]</sup> | Max. | Unit |
|------------------|--------------------|-----------------------|---------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 0V  | 4.5                 | 6.0  | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 0V | 5.5                 | 8.0  | pF   |

**Notes:**

- Typical values are at V<sub>CC</sub>= 5.0V, T<sub>A</sub>= +25°C ambient.
- This input is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Tested at +25°C.
- This parameter is specified but not tested.

**Power Supply Characteristics**

| Parameter       | Description                                      | Test Conditions <sup>[10]</sup>                                                                                                                                                    |                                                   | Min. | Typ. <sup>[5]</sup> | Max.                 | Unit                 |
|-----------------|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|------|---------------------|----------------------|----------------------|
| $I_{CC}$        | Quiescent Power Supply Current                   | $V_{CC} = \text{Max.}$                                                                                                                                                             | $V_{IN} \leq 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ | —    | 5                   | 500                  | $\mu A$              |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs HIGH) | $V_{CC} = \text{Max.}$                                                                                                                                                             | $V_{IN} = 3.4V^{[11]}$                            | —    | 0.5                 | 1.5                  | mA                   |
| $I_{CCD}$       | Dynamic Power Supply Current <sup>[12]</sup>     | $V_{CC} = \text{Max.}$ ,<br>One Input Toggling,<br>50% Duty Cycle,<br>Outputs Open,<br>$OE = \overline{CLKEN} = GND$                                                               | $V_{IN} = V_{CC}$ or<br>$V_{IN} = GND$            | —    | 75                  | 120                  | $\mu A / \text{MHz}$ |
| $I_C$           | Total Power Supply Current <sup>[13]</sup>       | $V_{CC} = \text{Max.}$ ,<br>$f_0 = 10 \text{ MHz}$ ,<br>50% Duty Cycle,<br>Outputs Open,<br>One Bit Toggling,<br>$OE = \overline{CLKEN} = GND$<br>at $f_1 = 5 \text{ MHz}$         | $V_{IN} = V_{CC}$ or<br>$V_{IN} = GND$            | —    | 0.8                 | 1.7                  | mA                   |
|                 |                                                  |                                                                                                                                                                                    | $V_{IN} = 3.4V$ or<br>$V_{IN} = GND$              | —    | 1.3                 | 3.2                  |                      |
|                 |                                                  | $V_{CC} = \text{Max.}$ ,<br>at $f_1 = 2.5 \text{ MHz}$ ,<br>50% Duty Cycle,<br>Outputs Open,<br>Eighteen Bits Toggling,<br>$OE = \overline{CLKEN} = GND$<br>$f_0 = 10 \text{ MHz}$ | $V_{IN} = V_{CC}$ or<br>$V_{IN} = GND$            | —    | 4.2                 | 7.1 <sup>[14]</sup>  |                      |
|                 |                                                  |                                                                                                                                                                                    | $V_{IN} = 3.4V$ or<br>$V_{IN} = GND$              | —    | 9.2                 | 22.1 <sup>[14]</sup> |                      |

**Notes:**

10. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
11. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
All currents are in milliamps and all frequencies are in megahertz.
14. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[15]</sup>

| Parameter                            | Description                                               | Condition <sup>[16]</sup>                                      | CY74FCT16823AT<br>CY74FCT162823AT |      | Unit | Fig.No. <sup>[16]</sup> |
|--------------------------------------|-----------------------------------------------------------|----------------------------------------------------------------|-----------------------------------|------|------|-------------------------|
|                                      |                                                           |                                                                | Min.                              | Max. |      |                         |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay CLK to Q                                | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 10.0 | ns   | 1, 5                    |
|                                      |                                                           | C <sub>L</sub> =300 pF <sup>[17]</sup><br>R <sub>L</sub> =500Ω | 1.5                               | 20.0 |      |                         |
| t <sub>PHL</sub>                     | Propagation Delay $\overline{\text{CLR}}$ to Q            | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 14.0 | ns   | 1, 5                    |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time $\overline{\text{OE}}$ to Q            | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 12.0 | ns   | 1, 7, 8                 |
|                                      |                                                           | C <sub>L</sub> =300 pF <sup>[17]</sup><br>R <sub>L</sub> =500Ω | 1.5                               | 23.0 |      |                         |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time $\overline{\text{OE}}$ to Q           | C <sub>L</sub> =5 pF <sup>[17]</sup><br>R <sub>L</sub> =500Ω   | 1.5                               | 7.0  | ns   | 1, 7, 8                 |
|                                      |                                                           | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 8.0  |      |                         |
| t <sub>SU</sub>                      | Set-Up Time HIGH or LOW, D to CLK                         | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 3.0                               | —    | ns   | 4                       |
| t <sub>H</sub>                       | Hold Time HIGH or LOW, D to CLK                           |                                                                | 1.5                               | —    | ns   | 4                       |
| t <sub>SU</sub>                      | Set-Up Time HIGH or LOW, $\overline{\text{CLKEN}}$ to CLK |                                                                | 3.0                               | —    | ns   | 9                       |
| t <sub>H</sub>                       | Hold Time HIGH or LOW $\overline{\text{CLKEN}}$ to CLK    |                                                                | 0.0                               | —    | ns   | 9                       |
| t <sub>W</sub>                       | CLK Pulse Width HIGH or LOW                               |                                                                | 6.0                               | —    | ns   | 5                       |
| t <sub>W</sub>                       | $\overline{\text{CLR}}$ Pulse Width LOW                   |                                                                | 6.0                               | —    | ns   | 5                       |
| t <sub>REM</sub>                     | Recovery Time $\overline{\text{CLR}}$ to CLK              |                                                                | 6.0                               | —    | ns   | 6                       |
| t <sub>SK(O)</sub>                   | Output Skew <sup>[18]</sup>                               |                                                                | —                                 | 0.5  | ns   | —                       |

**Switching Characteristics** Over the Operating Range<sup>[15]</sup>

| Parameter                            | Description                                        | Condition <sup>[16]</sup>                                      | CY74FCT16823CT<br>CY74FCT162823CT |      | Unit | Fig.No. <sup>[16]</sup> |
|--------------------------------------|----------------------------------------------------|----------------------------------------------------------------|-----------------------------------|------|------|-------------------------|
|                                      |                                                    |                                                                | Min.                              | Max. |      |                         |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLK to Q                      | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 6.0  | ns   | 1, 5                    |
|                                      |                                                    | C <sub>L</sub> =300 pF <sup>[17]</sup><br>R <sub>L</sub> =500Ω | 1.5                               | 12.5 |      |                         |
| t <sub>PHL</sub>                     | Propagation Delay<br>$\overline{\text{CLR}}$ to Q  | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 6.1  | ns   | 1, 5                    |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>$\overline{\text{OE}}$ to Q  | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 5.5  | ns   | 1, 7, 8                 |
|                                      |                                                    | C <sub>L</sub> =300 pF <sup>[17]</sup><br>R <sub>L</sub> =500Ω | 1.5                               | 12.5 |      |                         |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>$\overline{\text{OE}}$ to Q | C <sub>L</sub> =5 pF <sup>[17]</sup><br>R <sub>L</sub> =500Ω   | 1.5                               | 5.2  | ns   | 1, 7, 8                 |
|                                      |                                                    | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω                  | 1.5                               | 6.5  |      |                         |

**Switching Characteristics** Over the Operating Range<sup>[15]</sup> (continued)

| Parameter          | Description                                                  | Condition <sup>[16]</sup>                     | CY74FCT16823CT<br>CY74FCT162823CT |      | Unit | Fig.No. <sup>[16]</sup> |
|--------------------|--------------------------------------------------------------|-----------------------------------------------|-----------------------------------|------|------|-------------------------|
|                    |                                                              |                                               | Min.                              | Max. |      |                         |
| t <sub>SU</sub>    | Set-Up Time<br>HIGH or LOW, D to CLK                         | C <sub>L</sub> =50 pF<br>R <sub>L</sub> =500Ω | 2.0                               | —    | ns   | 4                       |
| t <sub>H</sub>     | Hold Time<br>HIGH or LOW, D to CLK                           |                                               | 1.5                               | —    | ns   | 4                       |
| t <sub>SU</sub>    | Set-Up Time<br>HIGH or LOW, $\overline{\text{CLKEN}}$ to CLK |                                               | 3.0                               | —    | ns   | 9                       |
| t <sub>H</sub>     | Hold Time HIGH or LOW<br>CLKEN to CLK                        |                                               | 0.0                               | —    | ns   | 9                       |
| t <sub>W</sub>     | CLK Pulse Width<br>HIGH or LOW                               |                                               | 3.3                               | —    | ns   | 5                       |
| t <sub>W</sub>     | $\overline{\text{CLR}}$ Pulse Width LOW                      |                                               | 3.3                               | —    | ns   | 5                       |
| t <sub>REM</sub>   | Recovery Time<br>CLR to CLK                                  |                                               | 6.0                               | —    | ns   | 6                       |
| t <sub>SK(O)</sub> | Output Skew <sup>[18]</sup>                                  |                                               | —                                 | 0.5  | ns   | —                       |

**Notes:**

15. Minimum limits are specified but not tested on Propagation Delays.

16. See "Parameter Measurement Information" in the General Information section.

17. These limits are specified but not tested.

18. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16823**

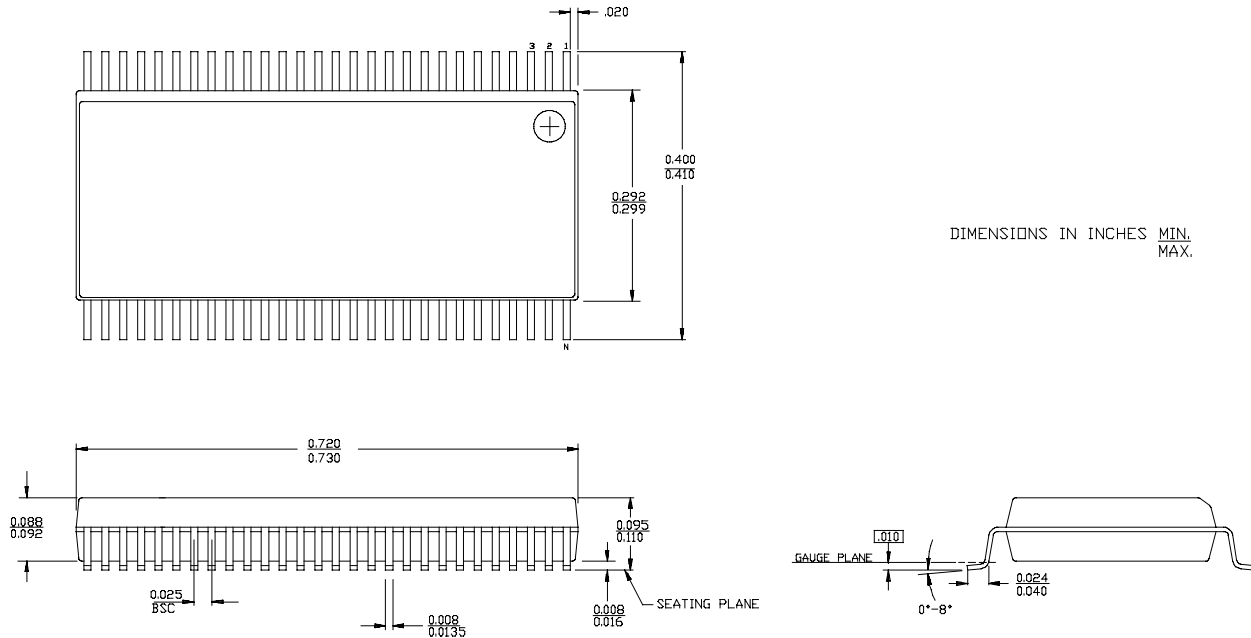
| Speed (ns) | Ordering Code          | Package Name | Package Type            | Operating Range |
|------------|------------------------|--------------|-------------------------|-----------------|
| 6.0        | CY74FCT16823CTPACT     | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |
|            | CY74FCT16823CTPVC/PVCT | O56          | 56-Lead (300-Mil) SSOP  |                 |
| 10.0       | CY74FCT16823ATPACT     | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |

**Ordering Information CY74FCT162823**

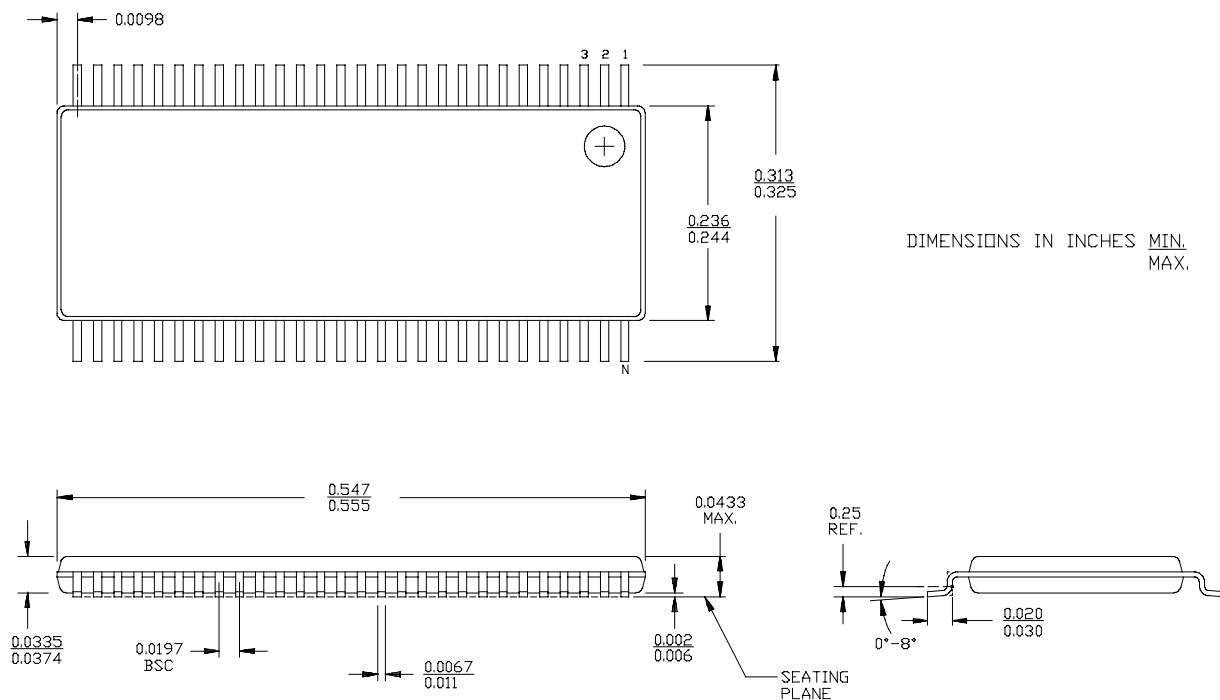
| Speed (ns) | Ordering Code      | Package Name | Package Type            | Operating Range |
|------------|--------------------|--------------|-------------------------|-----------------|
| 6.0        | 74FCT162823CTPACT  | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |
|            | CY74FCT162823CTPVC | O56          | 56-Lead (300-Mil) SSOP  |                 |
|            | 74FCT162823CTPVCT  | O56          | 56-Lead (300-Mil) SSOP  |                 |
| 10.0       | 74FCT162823ATPACT  | Z56          | 56-Lead (240-Mil) TSSOP | Industrial      |

**Package Diagrams**

**56-Lead Shrunk Small Outline Package O56**



**56-Lead Thin Shrunk Small Outline Package Z56**



PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CY74FCT16823ATPACT    | Obsolete      | Production           | TSSOP (DGG)   56 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | FCT16823A           |

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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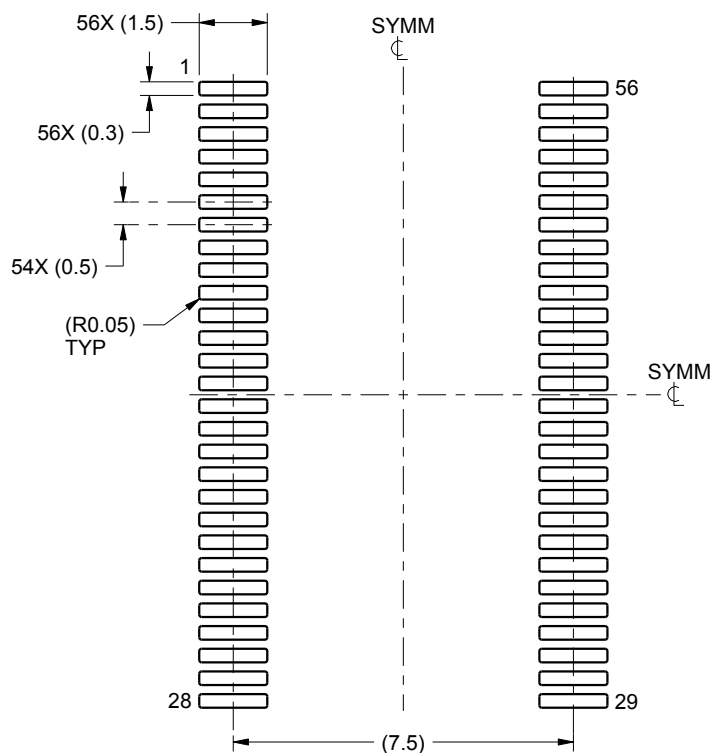


# EXAMPLE BOARD LAYOUT

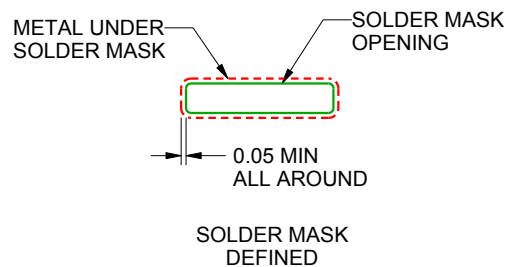
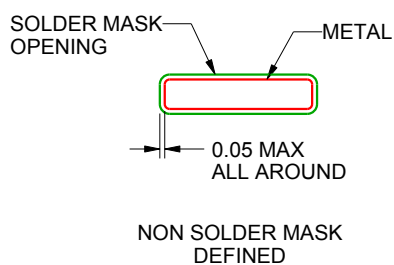
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

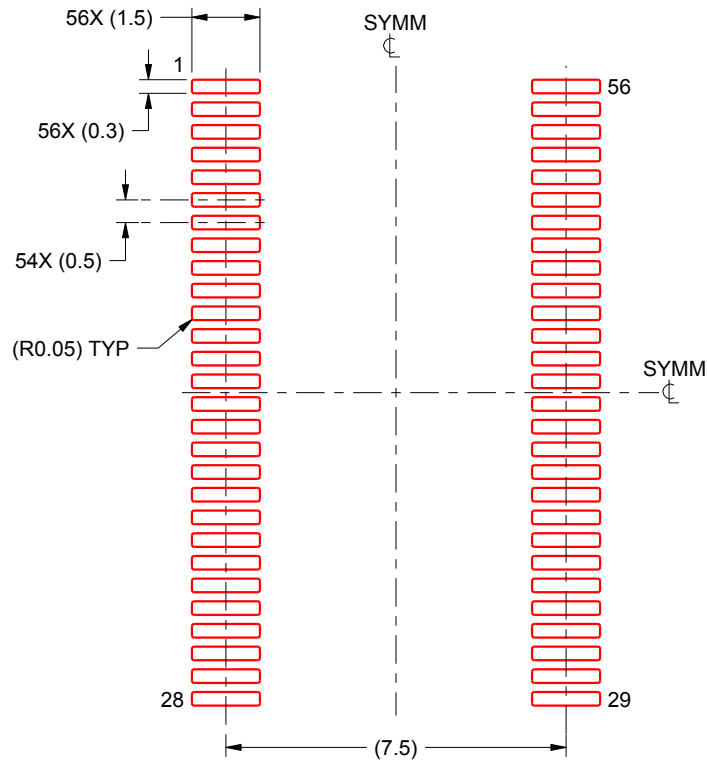
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025