

SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS382C – SEPTEMBER 1997 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $< 0.8\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $> 2\text{ V}$ at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

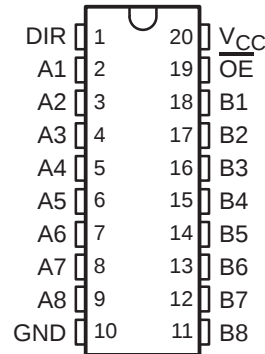
These octal bus transceivers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

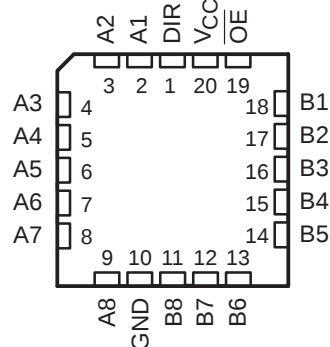
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV245A is characterized for operation from -40°C to 85°C .

SN54LV245A . . . J OR W PACKAGE
SN74LV245A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV245A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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**TEXAS
INSTRUMENTS**

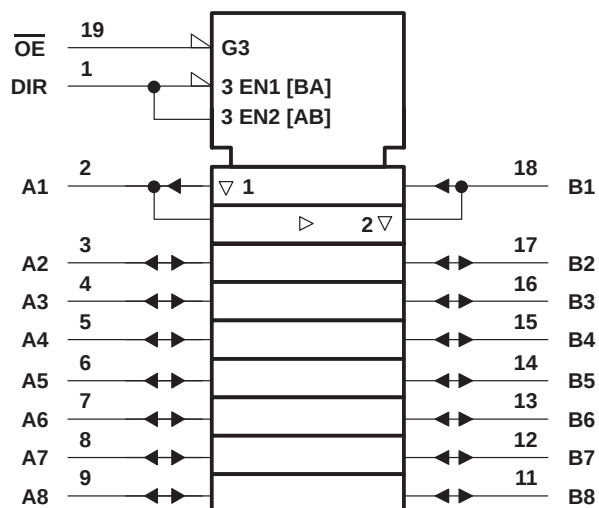
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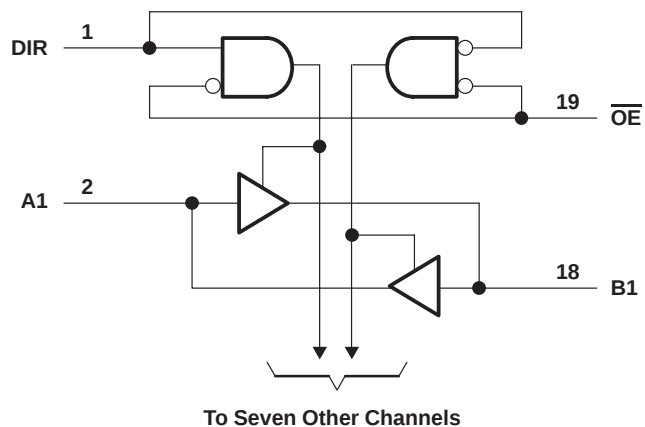
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, V_{CC}		-0.5 V to 7 V
Input voltage range, V_I : Except I/O ports (see Note 1)		-0.5 V to 7 V
I/O ports (see Notes 1 and 2)		-0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)		-0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1)		-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)		-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 35 mA
Continuous current through V_{CC} or GND		± 70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package		115°C/W
DGV package		146°C/W
DW package		97°C/W
NS package		100°C/W
PW package		128°C/W
Storage temperature range, T_{sta}		-65°C to 150°C

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

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recommended operating conditions (see Note 4)

			SN54LV245A		SN74LV245A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	–50		–50		μA
		V _{CC} = 2.3 V to 2.7 V	–2		–2		mA
		V _{CC} = 3 V to 3.6 V	–8		–8		
		V _{CC} = 4.5 V to 5.5 V	–16		–16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LV245A			SN74LV245A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}		I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
		I _{OH} = −2 mA	2.3 V	2			2			
		I _{OH} = −8 mA	3 V	2.48			2.48			
		I _{OH} = −16 mA	4.5 V	3.8			3.8			
V _{OL}		I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
		I _{OL} = 2 mA	2.3 V	0.4			0.4			
		I _{OL} = 8 mA	3 V	0.44			0.44			
		I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I		V _I = V _{CC} or GND	5.5 V	±1			±1			μA
I _{OZ}		V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}		V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	2.4			2.4			pF
			5 V	2.4			2.4			
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V	5.4			5.4			pF
			5 V	5.4			5.4			

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd} *	A or B	B or A	C _L = 15 pF	8.3	13		1	15	1	15	ns
t _{en} *	$\overline{\text{OE}}$	A or B		11.8	19.9		1	22	1	22	
t _{dis} *	$\overline{\text{OE}}$	A or B		11.8	18.1		1	20	1	20	
t _{pd}	A or B	B or A	C _L = 50 pF	11.2	15.9		1	18	1	18	ns
t _{en}	$\overline{\text{OE}}$	A or B		14.1	22.7		1	26	1	26	
t _{dis}	$\overline{\text{OE}}$	A or B		17.6	23.1		1	25	1	25	
t _{sk(o)} †				2						2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	B or A	$C_L = 15 \text{ pF}$	5.9	8.4		1	10	1	10	ns
t_{en}^*	$\overline{OE}$	A or B		8.2	13.2		1	15.5	1	15.5	
t_{dis}^*	$\overline{OE}$	A or B		9.6	16.5		1	19.5	1	19.5	
t_{pd}	A or B	B or A	$C_L = 50 \text{ pF}$	7.9	11.9		1	13.5	1	13.5	ns
t_{en}	$\overline{OE}$	A or B		9.9	16.7		1	19	1	19	
t_{dis}	$\overline{OE}$	A or B		13.9	19.8		1	22	1	22	
$t_{sk(o)}^\dagger$					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}^*	A or B	B or A	$C_L = 15 \text{ pF}$	4.3	5.5		1	6.5	1	6.5	ns
t_{en}^*	$\overline{OE}$	A or B		5.7	8.5		1	10.6	1	10	
t_{dis}^*	$\overline{OE}$	A or B		7.8	12.8		1	14.7	1	14.2	
t_{pd}	A or B	B or A	$C_L = 50 \text{ pF}$	5.6	7.5		1	8.5	1	8.5	ns
t_{en}	$\overline{OE}$	A or B		7	10.6		1	12	1	12	
t_{dis}	$\overline{OE}$	A or B		10.9	14.7		1	16	1	16	
$t_{sk(o)}^\dagger$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† Skew between any two outputs of the same package switching in the same direction

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV245A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.45		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.45		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.94		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

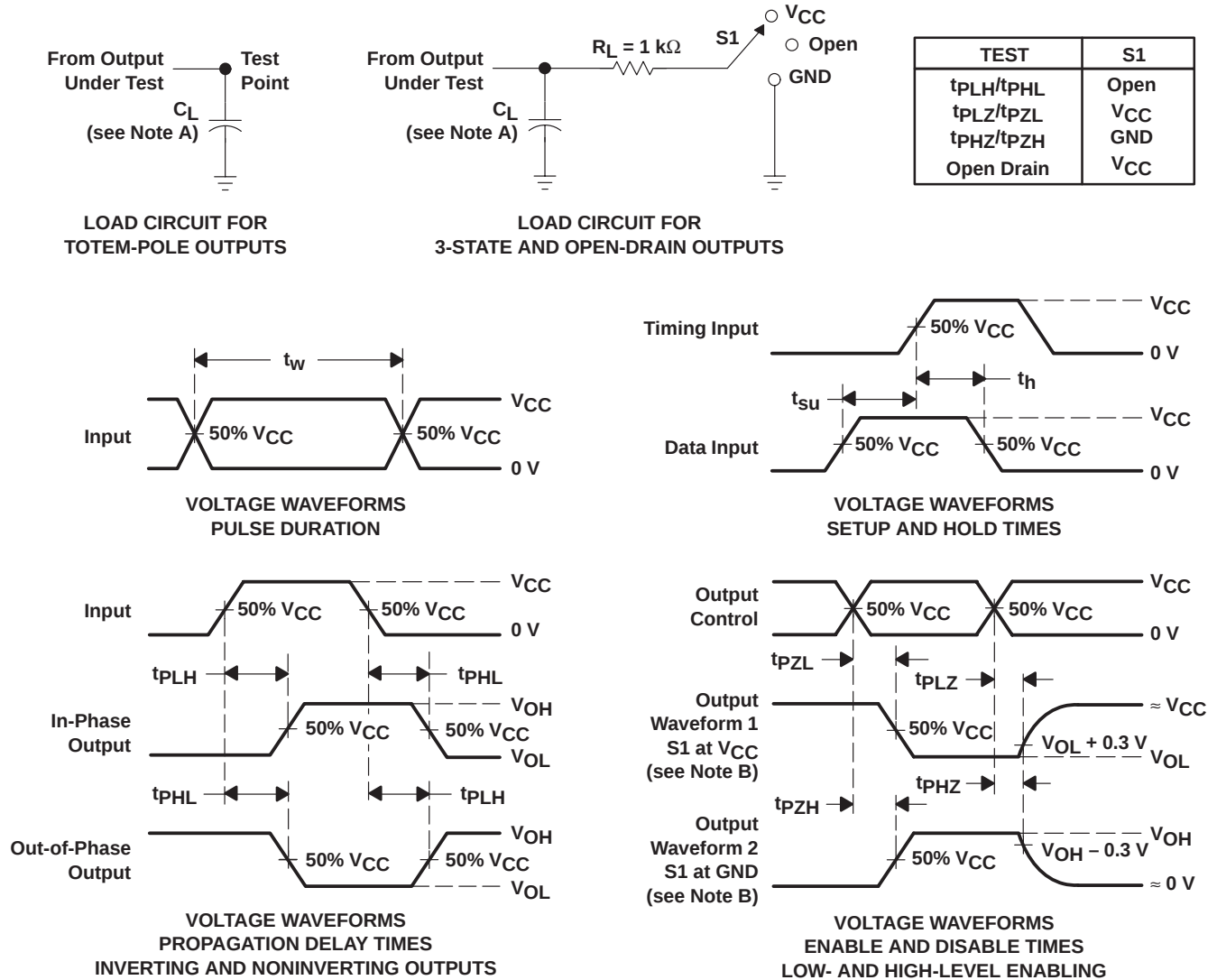
PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	20	pF
				5 V	25	

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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