

DS3680-N Quad Negative Voltage Relay Driver

Check for Samples: [DS3680-N](#)

FEATURES

- –10V to –60V Operation
- Quad 50 mA Sink Capability
- TTL/LS/CMOS or Voltage Comparator Input
- High Input Common-Mode Voltage Range
- Very Low Input Current
- Fail-Safe Disconnect Feature
- Built-In Output Clamp Diode

DESCRIPTION

The DS3680-N is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range ($\pm 20\text{V}$ referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which permits input signals from more than one element of the system.

With low differential input current requirements (typically 100 μA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to ensure that, if the + IN input or both inputs are open, the driver will be OFF.

Connection Diagram

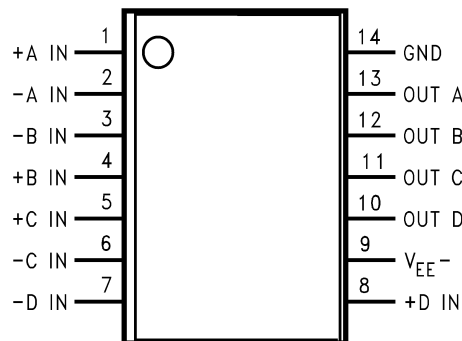


Figure 1. SOIC Package- Top View
See Package Number D0014A



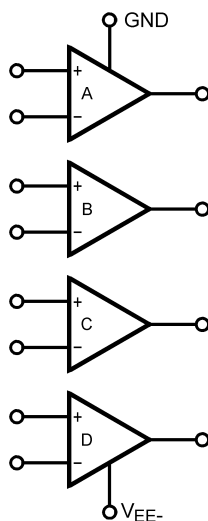
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Block Diagram



Truth Table

Differential Inputs	Outputs
$V_{ID} \geq 2V$	On
$V_{ID} \leq 0.8V$	Off
Open	Off



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (GND to V_{EE-} , and Any Pin)	-70V
Positive Input Voltage (Input to GND)	20V
Negative Input Voltage (Input to V_{EE-})	-5V
Differential Voltage (+ IN to - IN)	$\pm 20V$
Inductive Load	$L_L \leq 5h$
	$I_L \leq 50 \text{ mA}$
Output Current	-100 mA
Storage Temperature	-65°C to +150°C
Maximum Power Dissipation ⁽³⁾ at 25°C	
SOIC Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits. The [Electrical Characteristics](#) provides conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Derate SOIC package 8.02 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (GND to V_{EE-})	-10	-60	V
Input Voltage (Input to GND)	-20	20	V
Logic ON Voltage (+IN) Referenced to -IN	2	20	V

Recommended Operating Conditions (continued)

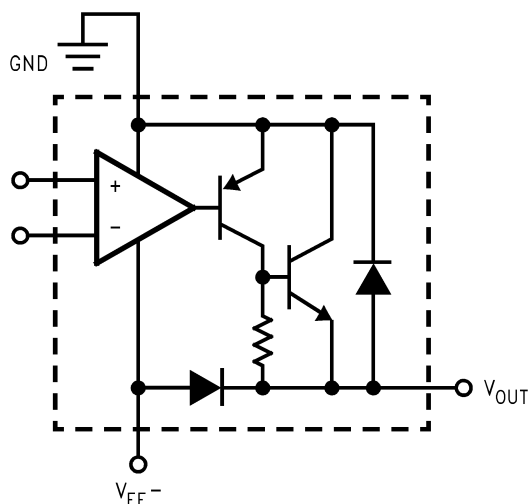
	Min	Max	Units
Logic OFF Voltage (+IN) Referenced to -IN	-20	0.8	V
Temperature Range	-25	+85	°C

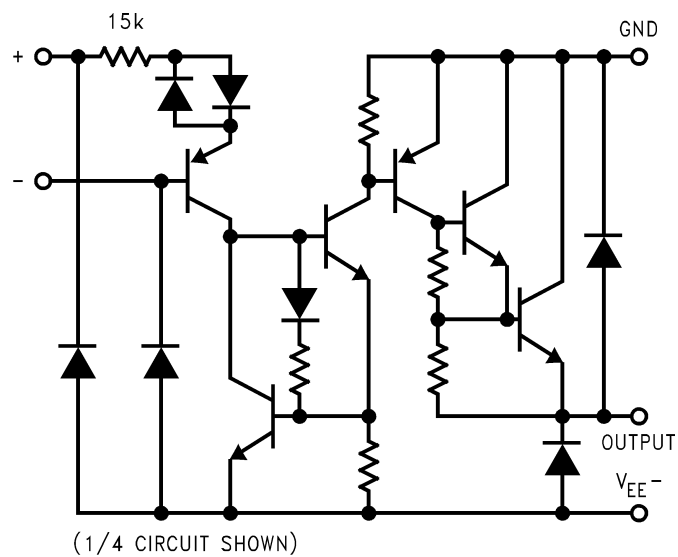
Electrical Characteristics⁽¹⁾⁽²⁾

Parameter	Test Conditions	Min	Typ	Max	Units
V _{IH}	Logic "1" Input Voltage	2.0	1.3		V
V _{IL}	Logic "0" Input Voltage		1.3	0.8	V
I _{INH}	Logic "1" Input Current V _{IN} = 2V V _{IN} = 7V		40 375	100 1000	μA μA
I _{INL}	Logic "0" Input Current V _{IN} = 0.4V V _{IN} = -7V		-0.01 -1	-5 -100	μA μA
V _{OL}	Output ON Voltage I _{OL} = 50 mA		-1.6	-2.1	V
I _{OFF}	Output Leakage V _{OUT} = V _{EE} ⁻		-2	-100	μA
I _{FS}	Fail-Safe Output Leakage V _{OUT} = V _{EE} ⁻ (Inputs Open)		-2	-100	μA
I _{LC}	Output Clamp Leakage Current V _{OUT} = GND		2	100	μA
V _C	Output Clamp Voltage I _{CLAMP} = -50 mA Referenced to V _{EE} ⁻		-2	-1.2	V
V _P	Positive Output Clamp Voltage I _{CLAMP} = 50 mA Referenced to GND		0.9	1.2	V
I _{EE(ON)}	ON Supply Current All Drivers ON		-2	-4.4	mA
I _{EE(OFF)}	OFF Supply Current All Drivers OFF		-1	-100	μA
t _{PD(ON)}	Propagation Delay to Driver ON L = 1h, R _L = 1k, V _{IN} = 3V Pulse		1	10	μs
t _{PD(OFF)}	Propagation Delay to Driver OF L = 1h, R _L = 1k, V _{IN} = 3V Pulse		1	10	μs

- (1) Unless otherwise specified, the min/max limits of the table of "Electrical Characteristics" apply within the range of the [Recommended Operating Conditions](#). All typical values are given for V_{EE}⁻ = 52V, and T_A = 25°C.
- (2) All currents into device pins shown as positive, out of the device as negative. All voltages are referenced to ground unless otherwise noted.

SCHEMATIC DIAGRAMS





REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS3680MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	DS3680M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3680MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

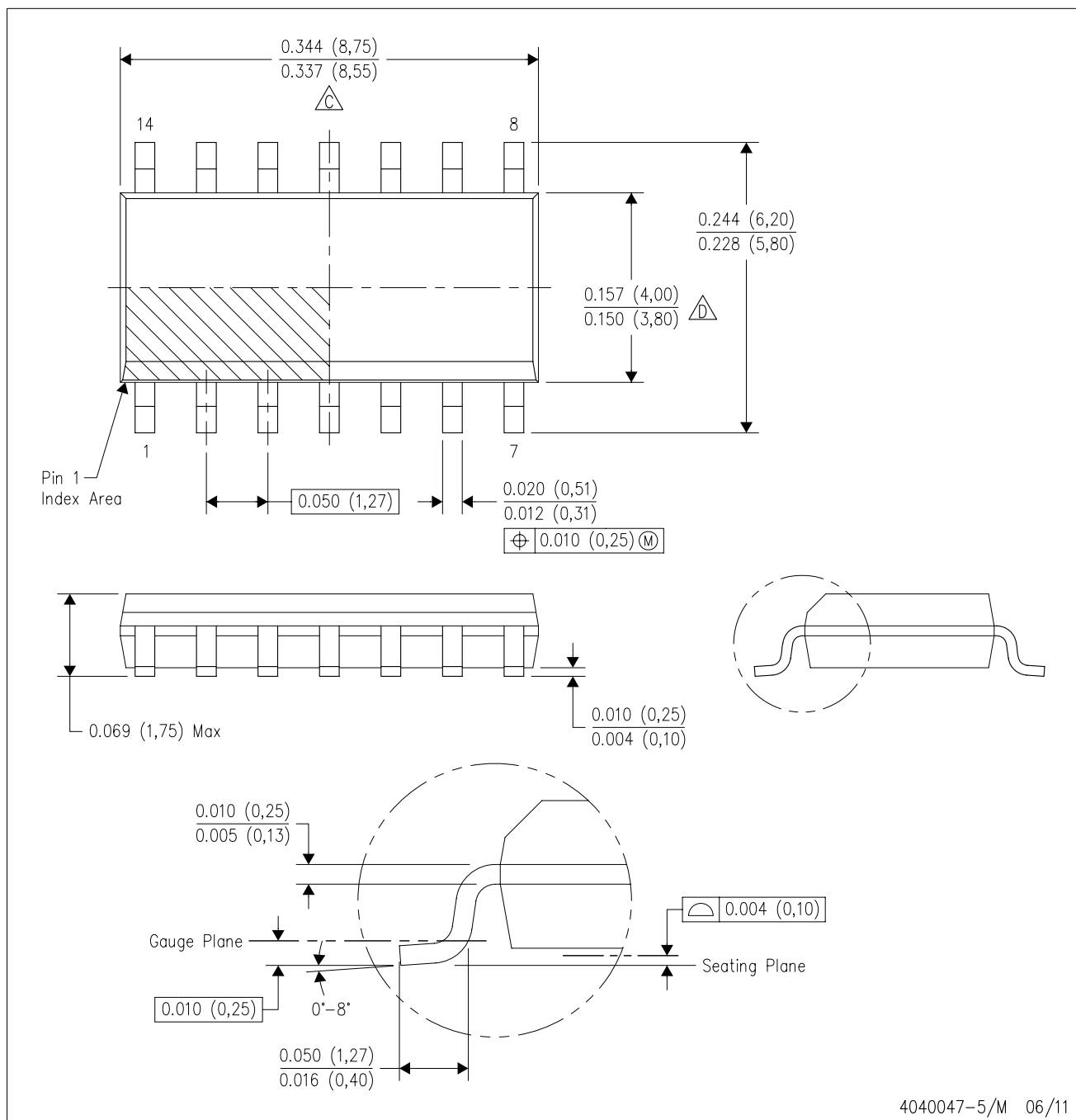


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3680MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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