

TK4P55D

Switching Regulator Applications

- Low drain-source ON-resistance: $R_{DS(ON)} = 1.5 \ \Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 2.0 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 10 \ \mu\text{A}$ (max) ($V_{DS} = 550 \text{ V}$)
- Enhancement-mode: $V_{th} = 2.4$ to 4.4 V ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	550	V
Gate-source voltage		V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	4	A
	Pulse ($t = 1 \text{ ms}$) (Note 1)	I_{DP}	16	
Drain power dissipation ($T_c = 25^\circ\text{C}$)		P_D	80	W
Single pulse avalanche energy (Note 2)		E_{AS}	139	mJ
Avalanche current		I_{AR}	4	A
Repetitive avalanche energy (Note 3)		E_{AR}	8	mJ
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.56	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	125	$^\circ\text{C/W}$

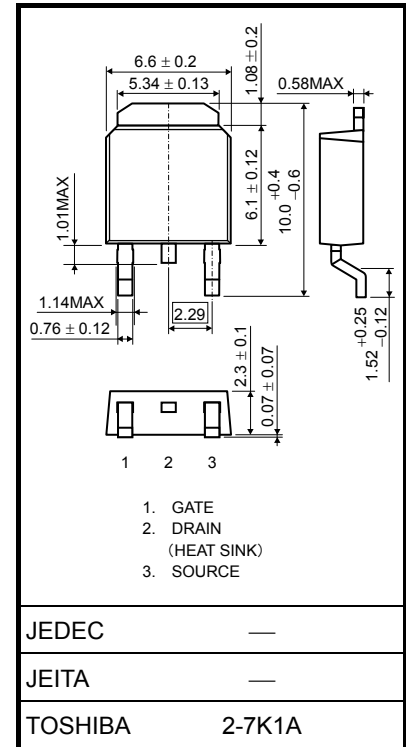
Note 1: Please use devices on conditions that the channel temperature is below 150°C .

Note 2: $V_{DD} = 90 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 15 \text{ mH}$, $R_G = 25 \ \Omega$, $I_{AR} = 4 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

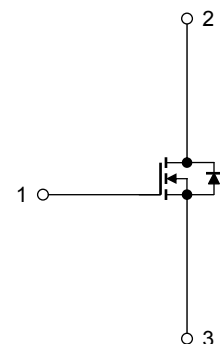
Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-7K1A

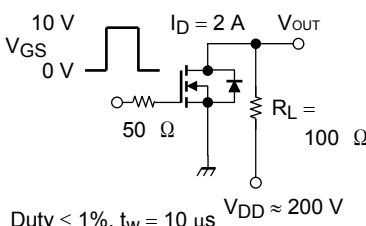
Weight : 0.36 g (typ.)

Internal Connection



Start of commercial production
2009-12

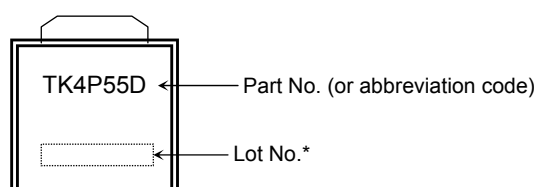
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 550 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	550	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	2.4	—	4.4	V
Drain-source ON-resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$	—	1.5	1.88	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 2 \text{ A}$	0.5	2.0	—	S
Input capacitance		C_{iss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	490	—	pF
Reverse transfer capacitance		C_{rss}		—	3	—	
Output capacitance		C_{oss}		—	55	—	
Switching time	Rise time	t_r		—	18	—	ns
	Turn-on time	t_{on}		—	40	—	
	Fall time	t_f		—	8	—	
	Turn-off time	t_{off}		—	55	—	
Total gate charge		Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	—	11	—	nC
Gate-source charge		Q_{gs}		—	6	—	
Gate-drain charge		Q_{gd}		—	5	—	

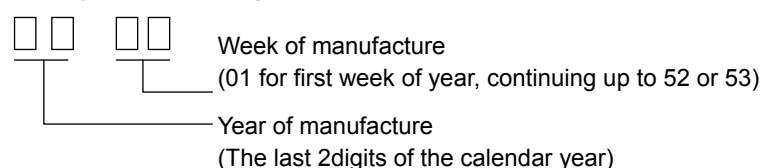
Source-Drain Ratings and Characteristics (Ta = 25°C)

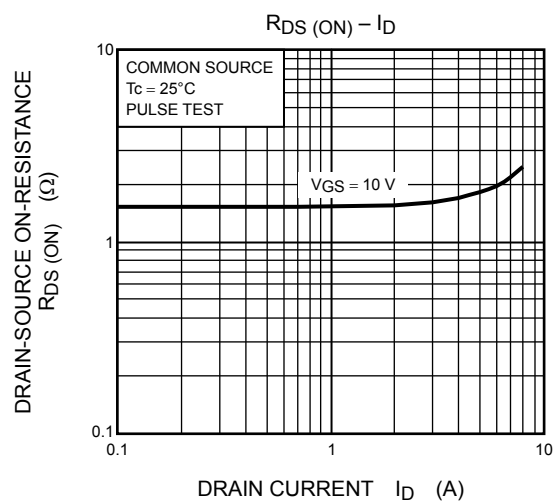
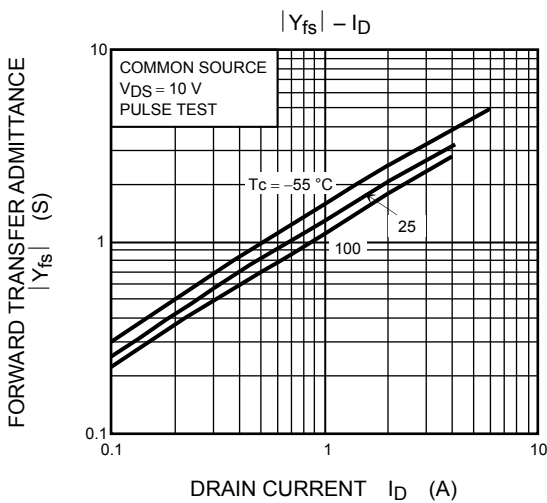
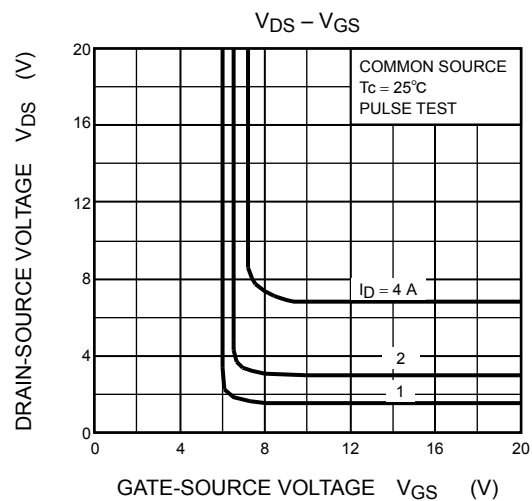
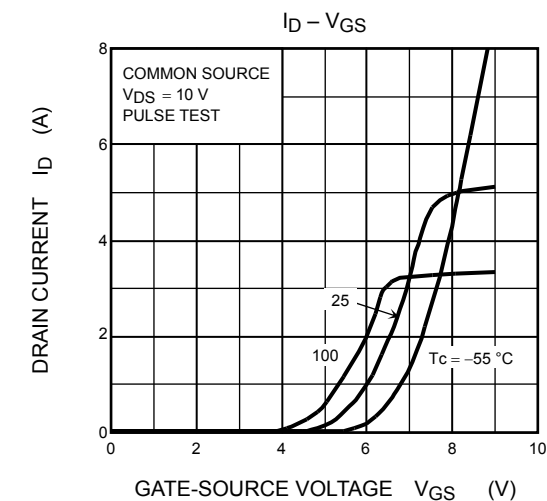
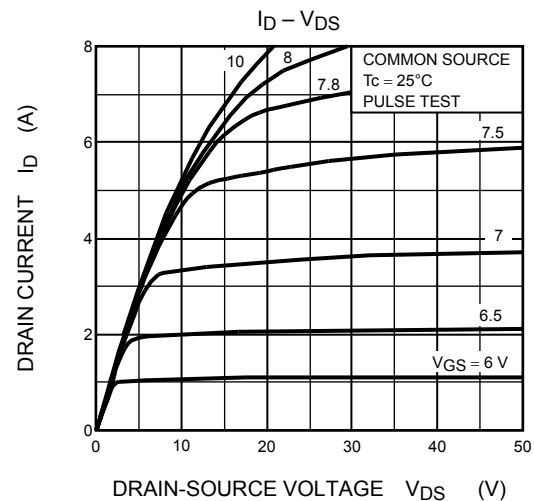
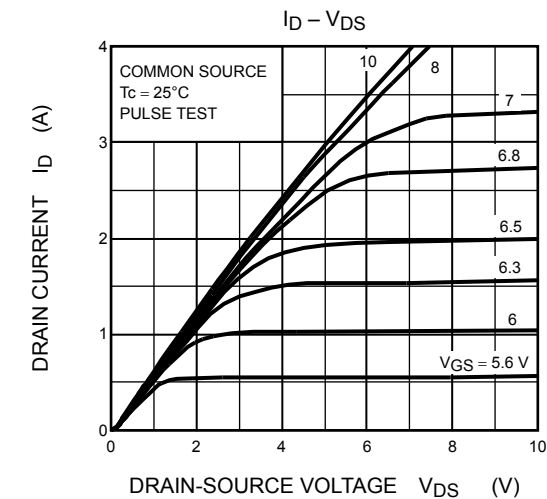
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	4	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	16	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 4 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 4 \text{ A}, V_{GS} = 0 \text{ V},$	—	900	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 100 \text{ A}/\mu\text{s}$	—	5	—	μC

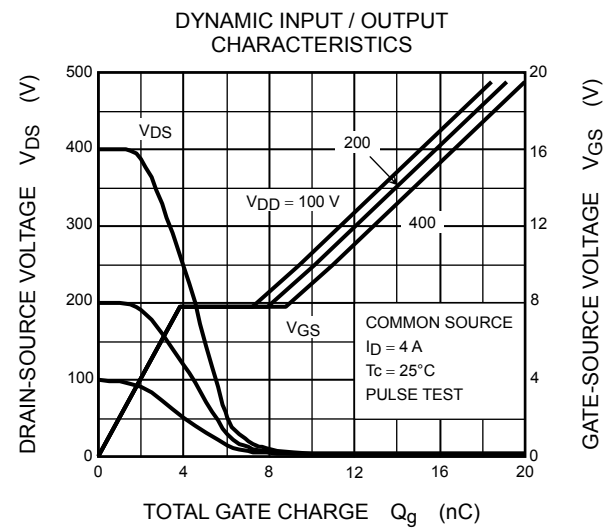
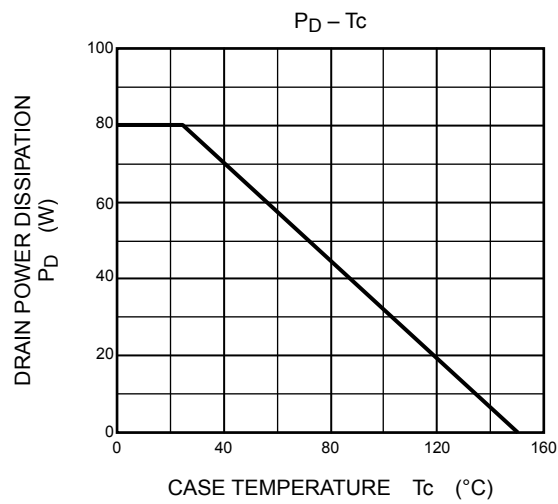
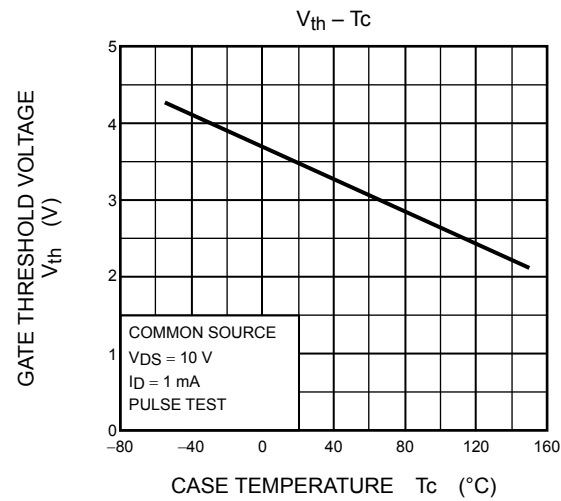
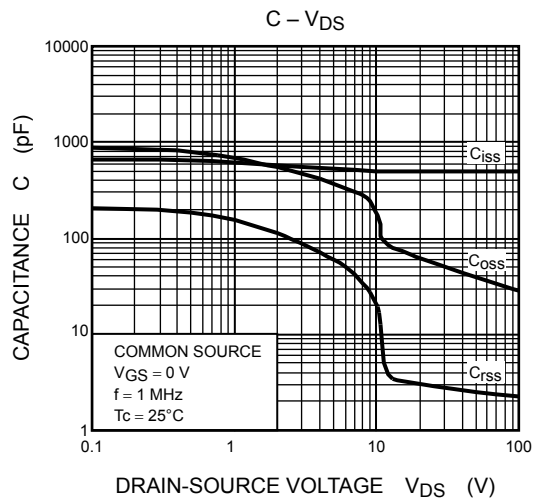
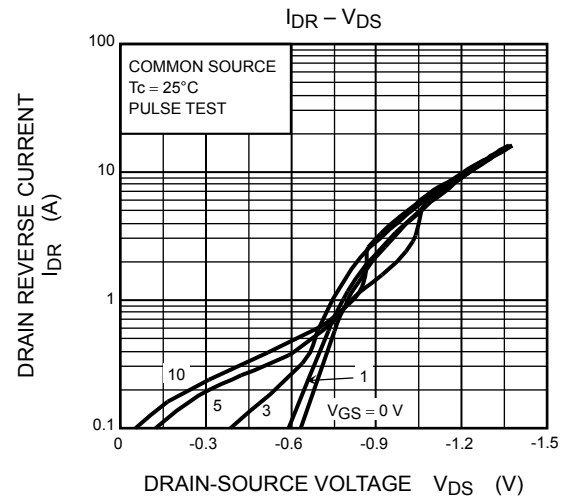
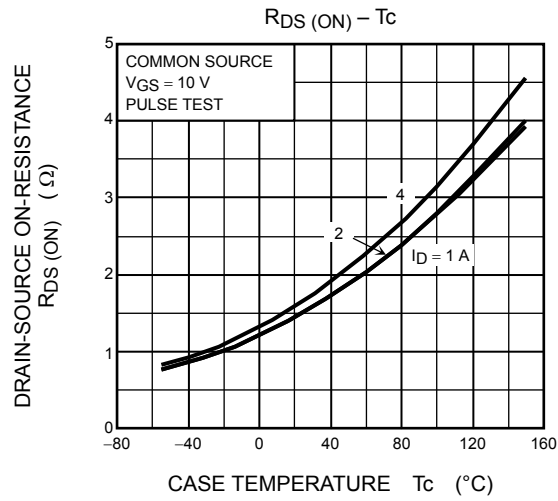
Marking (note 4)

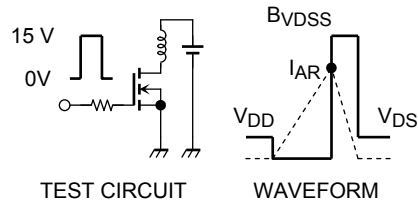
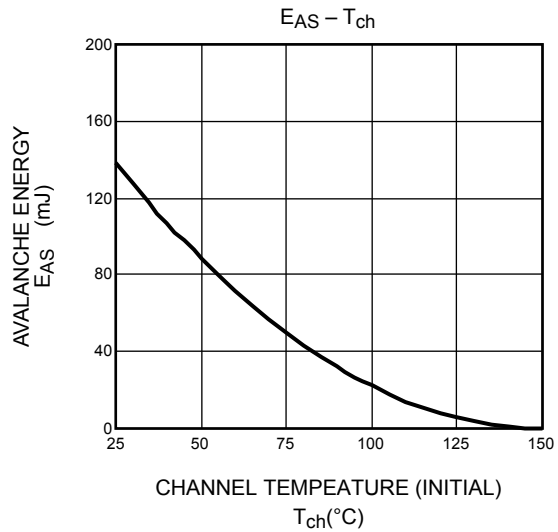
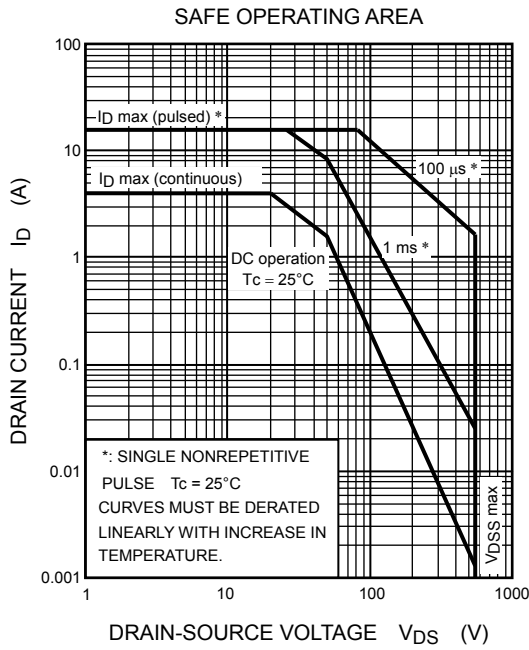
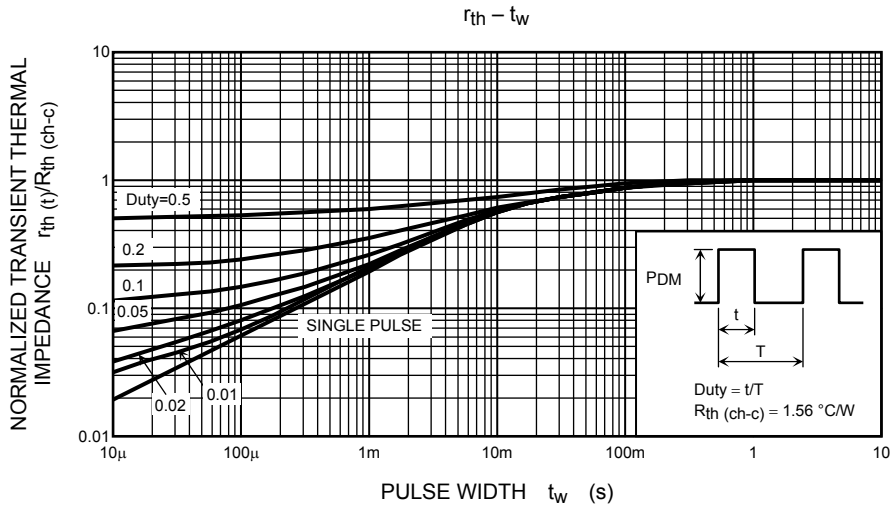


Note 4: * Weekly code: (Four digits)









$$R_G = 25 \, \Omega$$

$$V_{DD} = 90 \, V, L = 15 \, mH$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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