Universal High Side Active ORing Controller IC

Description

The PI2007 *Cool-ORing*® solution is a universal high-speed Active ORing controller IC designed for use with N-channel MOSFETs in redundant power system architectures. The PI2007 *Cool-ORing* controller enables an extremely low power loss solution with fast dynamic response to fault conditions, critical for high availability systems. The PI2007 controls single or parallel MOSFETs to address Active ORing applications protecting against power source failures. The PI2007 has an internal charge pump enabling an ideal solution in 12V or 36-75V bus high-side Active ORing applications.

The gate drive output turns the MOSFET on in normal steady state operation, while achieving high-speed turn-off during input power source fault conditions, that causes reverse current flow. The controller auto-resets once the fault clears. The MOSFET drain-to-source voltage is monitored to detect reverse current flow. The PI2007 has an internal charge pump to drive the gate of a high side N-Channel MOSFET above the VC input. There is an internal shunt regulator at the VC input for high voltage applications.

Features

- Fast dynamic response to power source failure, with 80ns reverse current turn off delay time.
- 4A gate discharge current
- Forward Over Current Fault indication
- Accurate MOSFET drain-to-source voltage sensing
- Internal charge pump
- FET check at initial power-up
- 100V for 100ms, operation in high side application
- VC under voltage fault detection

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- High-side Active ORing
- High current Active ORing

Package Information

The PI2007 is offered in the following packages:

- 10 Lead 3mm x 3mm DFN package

Typical Applications:

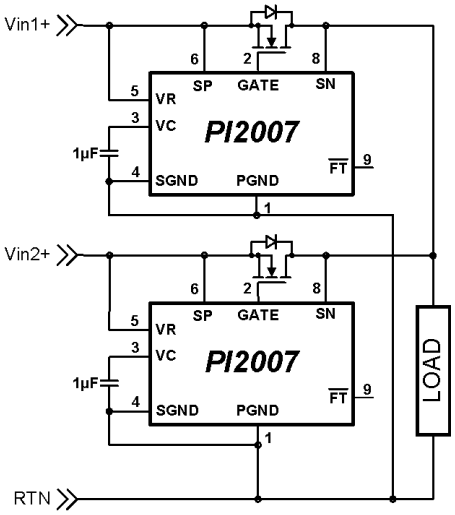


Figure 1: PI2007 High Side Active ORing for 12V Bus applications

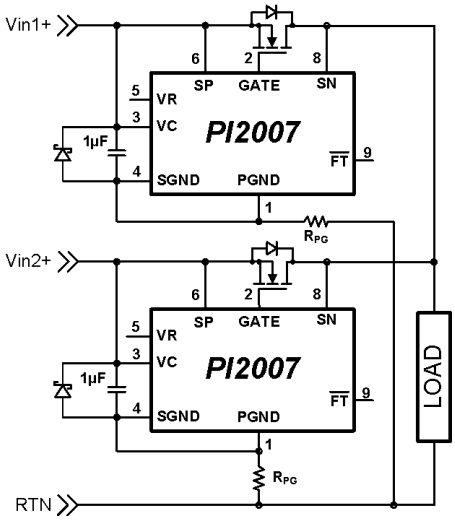
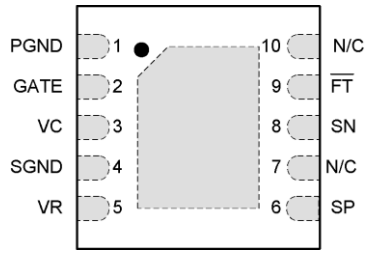


Figure 2: PI2007 referenced to Vin in high voltage high side Active ORing applications

Pin Description

Pin Name	Pin Number	Description
PGND	1	**Gate Turn Off Switch Return:** This pin is the high current return path for the gate driver during turn off. Connect this pin to the low side of the VC coupling capacitor and SGND.
GATE	2	**Gate Drive Output:** This pin drives the gate of the external N-channel MOSFET. Under normal operating conditions and when V_{SP-SN} > 6mV, the GATE pin pulls high to approximately 2*VC with respect to the SGND pin. The controller turns the gate off during a reverse current fault that is below the reverse voltage threshold (-6mV) and when VC is in Under Voltage (7.15V).
VC	3	**Controller Input Supply:** This pin is the supply pin for the control circuitry and gate driver. Connect a 1µF capacitor between the VC pin and the SGND pin. Voltage on this pin is regulated to 11.7V with respect to SGND by an internal shunt regulator. For high voltage supply applications connect a shunt resistor between the SGND and PGND pins and the supply return, as shown in Figure 2.
SGND	4	**VC Return:** This pin is the return (ground) for the control circuitry. Connect this pin to the low side of VC decoupling capacitor.
VR	5	**Controller Input Supply With Limiting Resistor:** This pin is connected internally to VC through a 420Ω resistor needed for Bus voltages greater than 10V and less than 14V. Leave this pin open if unused.
SP	6	**Positive Sense Input:** Connect SP pin to the Source pin of the external N-channel MOSFETs. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
NC	7, 10	**Not Connected:** Leave pins floating.
SN	8	**Negative Sense Input:** Connect SN to the Drain pin of the external N-channel MOSFET. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
$\overline{FT}$	9	**Fault Status Output:** This open collector pin pulls low to indicate one of the several potential fault conditions may exist. The $\overline{FT}$ pin will pull low after a reverse or forward fault has been detected with a defined delay time (8µs). In addition, the $\overline{FT}$ pin will pull low when the controller input voltage is below the VC under-voltage threshold $V_{VC-SGND}$ < 7V. When $V_{VC-SGND}$ > 7.15V and 6mV < V_{SP-SN} < 275mV this pin clears (High). In high voltage applications this output must be translated with reference to the system return with external circuitry, see Figure 19. Leave this pin open if unused.

Package Pin-Outs



10 Lead DFN (3mm x 3mm)
Top view

Absolute Maximum Ratings

Note: All voltage nodes are referenced to SGND

VR	-0.3V to 17.3V / 40mA
SP, $\overline{FT}$	-0.3V to 17.3V / 10mA
GATE	-0.3V to 24V / 5A peak
PGND	-0.3V to 3V / 5A peak
SGND, VC	40mA
SN (Continuous, $T_A \leq 85°C$)	-0.3V to 80V / 10mA
SN (100ms Pulse, $T_A \leq 85°C$)	100V / 10mA
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 140°C
Soldering Temperature for 20 seconds	260°C
ESD Rating	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =10.5V, VR open, C_{Vc} = 1uF, C_{GATE_PGND} = 1nF, SGND=PGND=0V

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VC Supply						
Operating Supply Range (3)	$V_{VC-SGND}$	8.5		10.5	V	No VC limiting Resistor
Quiescent Current	I_{VC}		1.5	2.0	mA	VC = 10.5V
VC Clamp Voltage	V_{VC-CLM}	11	11.7	12.5	V	I_{VC}=3mA
VC Clamp Shunt Resistance	R_{VC}			10	Ω	Delta I_{VC}=10mA
VC Under-Voltage Rising Threshold	V_{VCUVR}	6.1	7.15	8.0	V	
VC Under-Voltage Falling Threshold	V_{VCUVF}	6	7.00	7.9	V	
VC Under-Voltage Hysteresis	$V_{VCUV-HS}$	100	150	200	mV	
VR Supply *(VR pin connected to Vin, VC pin to bypass capacitor Figure 1)* Recommended for 12V Bus applications						
Operating Supply Range	$V_{VR-SGND}$	10		14	V	Biased from VR pin
Quiescent Current	I_{VR}	3.0	5.5	10	mA	VR = 14V
Bias Resistor	R_{Bias}	300	420	550	Ω	
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common Mode Input Voltage	V_{CM}	-3		3	V	SP to VC, SN to VC
Differential Operating Input Voltage(1)	V_{SP-SN}	-80		400	mV	SP-SN
SP Input Bias Current	I_{SP}	35	55	75	µA	SP=SN=VC
SN Input Bias Current	I_{SN}	35	55	75	µA	SP=SN=VC
SN Leakage Current	I_{SN_Lg}		7	9	mA	V_{SN} = 80V,SP=VC=0V

Electrical Specifications (*Continued*)

Unless otherwise specified: -40°C < T_J < 125°C, VC =10.5V, VR open, C_{Vc} = 1uF, C_{GATE_PGND} = 1nF, SGND=PGND=0V

Parameter	Symbol	Min	Typ	Max	Units	Conditions
DIFFERENTIAL AMPLIFIER AND COMPARATORS (Continued)						
Gate Enable Threshold	V_{RVS-EN}	+1	+6	+11	mV	V_{SN} = 10.5V @ 25°C
Reverse Comparator Threshold	V_{RVS-TH}	-11	-6	-2	mV	V_{SN} = 10.5V @ 25°C
Reverse Comparator Hysteresis	V_{RVS-HY}	10	12	14	mV	V_{SN} = 10.5V @ 25°C
Reverse Fault to Gate Turn-off Response Time	t_{RVS}		80	150	ns	V_{SP-SN} = +50mV to -50mV step to 90% of V_G max
Forward Comparator Threshold	V_{FWD-TH}	250	275	300	mV	V_{SN} = 10.5V @ 25°C
Forward Comparator Hysteresis	V_{FWD-HY}	15	25	35	mV	V_{SN} = 10.5V @ 25°C
GATE DRIVER						
Gate Source Current	I_{G-SC}		-20	-15	µA	V_G=V_{G-Hi} –1V, I_{VC}=3mA
Pull Down Peak Current to PGND**(1)**	I_{G-PGND}	1.5	4.0		A	
Pull-down Gate Resistance to PGND**(1)**	R_{G-PGND}		0.3		Ω	V_{G-PGND} = 1.5V @ 25°C
AC Gate Pull-down Voltage to PGND**(1)**	V_{G-PGND}			0.2	V	
DC Gate Pull-down Voltage	V_{G-SGND}		0.8	1.2	V	I_G=100mA, in reverse fault
Gate Drive Voltage to VC	V_{G-Hi}	7.0	8.0	11	V	I_G =-20µA, I_{VC}=3mA
		8.0	9.0	11	V	I_G =-2µA, I_{VC}=3mA
Gate Fall Time	t_{G-F}		10	25	ns	90% to 10% of V_G max.
Gate Voltage	V_{G-UVLO}		0.7	1	V	I_G =10µA, SP= SN=open **VC = 4.5V**
			0.7	1	V	I_G =10µA, SP=0V; **VC=0V** 5.5V ≤ SN ≤ 80V
GATE DRIVER ***(VR pin connected to Vin, VC pin to bypass capacitor Figure 1)***						
Gate Drive Voltage to VR	V_{G-Hi}	4.5	7.0	9.5	V	I_G =-20µA, 10V≤ VR ≤ 14V
		5.0	8.0	9.5	V	I_G =-2µA, 10V≤ VR ≤ 14V
Fault Status: $\overline{FT}$						
Fault Output Low Voltage	$V_{\overline{FT}}$		0.2	0.5	V	I_{FT} =1.5mA, VC > 4.5V
Fault Output High Source Current	I_{FT}	-1			µA	V_{FT}=14V, V_{SP-SN} > +6mV
Fault Delay time	T_{FT-DLY}	4	8	16	µs	V_{SP-SN} = ± 50mV step to 90% of V_{GST} max

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization, and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Refer to the *VC Bias* section in the *Application Information* for details on the VC requirement to meet the MOSFET V_{GS} requirement.

Functional Description:

The PI2007 *Cool-ORing* controller IC is designed to drive single or parallel N-channel MOSFETs in high side Active ORing applications. The PI2007 used with an external MOSFET can function as an ideal ORing diode in the high side of a redundant power system, significantly reducing power dissipation and eliminating the need for heatsinking.

An N-channel MOSFET in the conduction path offers extremely low on-resistance resulting in a dramatic reduction of power dissipation versus the performance of a diode used in conventional ORing applications due to its high forward voltage drop. This can allow for the elimination of complex heat sinking and other thermal management requirements.

Due to the inherent characteristics of the MOSFET, current will flow in the forward and reverse directions while the gate remains above the gate threshold voltage. Ideal ORing applications should not allow reverse current flow, so the controller has to be capable of very fast and accurate detection of reverse current caused by input power source failures, and very fast turn off of the gate of the MOSFET. Once the gate voltage falls below the gate threshold, the MOSFET is off and the body diode will be reverse biased preventing reverse current flow and subsequent excessive voltage droop on the redundant bus.

Differential Amplifier:

The PI2007 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to the Reverse and Forward comparators.

Reverse Current Comparator: RVS

The reverse current comparator provides the critical function in the controller, detecting negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will force the gate discharge circuit to turn off the MOSFETs in typically 80ns.

The reverse comparator will hold the gate low until the SP pin is 6mV higher than the SN pin. The reverse comparator hysteresis is shown in Figure 3.

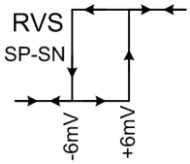


Figure 3: Reverse comparator hysteresis: V_{SP} - V_{SN}

There is a bias current path from SN to SP during the reverse fault condition. The bias current is proportional to the voltage between SN and SP. The maximum SN pin bias current is 9mA when V_{SN}=80V and V_{SP}=0V and assumes that the MOSFET is in the off condition. Refer to Figure 15 in the Application Information section for more details.

Forward Voltage Comparator: FWD

The FWD comparator detects when a forward voltage condition exists and SP is above 275mV (typical) positive with respect to SN. When SP-SN is more than 275mV, the FWD comparator will assert the Gate Status low to report a fault condition.

VC and Internal Voltage Regulator:

The PI2007 has a separate input VC that provides power to the control circuitry, charge pump and gate driver. An internal regulator clamps the VC voltage ($V_{VC-SGND}$) to 11.7V.

The internal regulator circuit has a comparator to monitor the VC voltage and pulls the GATE pin low when the VC is lower than the VC Under-Voltage Threshold.

In 12V Bus applications (10V to 14V) the VR input pin can be connected to the input voltage eliminating the need for an external limiter. An internal 420Ω resistor is connected between the VR pin and the internal regulator VC pin.

Charge Pump:

The PI2007 has an integrated charge pump that approximately doubles the VC voltage with reference to the SGND pin, to drive the N-Channel MOSFET gate to a voltage higher than the input voltage at 15µA minimum source current.

Gate Driver:

The gate driver (GATE) output is configured to drive an external N-channel MOSFET. In the high state, the gate driver applies a 20µA typical current source to the MOSFET gate from the integrated charge pump. The Charge Pump voltage is limited to $2*(V_{VC} - V_{SGND} - 1V)$.

When a reverse current fault is initiated, the gate driver pulls the GATE pin low to the PGND pin and discharges the MOSFET gate with 4A typical peak capability.

Fault Indication: $\overline{FT}$

The $\overline{FT}$ pin is an open collector NPN that will be pulled low when the Gate pin is low. The $\overline{FT}$ pin is also pulled low when $V_{VC-SGND}$ is below UVLO or during the following fault conditions as indicated in the table below:

		Condition	Indication of possible faults
1	Reverse:	$V_{SP} - V_{SN} \leq -6mV$	Input supply shorted
2	Forward:	$V_{SP} - V_{SN} \geq +275mV$	Open FET, Gate short or open, High current
3	Forward	$V_{SP} - V_{SN} \leq +6mV$	Shorted FET on power-up

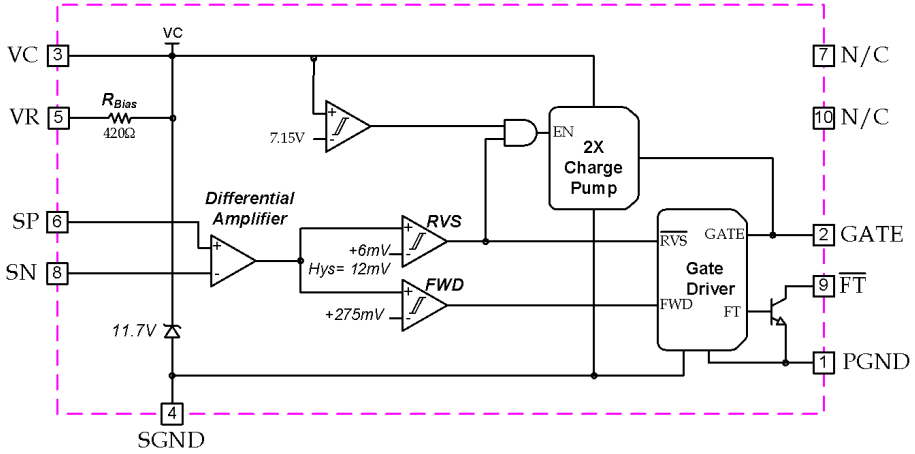


Figure 4: PI2007 Controller Internal Block Diagram

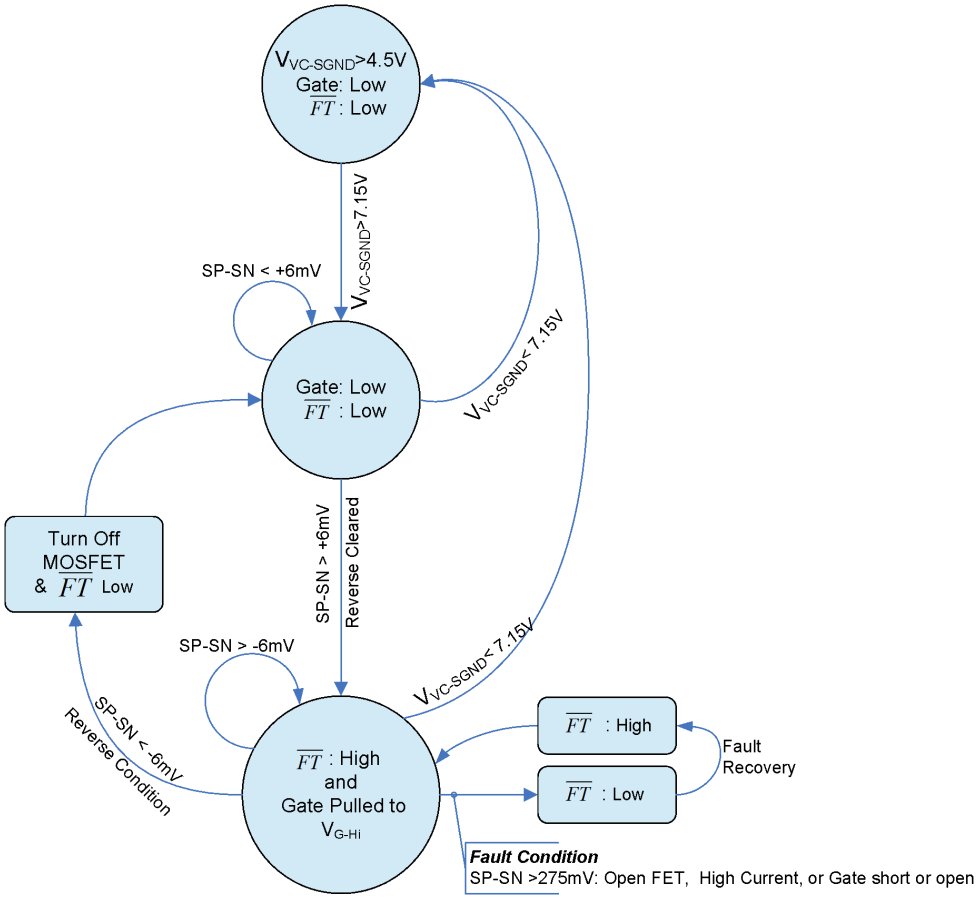


Figure 5: PI2007 State Diagram for gate drive.

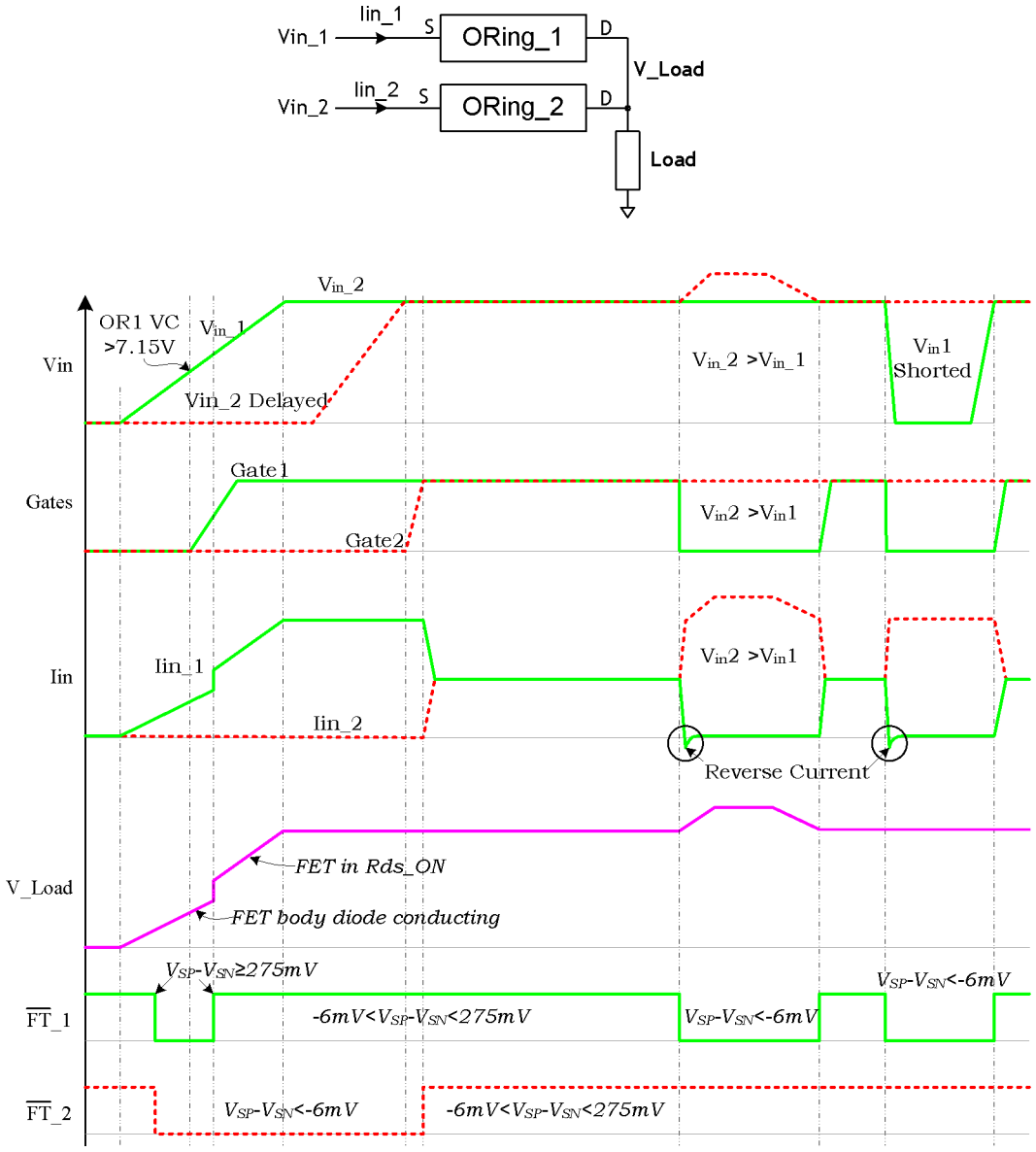


Figure 6: Timing diagram for two PI2007 controllers in a high side Active ORing application

Typical Characteristics:

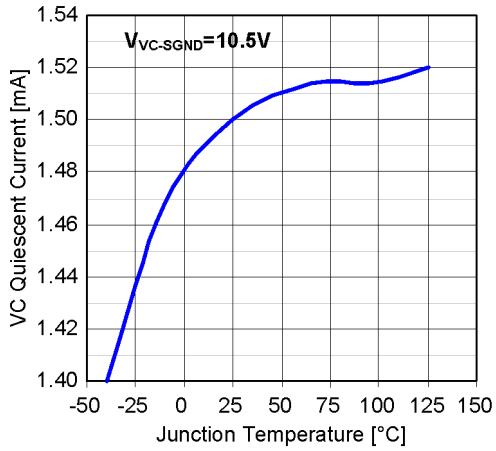


Figure 7: Controller bias current vs. temperature

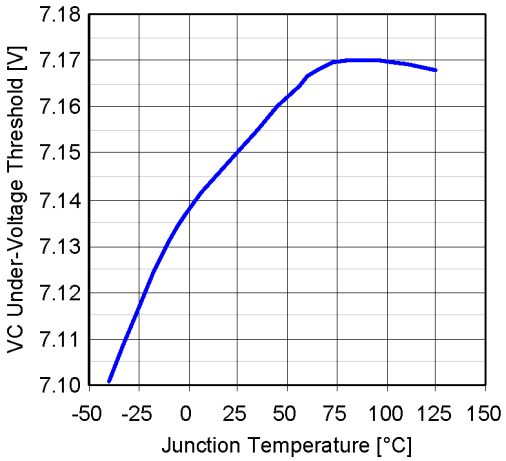


Figure 10: VC UVLO threshold vs. temperature

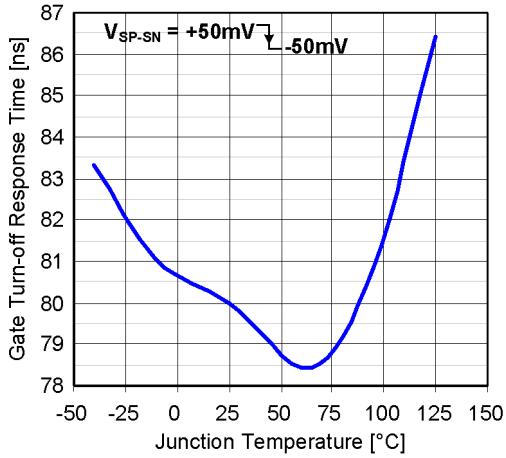


Figure 8: Reverse Fault to Gate Turn-off Response Time vs. temperature.

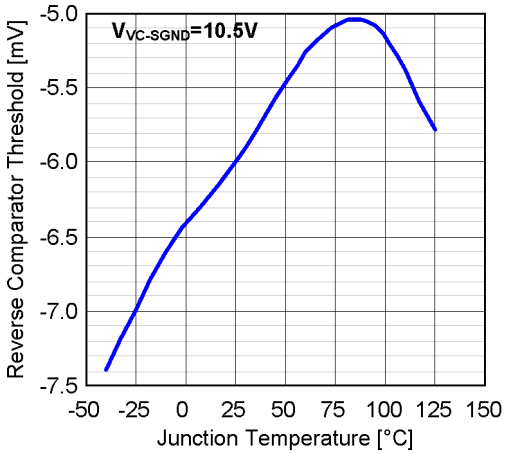


Figure 11: Reverse comparator threshold vs. temperature.

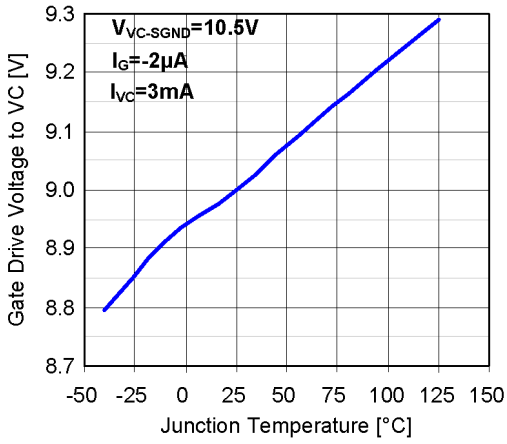


Figure 9: Gate drive voltage to VC vs. temperature.

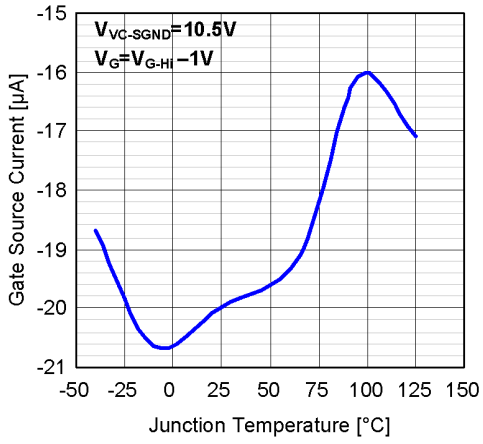


Figure 12: Gate source current vs. temperature

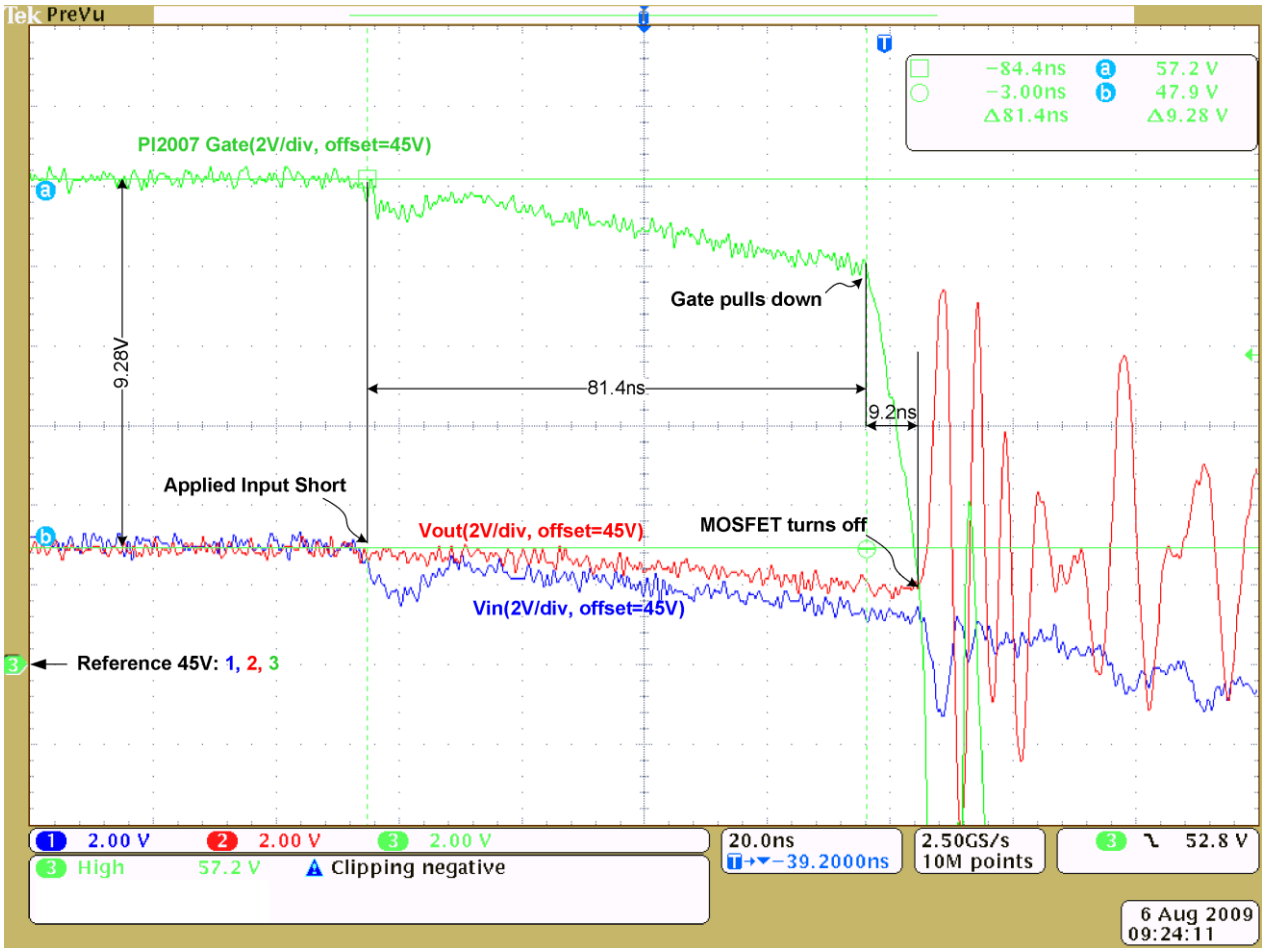


Figure 13: PI2007 performance in response to a fault (input short), configured for a +48V application as shown in Figure 17.

Application Information:

The PI2007 is designed to replace ORing diodes in high current redundant power architectures. Replacing a traditional diode with a PI2007 controller IC and a low on-state resistance N-channel MOSFET will result in significant power dissipation reduction as well as board space reduction, efficiency improvement and additional protection features. This section describes in detail the procedure to follow when designing with the PI2007 Active ORing controller and N-Channel MOSFETs. Two different Active ORing design examples are presented.

VC Bias:

The PI2007 has a separate input (VC) that provides power to the control circuitry, the charge pump and the gate driver. An internal regulator clamps the VC voltage ($V_{VC-SGND}$) to 11.7V. A bypass ceramic capacitor (C_{VC} = 1µF) has to be connected between VC and SGND to hold $V_{VC-SGND}$ steady. Also, the Gate turn off return (PGND) should be connected to SGND at the C_{VC} termination to keep SGND noise free when the Gate is turned off in response to a fault.

In 12V system applications, where the input voltage (Vin) is between 10V and 14V, connect the VR pin to Vin and connect SGND and PGND to the Vin return. A 420Ω internal resistor is connected between the VR pin and the VC pin.

In high voltage applications, above 14V, a bias resistor (R_{PG}) and low current low forward voltage drop Schottky diode are required. Connect one terminal of R_{PG} to the SGND and PGND and the other terminal to ground (Vin return). The Schottky diode anode will be connected to the SGND pin and its cathode connected at the VC pin. See typical application drawings on page 1.

Recommended Schottky:

PMEG3005AEA: from NXP or equivalent

R_{PG} selection for input voltage greater than 14V:

Select the resistor (R_{PG}) value at the minimum input voltage to avoid a voltage drop that may reduce $V_{VC-SGND}$ lower than VC under voltage lockout.

Select the value of R_{PG} using the following equations:

$$R_{PG} = \frac{V_{VC-\min} - V_{VC-CLMMax}}{I_{VC\_Max} + 0.1mA}$$

R_{PG} maximum power dissipation:

$$PdR_{PG} = \frac{(V_{VC-\max} - V_{VC-CLMMin})^2}{R_{PG}}$$

Where:

$V_{VC-\min}$: VC pin minimum applied voltage with respect to Vin return

$V_{VC-\max}$: VC pin maximum applied voltage with respect to Vin return

$V_{VC-CLMMax}$: Controller maximum clamp voltage, 12.5V

$V_{VC-CLMMin}$: Controller minimum clamp voltage, 11.0V

I_{VC_Max}: Controller maximum bias current, use 2.0mA plus 0.1mA for margin

Example: 40V <V_{VC} <50V

$$R_{PG} = \frac{V_{VC\min} - V_{VC-CLMMax}}{I_{VC\_Max} + 0.1mA} = \frac{40V - 12.5V}{2.1mA} = 13.1k\Omega$$

$$PdR_{PG} = \frac{(V_{VC-\max} - V_{VC-CLMMin})^2}{R_{PG}} = \frac{(50V - 11V)^2}{13.1k\Omega} = 116mW$$

Alternative Bias Circuit with Device Enable: *Constant current circuit*

In a wide operating input voltage range the size of R_{PG} may be become large to support power dissipation. A simple constant current circuit can be used instead of R_{PG} to reduce power dissipation and can be used as a device enable.

As shown in Figure 14, the constant current circuit consists of an NPN transistor (Q2), Zener diode D_Z, current limit resistor (R_{LIMIT}) and Zener bias resistor (R_Z). R_{LIMIT} and R_Z can be very low power resistors and Q2 is a signal transistor where its Collector-Emitter Voltage (V_{CEO}) is equal or greater than the input operating voltage and supports 2.5mA at the operating input voltage.

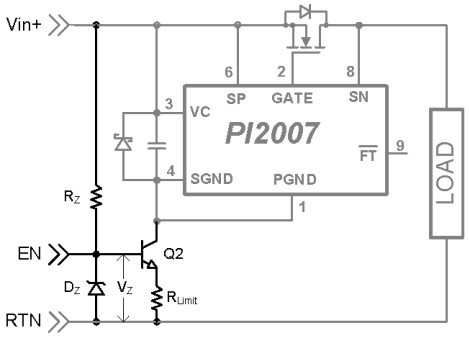


Figure 14: Constant current bias circuit

Pulling the Q2 base (EN) to the system return (RTN) will turn off the transistor and the controller returns (SGND pin and PGND pin) will float and eventually the MOSFET will be turned off. An open collector device can be used to enable and disable the PI2007.

The constant current circuit should guarantee current greater than the PI2007 maximum Quiescent current (I_{VC}), 2.0mA.

R_{LIMIT} can be calculated from the following equation:

$$R_{LIMIT} = \frac{V_{Z\_MIN} - V_{BE}(on)}{I_{VC\_MAX}}$$

Where:

V_{Z_MIN}: Minimum Zener diode voltage

$V_{BE}(on)$: Q2 Base-Emitter On maximum voltage, for default use $V_{BE}(on)$ =0.7V

I_{VC_MAX}: PI2007 Quiescent Current, maximum I_{VC}=2.0mA

Zener Diode Selection:

Select a Zener diode with a low reverse current requirement to minimize R_Z. *Zener diodes with higher break down voltage will have lower reverse current and reduce Q2 collector current variation. Zener diodes with a breakdown voltage of 6V and higher will require low bias current and accurate voltage breakdown.*

R_Z maximum value can be calculated with the following equation:

Note that the surface mount resistors have limited operating voltage capability. Be sure to pick a resistor package that can meet the maximum operating voltage (Vin).

$$R_Z = \frac{V_{in\_MIN} - V_{Z\_MAX}}{I_Z + I_{B\_MAX}}$$

Where:

V_{in_MIN}: Min input voltage

V_{Z_MAX}: Zener diode maximum breakdown voltage

I_Z: Zener diode required reverse current

I_{B_MAX}: Q2 required maximum base current which calculated from the following equation:

$$I_{B\_MAX} = \frac{I_{C\_MAX}}{h_{FE\_MIN}}$$

I_{C_MAX}: Q2 maximum expected collector current.

h_{FE_MIN}: Q2 minimum gain.

Fault Indication:

$\overline{FT}$ is an open collector output and its return is referenced to SGND. When SGND is referenced to system ground, $\overline{FT}$ should be pulled up to the logic voltage via a resistor (10KΩ). When the SGND pin is floating on a bias resistor (R_{PG}) or in a constant current circuit, a level shift circuit can be added to make the $\overline{FT}$ pin output referenced to the system ground. See Figure 19. Leave $\overline{FT}$ unconnected if not used.

Note that in case of an input fault condition, where the input voltage (Vin) and the VC pin are at ground and the SN pin is at a high voltage, a parasitic path between SN and VC will draw bias current (leakage current) from the output as a function of the voltage between SN and grounded VC (V_{SN-GND}) based on the following equation:

$$I_{SN\_Lg} = \frac{V_{SN-GND} - 12V}{R_{PAR}}$$

Where:

I_{SN_Lg}: SN leakage current during input short

V_{SN-GND}: Voltage difference between SN pin (or load voltage) and ground.

R_{PAR}: Resistor in the parasitic path, 10KΩ typical and 8kΩ minimum

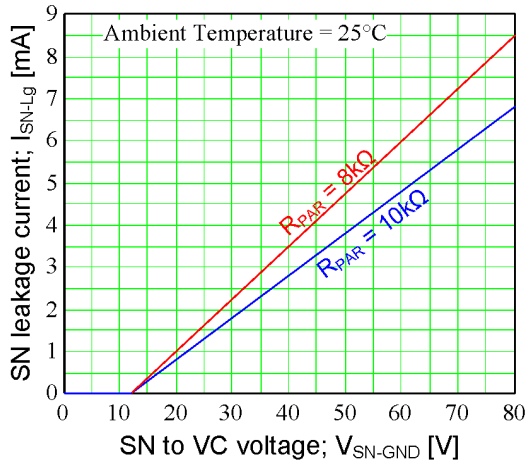


Figure 15: SN leakage current vs. SN voltage during input fault condition (input short)

N-Channel MOSFET Selection:

Several factors affect MOSFET selection including cost, on-state resistance ($R_{DS(on)}$), DC current rating, short pulse current rating, avalanche rating, power dissipation, thermal conductivity, drain-to-source breakdown voltage (BVdss), gate-to-source voltage rating (Vgs), and gate threshold voltage ($Vgs_{(TH)}$).

The first step is to select a suitable MOSFET based on the BVdss requirement for the application. The BVdss voltage rating should be higher than the applied Vin voltage plus expected transient voltages. Stray parasitic inductance in the circuit can also contribute to significant transient voltage conditions, particularly during MOSFET turn-off after a reverse current fault has been detected.

In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from the circuit output through the MOSFET. Depending on the output impedance of the system, the reverse current may get very high in some conditions before the MOSFET is turned off. Make sure that the MOSFET pulse current capability can withstand the peak current. Such high current conditions will store energy even in a small parasitic element. Note that PI2007 has a very fast response time to a fault condition achieving 80ns typical and 150ns maximum. This fast response time will minimize the reverse peak current to keep stored energy and MOSFET avalanche energy very low to avoid damage (breakdown) to the MOSFET.

Peak current during input short is calculated as follows, assuming that the output has very low impedance and it is not a limiting factor:

$$I_{PEAK} = \frac{V_S * t_{RVS}}{L_{PARASITIC}}$$

Where:

I_{PEAK} : Peak current in the MOSFET right before it is turned off.

V_S : Input voltage or load voltage at MOSFET source before input short condition did occur.

t_{RVS} : Reverse fault to MOSFET turn-off time. This will include PI2007 delay and the MOSFET turn off time.

$L_{PARASITIC}$: Circuit parasitic inductance

And the MOSFET avalanche energy during an input short is calculated as follows:

$$E_{AS} = \frac{1}{2} * \frac{1.3 * V_{(BR)DSS}}{*1.3V_{(BR)DSS} - V_S} * L_{PARASITIC} * I_{PEAK}{}^2$$

Where:

E_{AS} : Avalanche energy

$V_{(BR)DSS}$: MOSFET breakdown voltage

MOSFET $R_{DS(on)}$ and maximum steady state power dissipation are closely related. Generally the lower the MOSFET $R_{DS(on)}$, the higher the current capability and the lower the resultant power dissipation. This leads to reduced thermal management overhead, but will ultimately be higher cost compared to higher $R_{DS(on)}$ parts. It is important to understand the primary design goal objectives for the application in order to effectively trade off the performance of one MOSFET versus another.

Power dissipation in active ORing circuits is derived from the total source current and the on-state resistance of the selected MOSFET.

MOSFET power dissipation:

$$Pd_{MOSFET} = Is^2 * R_{DS(on)}$$

Where :
Is : Source Current
$R_{DS(on)}$: MOSFET on-state resistance

Note:
In the calculation use $R_{DS(on)}$ at maximum MOSFET temperature because $R_{DS(on)}$ is temperature dependent. Refer to the normalized $R_{DS(on)}$ curves in the MOSFET manufacturers datasheet. Some MOSFET $R_{DS(on)}$ values may increase by 50% at 125°C compared to values at 25°C.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$Trise_{MOSFET} = Rth_{JA} * Pd_{MOSFET} = Rth_{JA} * Is^2 * R_{DS(on)},$$

Where:
Rth_{JA} : Junction-to-Ambient thermal resistance

$R_{DS(on)}$ and PI2007 sensing:

The PI2007 senses the MOSFET source-to-drain voltage drop via the SP and SN pins to determine the status of the current through the MOSFET. When the MOSFET is fully enhanced, its source-to-drain voltage is equal to the MOSFET on-state resistance multiplied by the source current, $V_{SD} = R_{DS(on)} * Is$. The reverse current threshold is set for -6mV and when the differential voltage between the SP & SN pins is more negative than -6mV, i.e. SP-SN≤-6mV, the PI2007 detects a reverse current fault condition and pulls the MOSFET gate pin low, thus turning off the MOSFET and preventing further reverse current. The reverse current fault protection disconnects the power source fault condition from the redundant bus, and allows the system to keep running.

Typical application Example 1:

Requirement:
Redundant Bus Voltage = 12V (±10%, 10.8V to 13.2V)
Load Current = 15A (assume through each redundant path)
Maximum Ambient Temperature = 75°C

Solution:
A single PI2007 with a suitable external MOSFET for each redundant 12V power source should be used, configured as shown in the circuit schematic in Figure 16.

Select a suitable N-Channel MOSFET: Most industry standard MOSFETs have a Vgs rating of +/- 12V or higher. Select an N-Channel MOSFET with a low $R_{DS(on)}$ which is capable of supporting the full load current with some margin, so a MOSFET capable of at least 18A in steady state is reasonable. An exemplary MOSFET having these characteristic is the FDS6162N7 from Fairchild.

From FDS6162N7 datasheet:

- N-Channel MOSFET
- V_{DS}= 20V
- I_D = 23A continuous drain current
- I_D(Pulse) = 60A Pulsed drain current
- $V_{GS(MAX)}$= ± 12V
- $R_{\theta JA}$= 40°C/W when mounted on a 1in^2 PCB pad of 2 oz copper
- $R_{DS(on)}$=2.9mΩ typical and 3.5mΩ maximum at I_D=23A, V_{GS}≥4.5V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{2.9m\Omega} = -2.07A$$

Power dissipation:
$R_{DS(on)}$ is 3.5mΩ maximum at 25°C & 4.5Vgs and will increase as the temperature increases. Add 25°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (75°C + 25°C) $R_{DS(on)}$ will increase by 28%.

$R_{DS(on)} = 3.5m\Omega * 1.28 = 4.48m\Omega$ maximum at 100°C

$Trise = Rth_{JA} * Is^2 * R_{DS(on)}$

Maximum Junction temperature

$T_{J\max} = T_A + Trise$

$$T_{J\max} = 75°C + \left(\frac{40°C}{W} * (15A)^2 * 4.48m\Omega\right) = 115°C$$

Recalculate based on increased Junction temperature, 115°C.

At 115°C $R_{DS(on)}$ will increase by 32%.

$R_{DS(on)} = 3.5m\Omega * 1.32 = 4.62m\Omega$

$$T_{J\max} = 75°C + \left(\frac{40°C}{W} * (15A)^2 * 4.62m\Omega\right) = 116.5°C$$

VC Bias: Vin maximum input is 13.2V, this is higher than the 11V VC Clamp Voltage ($V_{VC\text{-}SGND}$) minimum. Use the high side PI2007 internal resistor between VR pin and VC pin will fit for this application.

Since the MOSFET requires only 4.5V for full enhancement then the PI2007 internal resistor between VR pin and VC pin will fit for this application. Connect VR to Vin at the source of the MOSFET and connect a 1µF ceramic capacitor between VC pin and SGND pin.

Fault Indication:

Connect $\overline{FT}$ pin to the logic input and to the logic power supply via a 10KΩ resistor.

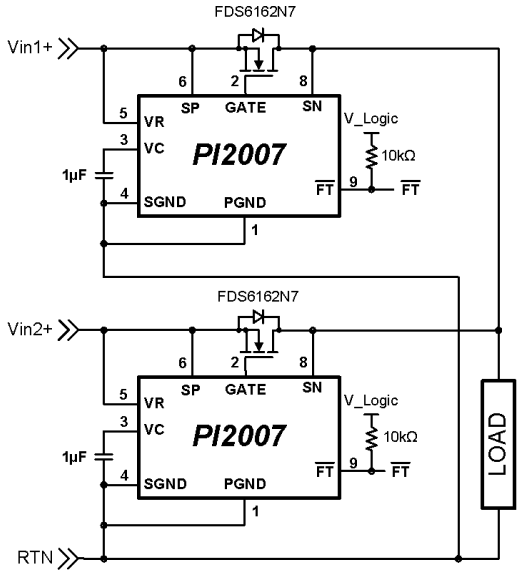


Figure 16: PI2007 in 12V bus high side Active ORing configuration

Typical application Example 2:
Requirement:
+48V High Side Redundant
Bus Voltage = +48V (+36V to +60V, 100V for 100ms transient)
Load Current = 5A load (assume through each redundant path)
Maximum Ambient Temperature = 60°C
Solution:

A single PI2007 with a suitable MOSFET for each redundant +48V power source should be used and configured as shown in Figure 17 or Figure 18. Figure 17 is configured with the VC biased from the return line through a bias resistor. Figure 18 is configured with the VC biased from the return line through the constant current circuit.

Select a suitable N-Channel MOSFET: Select the N-Channel MOSFET with voltage rating higher than the input voltage, Vin, plus any expected transient voltages, with a low $R_{DS(on)}$ that is capable of supporting the full load current with margin. For instance, a 100V rated MOSFET with 10A current capability is suitable. An exemplary MOSFET having these characteristic is IRF7853PbF from International Rectifier.

From the IRF7853PbF datasheet:
N-Channel MOSFET
V_{DS}= 100V
I_D = 8.3A maximum continuous drain current at 25°C
$I_{D\text{-}PULSE}$ = 66A pulsed drain current
$V_{GS(MAX)}$ = ± 20V
$R_{\theta JA}$= 50°C/W on 1in^2 copper, t ≤ 10seconds
$R_{\theta JA}$ for continuous operation not provided
$R_{DS(on)}$=14.4mΩ typical at V_{GS}=10V, T_J=25°C
$R_{DS(on)}$=18mΩ maximum at V_{GS}=10V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{R_{DS(on)}} = \frac{-6mV}{18m\Omega} = -333mA$$

Power dissipation:
Rds(on) is 18mΩ maximum at 25°C & 10Vgs and will increase as the temperature increases. Add 20°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 80°C (60°C + 20°C) Rds(on) will increase by 40%.

$R_{DS(on)} = 18m\Omega * 1.40 = 25.2m\Omega$ maximum at 80°C

Maximum Junction temperature

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 25.2m\Omega\right) = 91.5°C$$

Recalculate maximum $R_{DS(on)}$ at 95°C.
At 95°C Rds(on) will increase by 50%:

$R_{DS(on)} = 18m\Omega * 1.50 = 27m\Omega$ maximum at 95°C

Maximum Junction temperature after 10s

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 27m\Omega\right) = 93.75°C$$

For continuous operation refer the MOSFET datasheet for $R_{\theta JA}$ under continuous operation and plug it in place of 50°C/W.

VC Bias: Since the bus voltage is higher than 14V, connect VC pin to the high side of the input voltage and connect a bias resistor (R_{PG}) or a constant current circuit between PI2007 SGND pin and ground (Vin return), as shown in Figure 17 and Figure 18. Place a low forward voltage drop Schottky diode and a 1µF ceramic capacitor between SGND pin and VC pin. Also connect PGND pin to SGND at the coupling capacitor terminal.

Recommended Schottky: **PMEG3005AEA** from NXP or equivalent

R_{PG} selection:

$$R_{PG} = \frac{V_{VC-\min} - V_{VC-CLMMax}}{I_{VC\_Max} + 0.1mA} = \frac{36V - 12.5V}{2.0mA + 0.1mA} = 11.19k\Omega$$

Select R_{PG}=11kΩ 1%

R_{PG} maximum power dissipation:

$$PdR_{PG} = \frac{(V_{VC-\max} - V_{VC-CLMMin})^2}{R_{PG}} = \frac{(60V - 11V)^2}{11k\Omega} = 218mW$$

Use ¼ W Resistor in 1206 package

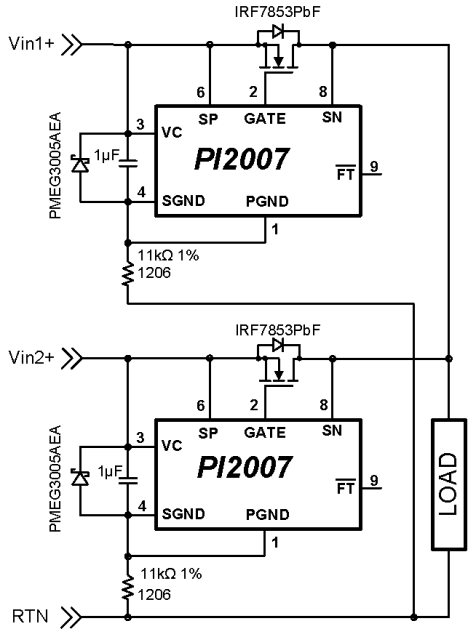


Figure 17: PI2007 in high side +48V application, VC is biased through a bias resistor

VC bias through Constant current circuit

Select an NPN transistor with V_{CEO} equal or higher than the input voltage (Vin) plus any expected transient voltage and capable of handling the expected maximum power dissipation. Any NPN transistor with V_{CEO} ≥ 100V in a small footprint is suitable. An exemplary NPN is FJV1845 from Fairchild:

From the FJV1845 datasheet:
NPN Silicon Transistor
V_{CEO}= 120V Collector-Emitter maximum voltage
I_C = 50mA maximum collector current
h_{FE} = 150 minimum at I_C=3mA
$V_{BE(sat)}$= 0.55V to 0.65V Base-Emitter saturation voltage at 25°C

Select Zener Diode: Select the Zener diode with low bias current, a Zener diode with V_Z=10 in small foot print is suitable for this application. An exemplary Zener diode MM3Z10VST1 from ON Semiconductor

From the MM3Z10VST1 datasheet:
10V, 200mW Zener Diode
V_Z= 9.80V to 10.2V Zener voltage range
I_R = 10µA will hold the Zener breakdown voltage at 9.8V

$$R_{LIMIT} = \frac{V_{Z\_MIN} - V_{BE}(on)}{I_{VC\_MAX}} = \frac{9.8V - 0.7V}{2.1mA} = 4.33k\Omega$$

Or 4.32kΩ 1%

$$I_{B\_MAX} = \frac{I_{C\_MAX}}{h_{FE\_MIN}} = \frac{3.5mA}{150} = 23.33\mu A$$

R_Z Calculation:
Use 100µA as minimum for the Zener diode reverse leakage current and Q2 base current combined.

$$R_Z = \frac{V_{in\_MIN} - V_{Z\_MAX}}{I_Z + I_{B\_MAX}} = \frac{36V - 10.2V}{100\mu A} = 258k\Omega$$

Select R_Z= 249kΩ 1%

Maximum Q2 collector current:

$$I_{C\_MAX} = \frac{V_{Z\_MAX} - V_{BE\_MIN}}{R_{LIMIT\_MIN}} = \frac{10.2V - 0.50V}{4.32k\Omega * 0.98} = 2.29mA$$

Maximum Q2 power dissipation

$$Pd_{Q2} = I_{C\_MAX} \bullet [Vin_{MAX} - V_{VC-CLM} - (V_{Z\_MIN} - V_{EB\_MAX})]$$

$$Pd_{Q2} = 2.29mA \bullet [60V - 11V - (9.8V - 0.7V)] = 91.37mW$$

The transistor Power De-rating vs. temperature curve in the manufacturer datasheet shows that the device can operate up to 110°C.

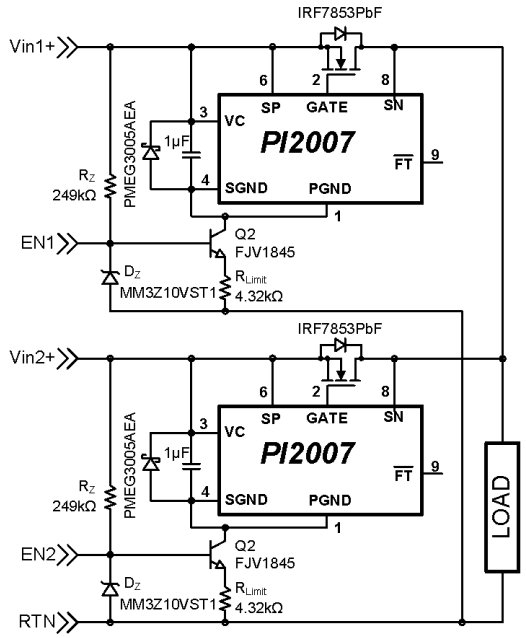


Figure 18: PI2007 in high side +48V application, VC is biased through constant current circuit.

Fault Indication:

PI2007 SGND pin in this application is floating and $\overline{FT}$ is referenced to SGND. The $\overline{FT}$ output can be referenced to system return (RTN) by adding a level shift circuit as shown in Figure 19.

Q1: 2SA1579T106R, 120V PNP transistor from Rohm.

Q2: DTC114EET1G, 50V NPN with bias resistors from ON semiconductor.

D1: 30V general purpose diode.

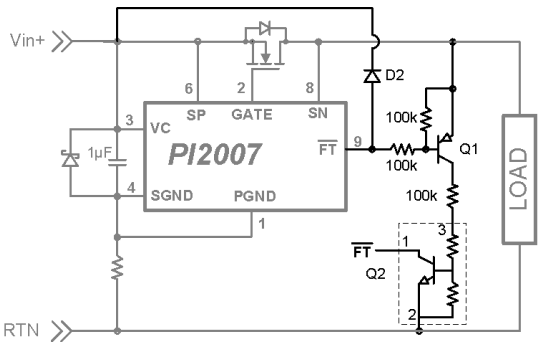


Figure 19: $\overline{FT}$ level shift circuitry

High and Low Side Active ORing for the Same Source:

PI2007 and Picor PI2003 controllers can be configured to meet ATCA application that requires low and high side ORing as shown in Figure 20. See PICOR Application Notes for more details of the design procedure for this application.

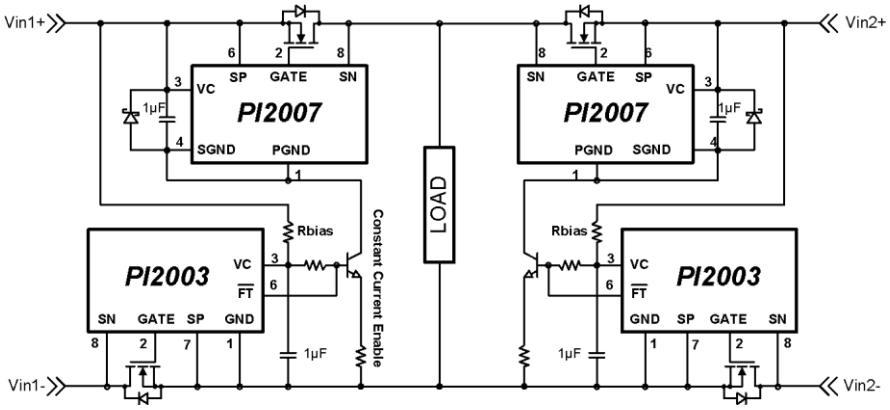


Figure 20: PI2007 and PI2003 configured for a combined high and low side ORing application

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for a DFN PI2007 and SO-8/PowerPak MOSFET is shown in Figure 21 and Figure 22:

- It is best to connect the gate of the MOSFET to the GATE pin of the controller with a short trace. A gate resistor (R_G) is added to slow down the gate turn off if needed.
- The VC bypass capacitor should be located as close as possible to the VC and SGND pins. Place the PI2007 and VC bypass capacitor on the same layer of the board. The VC pin and C_{VC} PCB trace should not contain any vias.
- In an application where SGND is floating, a low forward voltage drop Schottky diode has to be added in parallel with C_{VC} to protect the controller during an input voltage short fault.
- PGND pin of the controller carries high peak current during gate pull down, Connect PGND pin with a wide trace to the C_{VC} terminal at SGND. ***Make sure that SGND trace and PGND trace connect only at C_{VC} terminal.***
- Connections from the SP and SN pins to the MOSFET source and drain pins respectively should be as short as possible
- Connect all MOSFET source pins together with a wide trace to reduce trace parasitics and to accommodate the high current input. Similarly, connect all MOSFET Drain pins together with a wide trace to accommodate the high current output.

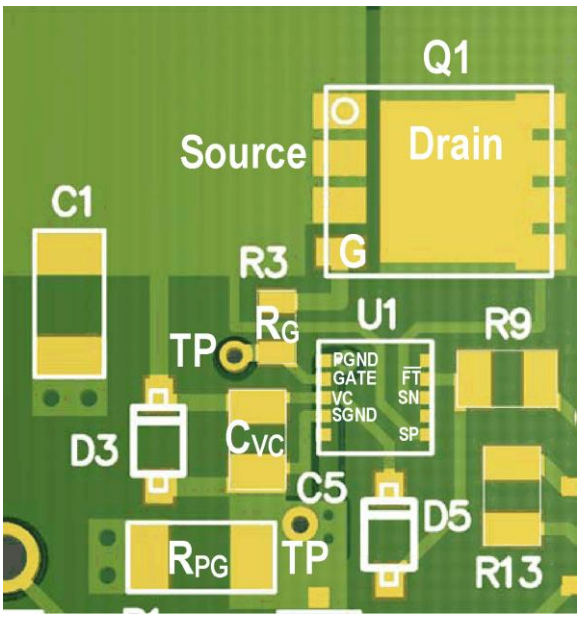


Figure 21: PI2007 controller and MOSFET layout recommendation in a floating application.

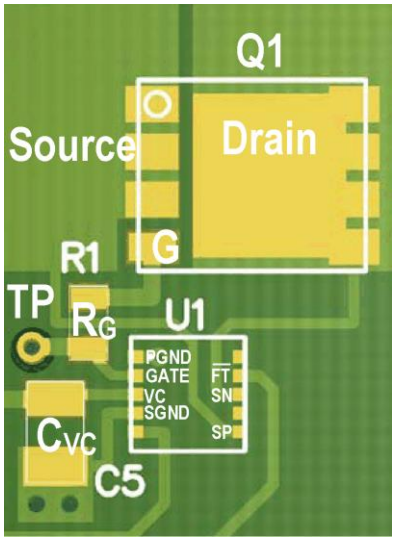
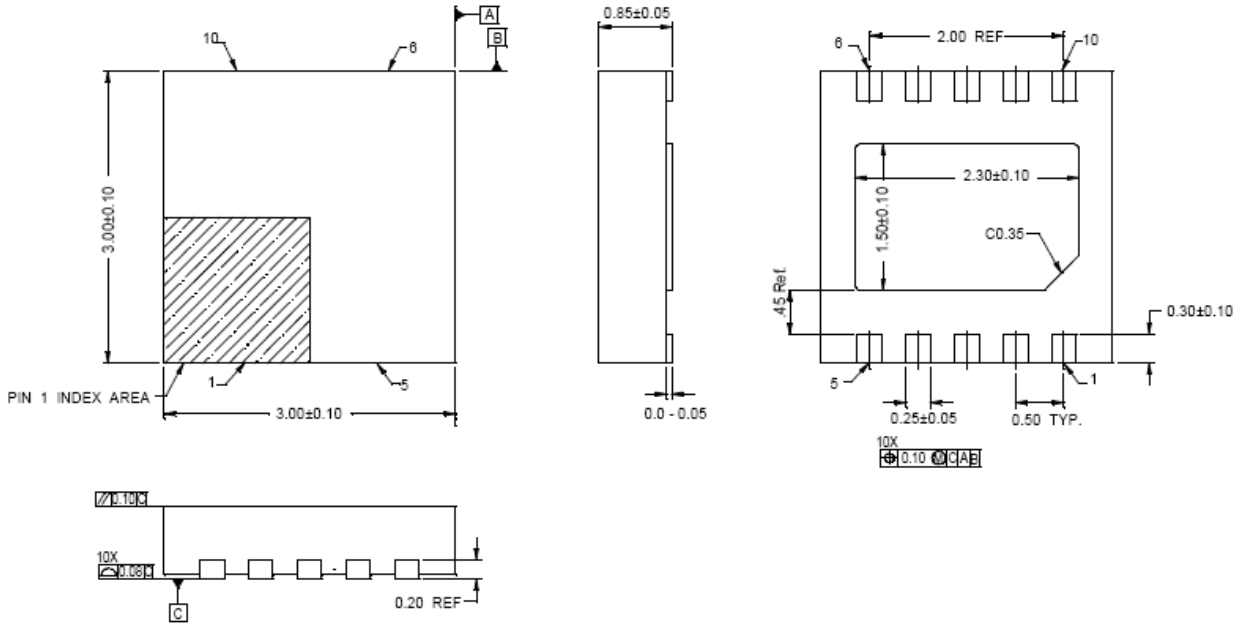


Figure 22: PI2007 controller and MOSFET layout recommendation in a non-floating application

Package Drawing: 10 Lead DFN



NOTES :

1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity does not exceed .05mm
3. Package is variation of JEDEC MO-229
4. Warpage does not exceed .05mm

Thermal Resistance Ratings			
Parameter	**Symbol**	**Typical**	**Unit**
Maximum Junction-to-Ambient (4)	θ_{JA}	53	°C/W

Note 4: In accordance with JEDEC JESD 51

Ordering Information		
Part Number	**Package**	**Transport Media**
PI2007-00-QEIG	3mm x 3mm 10 Lead DFN	T&R

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