

8-CHANNEL HIGH DEFINITION AUDIO CODEC

STAC9227/9228/9228D

Description

The STAC9227/9228/9228D are a family of Theater Quality 8-channel audio CODECs that enable systems with 7.1 audio or 5.1 audio playing simultaneously with VoIP or another stereo audio stream. SigmaTel's proprietary $\Sigma\Delta$ technology provides high fidelity with an estimated DAC SNR up to 105dB. Up to four digital microphones are supported enabling high quality voice input for increased usability of voice applications.

Features

- **High performance HD Audio CODEC provides Theater Quality Audio**
- **High performance $\Sigma\Delta$ technology**
 - 105dB DAC SNR
 - 90dB ADC SNR
- **Four Stereo DACs and three stereo ADCs**
 - Supports 7.1 audio or 5.1 audio with simultaneous Real Time Communication (RTC) channel such as VoIP or separate stereo audio stream
- **24-bit resolution with up to 192 KHz sample rates**
- **Digital Microphone Interface (STAC9228X/D only)**
 - Direct interface up to four Digital Microphones
- **Analog Stereo Microphone**
 - Microphone Boost 0, 10, 20, 30, 40dB
 - Six adjustable Vref outputs for microphone bias
- **Integrated Headphone Amps (3).**
- **S/PDIF In and Out**
- **Volume Up/Down Control**
- **Jack Insertion Detect and Impedance Sensing**
Supports Jack Retasking and Universal Jacks
- **Digital PC Beep to all outputs**
- **+3.3 V to +5 V analog power supply options**
- **Environmental 48-pin LQFP package option**

Software Support

- **SKPI (Kernel Processing Interface)**
 - Enables plug-ins that can operate globally on all audio streams of the system
- **12 band parametric equalizer SKPI plug-in**
 - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode "presets" tailored for specific acoustical environments and applications
 - System-level effects automatically disabled when external connections made
- **Dynamics Processing SKPI plug-in**
 - Enables improved voice articulation
 - Compressor/limiter allows higher average noise level without resonances
- **Dolby Home Theatre (STAC9228D)**
- **Dolby Technologies**
 - Dolby Headphone™, Dolby Virtual Speaker™
 - Dolby ProLogic II™, Dolby ProLogic IIx™
 - Dolby Digital Live™
- **Intel Audio Studio™ from Sonic Focus**
- **Maxx Player™ from Waves**
- **Microphone Beam Forming, Acoustic Echo Cancellation, & Noise Suppression from Knowles™**

TABLE OF CONTENTS

1. DESCRIPTION	14
2. CHARACTERISTICS	15
2.1. Audio Fidelity	15
2.2. Electrical Specifications	15
2.2.1. Absolute Maximum Ratings	15
2.2.2. Recommended Operation Conditions	15
2.3. STAC9227/9228/9228D 5V, 4.5V, 4.0V, and 3.3V Analog Performance Characteristics	17
3. DETAILED DESCRIPTION	22
3.1. Universal Jacks™	22
3.1.1. Audio Jack Presence Detect	22
3.2. Impedance Sense	23
3.3. SPDIF Input	23
3.4. SPDIF Output	23
3.5. Digital Microphone Support (STAC9228X/D)	23
3.6. Analog PC-Beep	27
3.7. Headphone Drivers (Restrictions)	27
3.8. Device IDs	27
4. FUNCTIONAL BLOCK DIAGRAMS	28
5. WIDGET DIAGRAM	29
5.1. Pin Configuration Default Register Settings	30
6. WIDGET INFORMATION FOR THE STAC9227/9228/9228D	31
6.1. Root Node (NID = 0x00)	33
6.1.1. Root ID	33
6.1.2. Root RevID	33
6.1.3. Root NodeInfo	34
6.2. AFG Node (NID = 0x01)	34
6.2.1. AFG Reset	34
6.2.2. AFG NodeInfo	35
6.2.3. AFG Type	35
6.2.4. AFG Cap	36
6.2.5. AFG PCMCap	37
6.2.6. AFG Stream	38
6.2.7. AFG InAmpCap	38
6.2.8. AFG SupPwrState	39
6.2.9. AFG GPIOCnt	39
6.2.10. AFG OutAmpCap	40
6.2.11. AFG PwrState	41
6.2.12. AFG UnsolResp	41
6.2.13. AFG GPIO	42
6.2.14. AFG GPIOEn	43
6.2.15. AFG GPIODir	44
6.2.16. AFG GPIOWakeEn	45
6.2.17. AFG GPIOUnsol	46
6.2.18. AFG GPIOSticky	47
6.2.19. AFG SubID	48
6.2.20. AFG TCKT	49
6.2.21. AFG Sply	49
6.2.22. AFG DACMode	50

6.2.23. AFG GPIOIrty	50
6.2.24. AFG GPIODrive	52
6.2.25. AFG DMic	53
6.3. DAC0 Node (NID = 0x02)	54
6.3.1. DAC0 Cnvtr	54
6.3.2. DAC0 OutAmpRight	55
6.3.3. DAC0 OutAmpLeft	55
6.3.4. DAC0 WCap	56
6.3.5. DAC0 PwrState	57
6.3.6. DAC0 CnvtrID	58
6.3.7. DAC0 LR	58
6.4. DAC1 Node (NID = 0x03)	59
6.4.1. DAC1 Cnvtr	59
6.4.2. DAC1 OutAmpRight	60
6.4.3. DAC1 OutAmpLeft	60
6.4.4. DAC1 WCap	61
6.4.5. DAC1 PwrState	62
6.4.6. DAC1 CnvtrID	63
6.4.7. DAC1 LR	63
6.5. DAC2 Node (NID = 0x04)	64
6.5.1. DAC2 Cnvtr	64
6.5.2. DAC2 OutAmpRight	65
6.5.3. DAC2 OutAmpLeft	65
6.5.4. DAC2 WCap	66
6.5.5. DAC2 PwrState	67
6.5.6. DAC2 CnvtrID	68
6.5.7. DAC2 LR	68
6.6. DAC3 Node (NID = 0x05)	69
6.6.1. DAC3 Cnvtr	69
6.6.2. DAC3 OutAmpRight	70
6.6.3. DAC3 OutAmpLeft	70
6.6.4. DAC3 WCap	71
6.6.5. DAC3 PwrState	72
6.6.6. DAC3 CnvtrID	73
6.6.7. DAC3 LR	73
6.7. DAC4 Node (NID = 0x06)	74
6.7.1. DAC4 Cnvtr	74
6.7.2. DAC4 OutAmpRight	75
6.7.3. DAC4 OutAmpLeft	75
6.7.4. DAC4 WCap	76
6.7.5. DAC4 PwrState	77
6.7.6. DAC4 CnvtrID	78
6.7.7. DAC4 LR	78
6.8. ADC0 Node (NID = 0x07)	79
6.8.1. ADC0 Cnvtr	79
6.8.2. ADC0 WCap	80
6.8.3. ADC0 ConLst	81
6.8.4. ADC0 ConLstEntry	81
6.8.5. ADC0 ProcState	82
6.8.6. ADC0 PwrState	82

6.8.7.	83
6.9. ADC1 Node (NID = 0x08)	84
6.9.1. ADC1 Cnvtr	84
6.9.2. ADC1 WCap	85
6.9.3. ADC1 ConLst	86
6.9.4. ADC1 ConLstEntry	86
6.9.5. ADC1 ProcState	87
6.9.6. ADC1 PwrState	87
6.9.7. ADC1 CnvtrID	88
6.10. ADC2 Node (NID = 0x09)	89
6.10.1. ADC2 Cnvtr	89
6.10.2. ADC2 WCap	90
6.10.3. ADC2 ConLst	91
6.10.4. ADC2 ConLstEntry	91
6.10.5. ADC2 ProcState	92
6.10.6. ADC2 PwrState	92
6.10.7. ADC2 CnvtrID	93
6.11. SPDIFOut Node (NID = 0x1E)	94
6.11.1. SPDIFOut Cnvtr	94
6.11.2. SPDIFOut WCap	95
6.11.3. SPDIFOut PCM	96
6.11.4. SPDIFOut Stream	97
6.11.5. SPDIFOut CnvtrID	98
6.11.6. SPDIFOut DigCnvtr	98
6.12. SPDIFIn Node (NID = 0x20)	99
6.12.1. SPDIFIn Cnvtr	99
6.12.2. SPDIFIn WCap	100
6.12.3. SPDIFIn PCMCap	101
6.12.4. SPDIFIn Stream	102
6.12.5. SPDIFIn ConLst	103
6.12.6. SPDIFIn ConLstEntry	103
6.12.7. SPDIFIn CnvtrID	104
6.12.8. SPDIFIn DigCnvtr	104
6.12.9. SPDIFIn VCSR0	105
6.13. PortA Node (NID = 0x0A)	107
6.13.1. PortA WCap	107
6.13.2. PortA PinCap	108
6.13.3. PortA ConLst	109
6.13.4. PortA ConLstEntry	110
6.13.5. PortA ConSelectCtrl	110
6.13.6. PortA PinWCntrl	110
6.13.7. PortA UnsolvResp	111
6.13.8. PortA ChSense	112
6.13.9. PortA ConfigDefault	112
6.14. PortB Node (NID = 0x0B)	113
6.14.1. PortB WCap	113
6.14.2. PortB PinCap	114
6.14.3. PortB ConLst	115
6.14.4. PortB ConLstEntry	115
6.14.5. PortB ConSelectCtrl	116

6.14.6. PortB PinWCntrl	116
6.14.7. PortB UnsolResp	117
6.14.8. PortB ChSense	118
6.14.9. PortB ConfigDefault	118
6.15. PortC Node (NID = 0x0C)	119
6.15.1. PortC WCap	119
6.15.2. PortC PinCap	120
6.15.3. PortC ConLst	121
6.15.4. PortC ConLstEntry	121
6.15.5. PortC PinWCntrl	122
6.15.6. PortC UnsolResp	122
6.15.7. PortC ChSense	123
6.15.8. PortC ConfigDefault	124
6.16. PortD Node (NID = 0x0D)	124
6.16.1. PortD WCap	124
6.16.2. PortD PinCap	125
6.16.3. PortD ConLst	126
6.16.4. PortD ConLstEntry	127
6.16.5. PortD PinWCntrl	127
6.16.6. PortD UnsolResp	128
6.16.7. PortD ChSense	128
6.16.8. PortD ConfigDefault	129
6.17. PortE Node (NID = 0x0E)	130
6.17.1. PortE WCap	130
6.17.2. PortE PinCap	131
6.17.3. PortE ConLst	132
6.17.4. PortE ConLstEntry	132
6.17.5. PortE PinWCntrl	133
6.17.6. PortE UnsolResp	133
6.17.7. PortE ChSense	134
6.17.8. PortE ConfigDefault	135
6.18. PortF Node (NID = 0x0F)	135
6.18.1. PortF WCap	135
6.18.2. PortF PinCap	136
6.18.3. PortF ConLst	137
6.18.4. PortF ConLstEntry	138
6.18.5. PortF PinWCntrl	138
6.18.6. PortF UnsolResp	139
6.18.7. PortF ChSense	140
6.18.8. PortF ConfigDefault	140
6.19. PortG Node (NID = 0x10)	141
6.19.1. PortG WCap	141
6.19.2. PortG PinCap	142
6.19.3. PortG ConLst	143
6.19.4. PortG ConLstEntry	143
6.19.5. PortG PinWCntrl	144
6.19.6. PortG UnsolResp	144
6.19.7. PortG ChSense	145
6.19.8. PortG ConfigDefault	146
6.20. PortH Node (NID = 0x11)	146

6.20.1. PortH WCap	146
6.20.2. PortH PinCap	147
6.20.3. PortH ConLst	148
6.20.4. PortH ConLstEntry	149
6.20.5. PortH PinWCntrl	149
6.20.6. PortH UnsolvResp	150
6.20.7. PortH ChSense	150
6.20.8. PortH ConfigDefault	151
6.21. DMic0 Node (NID = 0x13)	152
6.21.1. DMic0 WCap	152
6.21.2. DMic0 PinCap	153
6.21.3. DMic0 PinWCntrl	154
6.21.4. DMic0 ConfigDefault	154
6.22. DMic1 Node (NID = 0x14)	155
6.22.1. DMic1 WCap	155
6.22.2. DMic1 PinCap	156
6.22.3. DMic1 PinWCntrl	157
6.22.4. DMic1 ConfigDefault	157
6.23. DigOut0 Node (NID = 0x21)	158
6.23.1. DigOut0 WCap	158
6.23.2. DigOut0 PinCap	159
6.23.3. DigOut0 ConLst	160
6.23.4. DigOut0 ConLstEntry0	160
6.23.5. DigOut0 ConLstEntry4	161
6.23.6. DigOut0 ConSelectCtrl	161
6.23.7. DigOut0 PinWCntrl	162
6.23.8. DigOut0 ConfigDefault	162
6.24. DigIn Node (NID = 0x22)	163
6.24.1. DigIn WCap	163
6.24.2. DigIn PinCap	164
6.24.3. DigIn PwrState	165
6.24.4. DigIn PinWCntrl	165
6.24.5. DigIn UnsolvResp	166
6.24.6. DigIn ChSense	166
6.24.7. DigIn EAPD	167
6.24.8. DigIn ConfigDefault	168
6.25. InPort0Mux Node (NID = 0x15)	168
6.25.1. InPort0Mux WCap	168
6.25.2. InPort0Mux ConLst	169
6.25.3. InPort0Mux OutAmpCap	170
6.25.4. InPort0Mux OutAmpRight	170
6.25.5. InPort0Mux OutAmpLeft	171
6.25.6. InPort0Mux ConSelectCtrl	171
6.25.7. InPort0Mux ConLstEntry0	172
6.25.8. InPort0Mux ConLstEntry4	172
6.25.9. InPort0Mux ConLstEntry8	173
6.26. InPort1Mux Node (NID = 0x16)	173
6.26.1. InPort1Mux WCap	173
6.26.2. InPort1Mux ConLst	174
6.26.3. InPort1Mux OutAmpCap	175

6.26.4. InPort1Mux OutAmpRight	175
6.26.5. InPort1Mux OutAmpLeft	176
6.26.6. InPort1Mux ConSelectCtrl	176
6.26.7. InPort1Mux ConLstEntry0	177
6.26.8. InPort1Mux ConLstEntry4	177
6.26.9. InPort1Mux ConLstEntry8	178
6.27. InPort2Mux Node (NID = 0x17)	178
6.27.1. InPort2Mux WCap	178
6.27.2. InPort2Mux ConLst	179
6.27.3. InPort2Mux OutAmpCap	180
6.27.4. InPort2Mux OutAmpRight	180
6.27.5. InPort2Mux OutAmpLeft	181
6.27.6. InPort2Mux ConSelectCtrl	181
6.27.7. InPort2Mux ConLstEntry0	182
6.27.8. InPort2Mux ConLstEntry4	182
6.27.9. InPort2Mux ConLstEntry8	183
6.28. PCBEEP Node (NID = 0x23)	183
6.28.1. PCBEEP OutAmpLeft	183
6.28.2. PCBEEP WCap	184
6.28.3. PCBEEP OutAmpCap	184
6.28.4. PCBEEP Gen	185
6.29. CD Node (NID = 0x12)	186
6.29.1. CD WCap	186
6.29.2. CD PinCap	187
6.29.3. CD PinWCntrl	188
6.29.4. CD ConfigDefault	189
6.30. Reserved Node (NID = 0x1F)	189
6.31. VolumeKnob Node (NID = 0x24)	189
6.31.1. VolumeKnob WCap	189
6.31.2. VolumeKnob VolKnobCap	190
6.31.3. VolumeKnob ConLst	190
6.31.4. VolumeKnob ConLstEntry0	191
6.31.5. VolumeKnob ConLstEntry4	191
6.31.6. VolumeKnob UnsolResp	192
6.31.7. VolumeKnob Cntrl	192
6.31.8. VolumeKnob VCSR0	193
6.32. InPort0Vol Node (NID = 0x18)	193
6.32.1. InPort0Vol WCap	193
6.32.2. InPort0Vol ConLst	194
6.32.3. InPort0Vol InAmpRight	195
6.32.4. InPort0Vol InAmpLeft	195
6.32.5. InPort0Vol ConLstEntry	196
6.33. InPort1Vol Node (NID = 0x19)	196
6.33.1. InPort1Vol WCap	196
6.33.2. InPort1Vol ConLst	197
6.33.3. InPort1Vol InAmpRight	198
6.33.4. InPort1Vol InAmpLeft	198
6.33.5. InPort1Vol ConLstEntry	198
6.34. InPort2Vol Node (NID = 0x1A)	199
6.34.1. InPort2Vol WCap	199

6.34.2. InPort2Vol ConLst	200
6.34.3. InPort2Vol InAmpRight	200
6.34.4. InPort2Vol InAmpLeft	201
6.34.5. InPort2Vol ConLstEntry	201
6.35. ADC0Mux Node (NID = 0x1B)	202
6.35.1. ADC0Mux WCap	202
6.35.2. ADC0Mux ConLst	203
6.35.3. ADC0Mux ConSelectCtrl	203
6.35.4. ADC0Mux ConLstEntry	203
6.35.5. ADC0Mux LR	204
6.35.6. ADC0Mux OutAmpCap	204
6.35.7. ADC0Mux OutAmpRight	205
6.35.8. ADC0Mux OutAmpLeft	205
6.36. ADC1Mux Node (NID = 0x1C)	206
6.36.1. ADC1Mux WCap	206
6.36.2. ADC1Mux ConLst	207
6.36.3. ADC1Mux ConSelectCtrl	207
6.36.4. ADC1Mux ConLstEntry	208
6.36.5. ADC1Mux LR	208
6.36.6. ADC1Mux OutAmpCap	209
6.36.7. ADC1Mux OutAmpRight	209
6.36.8. ADC1Mux OutAmpLeft	210
6.37. ADC2Mux Node (NID = 0x1D)	210
6.37.1. ADC2Mux WCap	210
6.37.2. ADC2Mux ConLst	211
6.37.3. ADC2Mux ConSelectCtrl	212
6.37.4. ADC2Mux ConLstEntry	212
6.37.5. ADC2Mux LR	213
6.37.6. ADC2Mux OutAmpCap	213
6.37.7. ADC2Mux OutAmpRight	214
6.37.8. ADC2Mux OutAmpLeft	214
7. ORDERING INFORMATION	216
7.1. STAC9227/9228/9228D Options and Part Order Numbers	216
8. PIN INFORMATION	217
8.1. STAC9227/28/29/30 48-Pin LQFP Diagram	217
8.2. Pin Table	218
9. PACKAGE OUTLINE AND PACKAGE DIMENSIONS	220
9.1. 48-Pin LQFP	220
10. SOLDER REFLOW PROFILE	221
10.1. Standard Reflow Profile Data	221
10.2. Pb Free Process - Package Classification Reflow Temperatures	222
11. REVISION HISTORY	223

List of Figures

Figure 1. Single Digital Microphone (data is ported to both left and right channels)	26
Figure 2. Stereo Digital Microphone Configuration	27
Figure 3. Quad Digital Microphone Configuration	28
Figure 4. 48-Pin LQFP Pinout	248
Figure 5. 48-Pin LQFP Package Outline and Package Dimensions	255
Figure 6. Solder Reflow Profile	256

List of Tables

Table 2. Valid Digital Microphone Configurations	30
Table 3. DMIC_CLK, DMIC_0 and DMIC_1 Operation During Power States	30
Table 4. Device IDs	33
Table 5. Pin Configuration Default Settings	37
Table 6. High Definition Audio Widget List	38
Table 7. Root ID Command Verb Format	40
Table 8. Root ID Command Response Format	40
Table 9. Root RevID Command Verb Format	40
Table 10. Root RevID Command Response Format	40
Table 11. Root NodeInfo Command Verb Format	41
Table 12. Root NodeInfo Command Response Format	41
Table 13. AFG Reset Command Verb Format	41
Table 14. AFG Reset Command Response Format	42
Table 15. AFG NodeInfo Command Verb Format	42
Table 16. AFG NodeInfo Command Response Format	42
Table 17. AFG Type Command Verb Format	42
Table 18. AFG Type Command Response Format	43
Table 19. AFG Cap Command Verb Format	43
Table 20. AFG Cap Command Response Format	43
Table 21. AFG PCMCap Command Verb Format	44
Table 22. AFG PCMCap Command Response Format	44
Table 23. AFG Stream Command Verb Format	45
Table 24. AFG Stream Command Response Format	45
Table 25. AFG InAmpCap Command Verb Format	45
Table 26. AFG InAmpCap Command Response Format	45
Table 27. AFG SupPwrState Command Verb Format	46
Table 28. AFG SupPwrState Command Response Format	46
Table 29. AFG GPIOCnt Command Verb Format	46
Table 30. AFG GPIOCnt Command Response Format	47
Table 31. AFG OutAmpCap Command Verb Format	47
Table 32. AFG OutAmpCap Command Response Format	47
Table 33. AFG PwrState Command Verb Format	48
Table 34. AFG PwrState Command Response Format	48
Table 35. AFG UnsolResp Command Verb Format	48
Table 36. AFG UnsolResp Command Response Format	49
Table 37. AFG GPIO Command Verb Format	49
Table 38. AFG GPIO Command Response Format	49
Table 39. AFG GPIOEn Command Verb Format	50
Table 40. AFG GPIOEn Command Response Format	50
Table 41. AFG GPIODir Command Verb Format	51
Table 42. AFG GPIODir Command Response Format	51
Table 43. AFG GPIOWakeEn Command Verb Format	52
Table 44. AFG GPIOWakeEn Command Response Format	52
Table 45. AFG GPIOUnsol Command Verb Format	53
Table 46. AFG GPIOUnsol Command Response Format	53
Table 47. AFG GPIOSticky Command Verb Format	54
Table 48. AFG GPIOSticky Command Response Format	54
Table 49. AFG SubID Command Verb Format	55
Table 50. AFG SubID Command Response Format	55
Table 51. AFG TCKT Command Verb Format	56
Table 52. AFG TCKT Command Response Format	56
Table 53. AFG Sply Command Verb Format	56

Table 54. AFG Sply Command Response Format	56
Table 55. AFG DACMode Command Verb Format	57
Table 56. AFG DACMode Command Response Format	57
Table 57. AFG GPIOIrty Command Verb Format	57
Table 58. AFG GPIOIrty Command Response Format	58
Table 59. AFG GPIODrive Command Verb Format	59
Table 60. AFG GPIODrive Command Response Format	59
Table 61. AFG DMic Command Verb Format	60
Table 62. AFG DMic Command Response Format	60
Table 63. DAC0 Cnvtr Command Verb Format	61
Table 64. DAC0 Cnvtr Command Response Format	61
Table 65. DAC0 OutAmpRight Command Verb Format	62
Table 66. DAC0 OutAmpRight Command Response Format	62
Table 67. DAC0 OutAmpLeft Command Verb Format	62
Table 68. DAC0 OutAmpLeft Command Response Format	63
Table 69. DAC0 WCap Command Verb Format	63
Table 70. DAC0 WCap Command Response Format	63
Table 71. DAC0 PwrState Command Verb Format	64
Table 72. DAC0 PwrState Command Response Format	64
Table 73. DAC0 CnvtrID Command Verb Format	65
Table 74. DAC0 CnvtrID Command Response Format	65
Table 75. DAC0 LR Command Verb Format	65
Table 76. DAC0 LR Command Response Format	65
Table 77. DAC1 Cnvtr Command Verb Format	66
Table 78. DAC1 Cnvtr Command Response Format	66
Table 79. DAC1 OutAmpRight Command Verb Format	67
Table 80. DAC1 OutAmpRight Command Response Format	67
Table 81. DAC1 OutAmpLeft Command Verb Format	67
Table 82. DAC1 OutAmpLeft Command Response Format	68
Table 83. DAC1 WCap Command Verb Format	68
Table 84. DAC1 WCap Command Response Format	68
Table 85. DAC1 PwrState Command Verb Format	69
Table 86. DAC1 PwrState Command Response Format	69
Table 87. DAC1 CnvtrID Command Verb Format	70
Table 88. DAC1 CnvtrID Command Response Format	70
Table 89. DAC1 LR Command Verb Format	70
Table 90. DAC1 LR Command Response Format	70
Table 91. DAC2 Cnvtr Command Verb Format	71
Table 92. DAC2 Cnvtr Command Response Format	71
Table 93. DAC2 OutAmpRight Command Verb Format	72
Table 94. DAC2 OutAmpRight Command Response Format	72
Table 95. DAC2 OutAmpLeft Command Verb Format	72
Table 96. DAC2 OutAmpLeft Command Response Format	73
Table 97. DAC2 WCap Command Verb Format	73
Table 98. DAC2 WCap Command Response Format	73
Table 99. DAC2 PwrState Command Verb Format	74
Table 100. DAC2 PwrState Command Response Format	74
Table 101. DAC2 CnvtrID Command Verb Format	75
Table 102. DAC2 CnvtrID Command Response Format	75
Table 103. DAC2 LR Command Verb Format	75
Table 104. DAC2 LR Command Response Format	75
Table 105. DAC3 Cnvtr Command Verb Format	76
Table 106. DAC3 Cnvtr Command Response Format	76
Table 107. DAC3 OutAmpRight Command Verb Format	77
Table 108. DAC3 OutAmpRight Command Response Format	77
Table 109. DAC3 OutAmpLeft Command Verb Format	77

Table 110. DAC3 OutAmpLeft Command Response Format	78
Table 111. DAC3 WCap Command Verb Format	78
Table 112. DAC3 WCap Command Response Format	78
Table 113. DAC3 PwrState Command Verb Format	79
Table 114. DAC3 PwrState Command Response Format	79
Table 115. DAC3 CnvtrID Command Verb Format	80
Table 116. DAC3 CnvtrID Command Response Format	80
Table 117. DAC3 LR Command Verb Format	80
Table 118. DAC3 LR Command Response Format	80
Table 119. DAC4 Cnvtr Command Verb Format	81
Table 120. DAC4 Cnvtr Command Response Format	81
Table 121. DAC4 OutAmpRight Command Verb Format	82
Table 122. DAC4 OutAmpRight Command Response Format	82
Table 123. DAC4 OutAmpLeft Command Verb Format	82
Table 124. DAC4 OutAmpLeft Command Response Format	83
Table 125. DAC4 WCap Command Verb Format	83
Table 126. DAC4 WCap Command Response Format	83
Table 127. DAC4 PwrState Command Verb Format	84
Table 128. DAC4 PwrState Command Response Format	84
Table 129. DAC4 CnvtrID Command Verb Format	85
Table 130. DAC4 CnvtrID Command Response Format	85
Table 131. DAC4 LR Command Verb Format	85
Table 132. DAC4 LR Command Response Format	85
Table 133. ADC0 Cnvtr Command Verb Format	86
Table 134. ADC0 Cnvtr Command Response Format	86
Table 135. ADC0 WCap Command Verb Format	87
Table 136. ADC0 WCap Command Response Format	87
Table 137. ADC0 ConLst Command Verb Format	88
Table 138. ADC0 ConLst Command Response Format	88
Table 139. ADC0 ConLstEntry Command Verb Format	88
Table 140. ADC0 ConLstEntry Command Response Format	89
Table 141. ADC0 ProcState Command Verb Format	89
Table 142. ADC0 ProcState Command Response Format	89
Table 143. ADC0 PwrState Command Verb Format	89
Table 144. ADC0 PwrState Command Response Format	90
Table 145. ADC0 CnvtrID Command Verb Format	90
Table 146. ADC0 CnvtrID Command Response Format	90
Table 147. ADC1 Cnvtr Command Verb Format	91
Table 148. ADC1 Cnvtr Command Response Format	91
Table 149. ADC1 WCap Command Verb Format	92
Table 150. ADC1 WCap Command Response Format	92
Table 151. ADC1 ConLst Command Verb Format	93
Table 152. ADC1 ConLst Command Response Format	93
Table 153. ADC1 ConLstEntry Command Verb Format	93
Table 154. ADC1 ConLstEntry Command Response Format	94
Table 155. ADC1 ProcState Command Verb Format	94
Table 156. ADC1 ProcState Command Response Format	94
Table 157. ADC1 PwrState Command Verb Format	94
Table 158. ADC1 PwrState Command Response Format	95
Table 159. ADC1 CnvtrID Command Verb Format	95
Table 160. ADC1 CnvtrID Command Response Format	95
Table 161. ADC2 Cnvtr Command Verb Format	96
Table 162. ADC2 Cnvtr Command Response Format	96
Table 163. ADC2 WCap Command Verb Format	97
Table 164. ADC2 WCap Command Response Format	97

Table 165. ADC2 ConLst Command Verb Format	98
Table 166. ADC2 ConLst Command Response Format	98
Table 167. ADC2 ConLstEntry Command Verb Format	98
Table 168. ADC2 ConLstEntry Command Response Format	99
Table 169. ADC2 ProcState Command Verb Format	99
Table 170. ADC2 ProcState Command Response Format	99
Table 171. ADC2 PwrState Command Verb Format	99
Table 172. ADC2 PwrState Command Response Format	100
Table 173. ADC2 CnvtrID Command Verb Format	100
Table 174. ADC2 CnvtrID Command Response Format	100
Table 175. SPDIFOut Cnvtr Command Verb Format	101
Table 176. SPDIFOut Cnvtr Command Response Format	101
Table 177. SPDIFOut WCap Command Verb Format	102
Table 178. SPDIFOut WCap Command Response Format	102
Table 179. SPDIFOut PCM Command Verb Format	103
Table 180. SPDIFOut PCM Command Response Format	103
Table 181. SPDIFOut Stream Command Verb Format	104
Table 182. SPDIFOut Stream Command Response Format	104
Table 183. SPDIFOut CnvtrID Command Verb Format	105
Table 184. SPDIFOut CnvtrID Command Response Format	105
Table 185. SPDIFOut DigCnvtr Command Verb Format	105
Table 186. SPDIFOut DigCnvtr Command Response Format	105
Table 187. SPDIFIn Cnvtr Command Verb Format	106
Table 188. SPDIFIn Cnvtr Command Response Format	106
Table 189. SPDIFIn WCap Command Verb Format	107
Table 190. SPDIFIn WCap Command Response Format	108
Table 191. SPDIFIn PCMCap Command Verb Format	108
Table 192. SPDIFIn PCMCap Command Response Format	109
Table 193. SPDIFIn Stream Command Verb Format	109
Table 194. SPDIFIn Stream Command Response Format	110
Table 195. SPDIFIn ConLst Command Verb Format	110
Table 196. SPDIFIn ConLst Command Response Format	110
Table 197. SPDIFIn ConLstEntry Command Verb Format	110
Table 198. SPDIFIn ConLstEntry Command Response Format	110
Table 199. SPDIFIn CnvtrID Command Verb Format	111
Table 200. SPDIFIn CnvtrID Command Response Format	111
Table 201. SPDIFIn DigCnvtr Command Verb Format	111
Table 202. SPDIFIn DigCnvtr Command Response Format	112
Table 203. SPDIFIn VCSR0 Command Verb Format	112
Table 204. SPDIFIn VCSR0 Command Response Format	112
Table 205. PortA WCap Command Verb Format	114
Table 206. PortA WCap Command Response Format	114
Table 207. PortA PinCap Command Verb Format	115
Table 208. PortA PinCap Command Response Format	115
Table 209. PortA ConLst Command Verb Format	116
Table 210. PortA ConLst Command Response Format	116
Table 211. PortA ConLstEntry Command Verb Format	117
Table 212. PortA ConLstEntry Command Response Format	117
Table 213. PortA ConSelectCtrl Command Verb Format	117
Table 214. PortA ConSelectCtrl Command Response Format	117
Table 215. PortA PinWCntrl Command Verb Format	117
Table 216. PortA PinWCntrl Command Response Format	118
Table 217. PortA UnsolResp Command Verb Format	118
Table 218. PortA UnsolResp Command Response Format	118
Table 219. PortA ChSense Command Verb Format	119

Table 220. PortA ChSense Command Response Format	119
Table 221. PortA ConfigDefault Command Verb Format	119
Table 222. PortA ConfigDefault Command Response Format	120
Table 223. PortB WCap Command Verb Format	120
Table 224. PortB WCap Command Response Format	120
Table 225. PortB PinCap Command Verb Format	121
Table 226. PortB PinCap Command Response Format	121
Table 227. PortB ConLst Command Verb Format	122
Table 228. PortB ConLst Command Response Format	122
Table 229. PortB ConLstEntry Command Verb Format	122
Table 230. PortB ConLstEntry Command Response Format	123
Table 231. PortB ConSelectCtrl Command Verb Format	123
Table 232. PortB ConSelectCtrl Command Response Format	123
Table 233. PortB PinWCntrl Command Verb Format	123
Table 234. PortB PinWCntrl Command Response Format	124
Table 235. PortB UnsolResp Command Verb Format	124
Table 236. PortB UnsolResp Command Response Format	124
Table 237. PortB ChSense Command Verb Format	125
Table 238. PortB ChSense Command Response Format	125
Table 239. PortB ConfigDefault Command Verb Format	125
Table 240. PortB ConfigDefault Command Response Format	126
Table 241. PortC WCap Command Verb Format	126
Table 242. PortC WCap Command Response Format	126
Table 243. PortC PinCap Command Verb Format	127
Table 244. PortC PinCap Command Response Format	127
Table 245. PortC ConLst Command Verb Format	128
Table 246. PortC ConLst Command Response Format	128
Table 247. PortC ConLstEntry Command Verb Format	128
Table 248. PortC ConLstEntry Command Response Format	128
Table 249. PortC PinWCntrl Command Verb Format	129
Table 250. PortC PinWCntrl Command Response Format	129
Table 251. PortC UnsolResp Command Verb Format	129
Table 252. PortC UnsolResp Command Response Format	130
Table 253. PortC ChSense Command Verb Format	130
Table 254. PortC ChSense Command Response Format	130
Table 255. PortC ConfigDefault Command Verb Format	131
Table 256. PortC ConfigDefault Command Response Format	131
Table 257. PortD WCap Command Verb Format	131
Table 258. PortD WCap Command Response Format	132
Table 259. PortD PinCap Command Verb Format	132
Table 260. PortD PinCap Command Response Format	133
Table 261. PortD ConLst Command Verb Format	133
Table 262. PortD ConLst Command Response Format	133
Table 263. PortD ConLstEntry Command Verb Format	134
Table 264. PortD ConLstEntry Command Response Format	134
Table 265. PortD PinWCntrl Command Verb Format	134
Table 266. PortD PinWCntrl Command Response Format	134
Table 267. PortD UnsolResp Command Verb Format	135
Table 268. PortD UnsolResp Command Response Format	135
Table 269. PortD ChSense Command Verb Format	135
Table 270. PortD ChSense Command Response Format	136
Table 271. PortD ConfigDefault Command Verb Format	136
Table 272. PortD ConfigDefault Command Response Format	137
Table 273. PortE WCap Command Verb Format	137
Table 274. PortE WCap Command Response Format	137

Table 275. PortE PinCap Command Verb Format	138
Table 276. PortE PinCap Command Response Format	138
Table 277. PortE ConLst Command Verb Format	139
Table 278. PortE ConLst Command Response Format	139
Table 279. PortE ConLstEntry Command Verb Format	139
Table 280. PortE ConLstEntry Command Response Format	139
Table 281. PortE PinWCntrl Command Verb Format	140
Table 282. PortE PinWCntrl Command Response Format	140
Table 283. PortE UnsolResp Command Verb Format	140
Table 284. PortE UnsolResp Command Response Format	141
Table 285. PortE ChSense Command Verb Format	141
Table 286. PortE ChSense Command Response Format	141
Table 287. PortE ConfigDefault Command Verb Format	142
Table 288. PortE ConfigDefault Command Response Format	142
Table 289. PortF WCap Command Verb Format	142
Table 290. PortF WCap Command Response Format	143
Table 291. PortF PinCap Command Verb Format	143
Table 292. PortF PinCap Command Response Format	144
Table 293. PortF ConLst Command Verb Format	144
Table 294. PortF ConLst Command Response Format	144
Table 295. PortF ConLstEntry Command Verb Format	145
Table 296. PortF ConLstEntry Command Response Format	145
Table 297. PortF PinWCntrl Command Verb Format	145
Table 298. PortF PinWCntrl Command Response Format	145
Table 299. PortF UnsolResp Command Verb Format	146
Table 300. PortF UnsolResp Command Response Format	146
Table 301. PortF ChSense Command Verb Format	147
Table 302. PortF ChSense Command Response Format	147
Table 303. PortF ConfigDefault Command Verb Format	147
Table 304. PortF ConfigDefault Command Response Format	148
Table 305. PortG WCap Command Verb Format	148
Table 306. PortG WCap Command Response Format	148
Table 307. PortG PinCap Command Verb Format	149
Table 308. PortG PinCap Command Response Format	149
Table 309. PortG ConLst Command Verb Format	150
Table 310. PortG ConLst Command Response Format	150
Table 311. PortG ConLstEntry Command Verb Format	150
Table 312. PortG ConLstEntry Command Response Format	150
Table 313. PortG PinWCntrl Command Verb Format	151
Table 314. PortG PinWCntrl Command Response Format	151
Table 315. PortG UnsolResp Command Verb Format	151
Table 316. PortG UnsolResp Command Response Format	152
Table 317. PortG ChSense Command Verb Format	152
Table 318. PortG ChSense Command Response Format	152
Table 319. PortG ConfigDefault Command Verb Format	153
Table 320. PortG ConfigDefault Command Response Format	153
Table 321. PortH WCap Command Verb Format	153
Table 322. PortH WCap Command Response Format	154
Table 323. PortH PinCap Command Verb Format	154
Table 324. PortH PinCap Command Response Format	155
Table 325. PortH ConLst Command Verb Format	155
Table 326. PortH ConLst Command Response Format	155
Table 327. PortH ConLstEntry Command Verb Format	156
Table 328. PortH ConLstEntry Command Response Format	156
Table 329. PortH PinWCntrl Command Verb Format	156

Table 330. PortH PinWCntrl Command Response Format	156
Table 331. PortH UnsolResp Command Verb Format	157
Table 332. PortH UnsolResp Command Response Format	157
Table 333. PortH ChSense Command Verb Format	157
Table 334. PortH ChSense Command Response Format	158
Table 335. PortH ConfigDefault Command Verb Format	158
Table 336. PortH ConfigDefault Command Response Format	158
Table 337. DMic0 WCap Command Verb Format	159
Table 338. DMic0 WCap Command Response Format	159
Table 339. DMic0 PinCap Command Verb Format	160
Table 340. DMic0 PinCap Command Response Format	160
Table 341. DMic0 PinWCntrl Command Verb Format	161
Table 342. DMic0 PinWCntrl Command Response Format	161
Table 343. DMic0 ConfigDefault Command Verb Format	161
Table 344. DMic0 ConfigDefault Command Response Format	161
Table 345. DMic1 WCap Command Verb Format	162
Table 346. DMic1 WCap Command Response Format	162
Table 347. DMic1 PinCap Command Verb Format	163
Table 348. DMic1 PinCap Command Response Format	163
Table 349. DMic1 PinWCntrl Command Verb Format	164
Table 350. DMic1 PinWCntrl Command Response Format	164
Table 351. DMic1 ConfigDefault Command Verb Format	164
Table 352. DMic1 ConfigDefault Command Response Format	165
Table 353. DigOut0 WCap Command Verb Format	165
Table 354. DigOut0 WCap Command Response Format	165
Table 355. DigOut0 PinCap Command Verb Format	166
Table 356. DigOut0 PinCap Command Response Format	166
Table 357. DigOut0 ConLst Command Verb Format	167
Table 358. DigOut0 ConLst Command Response Format	167
Table 359. DigOut0 ConLstEntry0 Command Verb Format	167
Table 360. DigOut0 ConLstEntry0 Command Response Format	167
Table 361. DigOut0 ConLstEntry4 Command Verb Format	168
Table 362. DigOut0 ConLstEntry4 Command Response Format	168
Table 363. DigOut0 ConSelectCtrl Command Verb Format	168
Table 364. DigOut0 ConSelectCtrl Command Response Format	168
Table 365. DigOut0 PinWCntrl Command Verb Format	169
Table 366. DigOut0 PinWCntrl Command Response Format	169
Table 367. DigOut0 ConfigDefault Command Verb Format	169
Table 368. DigOut0 ConfigDefault Command Response Format	169
Table 369. DigIn WCap Command Verb Format	170
Table 370. DigIn WCap Command Response Format	170
Table 371. DigIn PinCap Command Verb Format	171
Table 372. DigIn PinCap Command Response Format	171
Table 373. DigIn PwrState Command Verb Format	172
Table 374. DigIn PwrState Command Response Format	172
Table 375. DigIn PinWCntrl Command Verb Format	172
Table 376. DigIn PinWCntrl Command Response Format	172
Table 377. DigIn UnsolResp Command Verb Format	173
Table 378. DigIn UnsolResp Command Response Format	173
Table 379. DigIn ChSense Command Verb Format	173
Table 380. DigIn ChSense Command Response Format	174
Table 381. DigIn EAPD Command Verb Format	174
Table 382. DigIn EAPD Command Response Format	174
Table 383. DigIn ConfigDefault Command Verb Format	175
Table 384. DigIn ConfigDefault Command Response Format	175

Table 385. InPort0Mux WCap Command Verb Format	175
Table 386. InPort0Mux WCap Command Response Format	176
Table 387. InPort0Mux ConLst Command Verb Format	176
Table 388. InPort0Mux ConLst Command Response Format	177
Table 389. InPort0Mux OutAmpCap Command Verb Format	177
Table 390. InPort0Mux OutAmpCap Command Response Format	177
Table 391. InPort0Mux OutAmpRight Command Verb Format	177
Table 392. InPort0Mux OutAmpRight Command Response Format	178
Table 393. InPort0Mux OutAmpLeft Command Verb Format	178
Table 394. InPort0Mux OutAmpLeft Command Response Format	178
Table 395. InPort0Mux ConSelectCtrl Command Verb Format	178
Table 396. InPort0Mux ConSelectCtrl Command Response Format	179
Table 397. InPort0Mux ConLstEntry0 Command Verb Format	179
Table 398. InPort0Mux ConLstEntry0 Command Response Format	179
Table 399. InPort0Mux ConLstEntry4 Command Verb Format	179
Table 400. InPort0Mux ConLstEntry4 Command Response Format	179
Table 401. InPort0Mux ConLstEntry8 Command Verb Format	180
Table 402. InPort0Mux ConLstEntry8 Command Response Format	180
Table 403. InPort1Mux WCap Command Verb Format	180
Table 404. InPort1Mux WCap Command Response Format	180
Table 405. InPort1Mux ConLst Command Verb Format	181
Table 406. InPort1Mux ConLst Command Response Format	181
Table 407. InPort1Mux OutAmpCap Command Verb Format	182
Table 408. InPort1Mux OutAmpCap Command Response Format	182
Table 409. InPort1Mux OutAmpRight Command Verb Format	182
Table 410. InPort1Mux OutAmpRight Command Response Format	183
Table 411. InPort1Mux OutAmpLeft Command Verb Format	183
Table 412. InPort1Mux OutAmpLeft Command Response Format	183
Table 413. InPort1Mux ConSelectCtrl Command Verb Format	183
Table 414. InPort1Mux ConSelectCtrl Command Response Format	184
Table 415. InPort1Mux ConLstEntry0 Command Verb Format	184
Table 416. InPort1Mux ConLstEntry0 Command Response Format	184
Table 417. InPort1Mux ConLstEntry4 Command Verb Format	184
Table 418. InPort1Mux ConLstEntry4 Command Response Format	184
Table 419. InPort1Mux ConLstEntry8 Command Verb Format	185
Table 420. InPort1Mux ConLstEntry8 Command Response Format	185
Table 421. InPort2Mux WCap Command Verb Format	185
Table 422. InPort2Mux WCap Command Response Format	185
Table 423. InPort2Mux ConLst Command Verb Format	186
Table 424. InPort2Mux ConLst Command Response Format	186
Table 425. InPort2Mux OutAmpCap Command Verb Format	187
Table 426. InPort2Mux OutAmpCap Command Response Format	187
Table 427. InPort2Mux OutAmpRight Command Verb Format	187
Table 428. InPort2Mux OutAmpRight Command Response Format	188
Table 429. InPort2Mux OutAmpLeft Command Verb Format	188
Table 430. InPort2Mux OutAmpLeft Command Response Format	188
Table 431. InPort2Mux ConSelectCtrl Command Verb Format	188
Table 432. InPort2Mux ConSelectCtrl Command Response Format	189
Table 433. InPort2Mux ConLstEntry0 Command Verb Format	189
Table 434. InPort2Mux ConLstEntry0 Command Response Format	189
Table 435. InPort2Mux ConLstEntry4 Command Verb Format	189
Table 436. InPort2Mux ConLstEntry4 Command Response Format	189
Table 437. InPort2Mux ConLstEntry8 Command Verb Format	190
Table 438. InPort2Mux ConLstEntry8 Command Response Format	190
Table 439. PCBEEP OutAmpLeft Command Verb Format	190

Table 440. PCBEEP OutAmpLeft Command Response Format	190
Table 441. PCBEEP WCap Command Verb Format	191
Table 442. PCBEEP WCap Command Response Format	191
Table 443. PCBEEP OutAmpCap Command Verb Format	191
Table 444. PCBEEP OutAmpCap Command Response Format	192
Table 445. PCBEEP Gen Command Verb Format	192
Table 446. PCBEEP Gen Command Response Format	193
Table 447. CD WCap Command Verb Format	193
Table 448. CD WCap Command Response Format	193
Table 449. CD PinCap Command Verb Format	194
Table 450. CD PinCap Command Response Format	194
Table 451. CD PinWCntrl Command Verb Format	195
Table 452. CD PinWCntrl Command Response Format	195
Table 453. CD ConfigDefault Command Verb Format	196
Table 454. CD ConfigDefault Command Response Format	196
Table 455. VolumeKnob WCap Command Verb Format	196
Table 456. VolumeKnob WCap Command Response Format	197
Table 457. VolumeKnob VolKnobCap Command Verb Format	197
Table 458. VolumeKnob VolKnobCap Command Response Format	197
Table 459. VolumeKnob ConLst Command Verb Format	197
Table 460. VolumeKnob ConLst Command Response Format	198
Table 461. VolumeKnob ConLstEntry0 Command Verb Format	198
Table 462. VolumeKnob ConLstEntry0 Command Response Format	198
Table 463. VolumeKnob ConLstEntry4 Command Verb Format	198
Table 464. VolumeKnob ConLstEntry4 Command Response Format	198
Table 465. VolumeKnob UnsolResp Command Verb Format	199
Table 466. VolumeKnob UnsolResp Command Response Format	199
Table 467. VolumeKnob Cntrl Command Verb Format	199
Table 468. VolumeKnob Cntrl Command Response Format	200
Table 469. VolumeKnob VCSR0 Command Verb Format	200
Table 470. VolumeKnob VCSR0 Command Response Format	200
Table 471. InPort0Vol WCap Command Verb Format	200
Table 472. InPort0Vol WCap Command Response Format	201
Table 473. InPort0Vol ConLst Command Verb Format	201
Table 474. InPort0Vol ConLst Command Response Format	202
Table 475. InPort0Vol InAmpRight Command Verb Format	202
Table 476. InPort0Vol InAmpRight Command Response Format	202
Table 477. InPort0Vol InAmpLeft Command Verb Format	202
Table 478. InPort0Vol InAmpLeft Command Response Format	202
Table 479. InPort0Vol ConLstEntry Command Verb Format	203
Table 480. InPort0Vol ConLstEntry Command Response Format	203
Table 481. InPort1Vol WCap Command Verb Format	203
Table 482. InPort1Vol WCap Command Response Format	203
Table 483. InPort1Vol ConLst Command Verb Format	204
Table 484. InPort1Vol ConLst Command Response Format	204
Table 485. InPort1Vol InAmpRight Command Verb Format	205
Table 486. InPort1Vol InAmpRight Command Response Format	205
Table 487. InPort1Vol InAmpLeft Command Verb Format	205
Table 488. InPort1Vol InAmpLeft Command Response Format	205
Table 489. InPort1Vol ConLstEntry Command Verb Format	205
Table 490. InPort1Vol ConLstEntry Command Response Format	206
Table 491. InPort2Vol WCap Command Verb Format	206
Table 492. InPort2Vol WCap Command Response Format	206
Table 493. InPort2Vol ConLst Command Verb Format	207
Table 494. InPort2Vol ConLst Command Response Format	207

Table 495. InPort2Vol InAmpRight Command Verb Format	207
Table 496. InPort2Vol InAmpRight Command Response Format	208
Table 497. InPort2Vol InAmpLeft Command Verb Format	208
Table 498. InPort2Vol InAmpLeft Command Response Format	208
Table 499. InPort2Vol ConLstEntry Command Verb Format	208
Table 500. InPort2Vol ConLstEntry Command Response Format	208
Table 501. ADC0Mux WCap Command Verb Format	209
Table 502. ADC0Mux WCap Command Response Format	209
Table 503. ADC0Mux ConLst Command Verb Format	210
Table 504. ADC0Mux ConLst Command Response Format	210
Table 505. ADC0Mux ConSelectCtrl Command Verb Format	210
Table 506. ADC0Mux ConSelectCtrl Command Response Format	210
Table 507. ADC0Mux ConLstEntry Command Verb Format	210
Table 508. ADC0Mux ConLstEntry Command Response Format	211
Table 509. ADC0Mux LR Command Verb Format	211
Table 510. ADC0Mux LR Command Response Format	211
Table 511. ADC0Mux OutAmpCap Command Verb Format	211
Table 512. ADC0Mux OutAmpCap Command Response Format	212
Table 513. ADC0Mux OutAmpRight Command Verb Format	212
Table 514. ADC0Mux OutAmpRight Command Response Format	212
Table 515. ADC0Mux OutAmpLeft Command Verb Format	212
Table 516. ADC0Mux OutAmpLeft Command Response Format	213
Table 517. ADC1Mux WCap Command Verb Format	213
Table 518. ADC1Mux WCap Command Response Format	213
Table 519. ADC1Mux ConLst Command Verb Format	214
Table 520. ADC1Mux ConLst Command Response Format	214
Table 521. ADC1Mux ConSelectCtrl Command Verb Format	214
Table 522. ADC1Mux ConSelectCtrl Command Response Format	215
Table 523. ADC1Mux ConLstEntry Command Verb Format	215
Table 524. ADC1Mux ConLstEntry Command Response Format	215
Table 525. ADC1Mux LR Command Verb Format	215
Table 526. ADC1Mux LR Command Response Format	216
Table 527. ADC1Mux OutAmpCap Command Verb Format	216
Table 528. ADC1Mux OutAmpCap Command Response Format	216
Table 529. ADC1Mux OutAmpRight Command Verb Format	216
Table 530. ADC1Mux OutAmpRight Command Response Format	217
Table 531. ADC1Mux OutAmpLeft Command Verb Format	217
Table 532. ADC1Mux OutAmpLeft Command Response Format	217
Table 533. ADC2Mux WCap Command Verb Format	217
Table 534. ADC2Mux WCap Command Response Format	218
Table 535. ADC2Mux ConLst Command Verb Format	218
Table 536. ADC2Mux ConLst Command Response Format	219
Table 537. ADC2Mux ConSelectCtrl Command Verb Format	219
Table 538. ADC2Mux ConSelectCtrl Command Response Format	219
Table 539. ADC2Mux ConLstEntry Command Verb Format	219
Table 540. ADC2Mux ConLstEntry Command Response Format	219
Table 541. ADC2Mux LR Command Verb Format	220
Table 542. ADC2Mux LR Command Response Format	220
Table 543. ADC2Mux OutAmpCap Command Verb Format	220
Table 544. ADC2Mux OutAmpCap Command Response Format	220
Table 545. ADC2Mux OutAmpRight Command Verb Format	221
Table 546. ADC2Mux OutAmpRight Command Response Format	221
Table 547. ADC2Mux OutAmpLeft Command Verb Format	221
Table 548. ADC2Mux OutAmpLeft Command Response Format	222
Table 549. STAC9227/9228/9229/9230 Options and Part Order Numbers	223

Table 550. Pin Table 225

1. DESCRIPTION

The STAC9227/9228/9228D are high fidelity, 8-channel audio CODECs compatible with the Intel High Definition (HD) Audio Interface. The STAC9227/9228/9228D CODECs provide high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9227/9228/9228D incorporate SigmaTel's proprietary technology to achieve a DAC SNR in excess of 100 dB. The higher performance and quality of SigmaTel's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9227/9228/9228D provide stereo 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9227/9228/9228D SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF OUT supports 88.2 KHz. Additional sample rates are supported by the driver software.

The STAC9227/9228/9228D support all desired eight channel configurations, including switchable Headphone Out, and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9227/9228/9228D has up to four General Purpose I/O (GPIO) pin. The STAC9227/9228/9228D also provide a single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9227/9228/9228D integrate a headphone amplifier which is available on Ports A, B and D. The headphone amplifier is dedicated to these three outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected to the CODEC, and to allow the CODECs to be reconfigured to support these devices regardless of which port they are plugged into the system. SPDIF input sensing is also supported. The fully parametric SigmaTel SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers. Note: The Jack Detect circuit and component selection are critical for accurate detection of audio jacks on individual ports. Please see the reference design for circuit implementation details.

The STAC9227/9228/9228D operate with a 3.3 V digital supply and a 3.3 V to 5 V analog supply.

The STAC9227/9228/9228D are available in a 48-pin LQFP Environmental (ROHS) package.

2. CHARACTERISTICS

2.1. Audio Fidelity

DAC SNR:	105dB	A-Weighted	5.0 V +/- 5%
ADC SNR:	90dB	A-Weighted	5.0 V +/- 5%

2.2. Electrical Specifications

2.2.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9227/9228/9228D. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0°C to +70°C
Storage temperature		-55 °C to +125 °C
Soldering temperature		260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 228.

2.2.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: With Supply Override Enable Bit set to force 5 V operation.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 4.5 V	4.275	4.5	4.725	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T _{case} (48-LQFP)			+90	°C

ESD: The STAC9227/9228/9228D is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9227/9228/9228D implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.3. STAC9227/9228/9228D 5V, 4.5V, 4.0V, and 3.3V Analog Performance Characteristics

($T_{\text{ambient}} = 25^{\circ}\text{C}$, $AV_{\text{dd}} = \text{Supply} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}} = DV_{\text{ss}} = 0\text{ V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 VRMS, 10 K Ω /50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0 dB settings on all gain stages)

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Digital to Analog Converters						
Resolution		All		24		Bits
SNR - DAC to All Line-Out Ports (Note 4)	Analog Mixer Disabled, PCM data	5 V 4.5 V 4.0 V 3.3 V		105 101 100 98		dB
THD+N - DAC to All Line-Out Ports (Note 3)	Analog Mixer Disabled, -3dB Signal, PCM data	5 V 4.5 V 4.0 V 3.3 V		90 88 86 84		dB
SNR - DAC to All Line-Out Ports (Note 4)	Analog Mixer Enabled, PCM data	5 V 4.5 V 4.0 V 3.3 V		90 88 87 85		dB
THD+N - DAC to All Line-Out Ports (Note 3)	Analog Mixer Enabled, -3dB Signal, PCM data	5 V 4.5 V 4.0 V 3.3 V		80 78 77 75		dB
Dynamic Range: DAC to All Line Out Ports (Note2)	-60dB signal level	5 V 4.5 V 4.0 V 3.3 V	-	95 93 92 90	-	dB
SNR - DAC to All Headphone Ports (Note 4)	Analog Mixer Disabled, 10 K Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		105 101 100 98		dB
THD+N - DAC to All Headphone Ports (Note 3)	Analog Mixer Disabled, -3dB Signal, 10 K Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		85 83 82 80		dB
SNR - DAC to All Headphone Ports with 2 Headphone Outputs Operating (Note 4)	Analog Mixer Disabled, 32 Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		100 98 97 95		dB
THD+N - DAC to All Headphone Ports with 2 Headphone Outputs Operating (Note 3)	Analog Mixer Disabled, -3dB Signal, 32 Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		82 80 79 77		dB
SNR - DAC to All Headphone Ports (Note 4)	Analog Mixer Disabled, 32 Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		100 98 97 95		dB

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
THD+N - DAC to All Headphone Ports (Note 3)	Analog Mixer Disabled, -3dB Signal, 32 Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		85 83 82 80		dB
SNR - DAC to All Headphone Ports (Note 4)	Analog Mixer Enabled, 10 K Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		90 88 87 85		dB
THD+N - DAC to All Headphone Ports (Note 3)	Analog Mixer Enabled, -3dB Signal, 10k Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		79 77 76 74		dB
SNR - DAC to All Headphone Ports (Note 4)	Analog Mixer Enabled, 32 Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		87 85 84 82		dB
THD+N - DAC to All Headphone Ports (Note 3)	Analog Mixer Enabled, -3dB Signal, 32 Ω load, PCM data	5 V 4.5 V 4.0 V 3.3 V		74 72 71 69		dB
Any Analog Input to DAC Crosstalk	10 KHz Signal Frequency	All	-	-85	-	dB
Any Analog Input to DAC Crosstalk	1 KHz Signal Frequency	All	-	-80	-	dB
Gain Error	Analog Mixer Disabled	All			0.5	dB
Interchannel Gain Mismatch	Analog Mixer Disabled	All			0.5	dB
D/A Digital Filter Pass Band (Note 5)		All	20	-	19,200	Hz
D/A Digital Filter Transition Band		All	19,200	-	28,800	Hz
D/A Digital Filter Stop Band		All	28,800	-	-	Hz
D/A Digital Filter Stop Band Rejcn (Note 6)		All	-100	-	-	dB
D/A Out-of-Band Rejection (Note 7)		All	-55	-	-	dB
Group Delay (48 KHz sample rate)		All	-	-	1	ms
Attenuation, Gain Step Size DIGITAL		All	-	0.75	-	dB
Gain Drift		All	-	100	-	ppm/ $^{\circ}$ C
DAC Offset Voltage		All	-	100	20	mV
Deviation from Linear Phase		All	-	1	10	degrees
Analog Outputs						

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Full Scale All Line-Outs	DAC PCM Data	5 V 4.5 V 4.0 V 3.3 V	1.00 1.00 1.00 0.70	-	-	Vrms
Full Scale All Line-Outs	DAC PCM Data	All	2.83	-	-	Vp-p
All Headphone Capable Outputs	32 Ω load	All	31	50	-	mW peak
Analog inputs						
Full Scale Input Voltage	0dB Boost @ 4.75 V	All	1.00	-	-	Vrms
All Analog Inputs with boost	10dB Boost	All	0.31	-	-	Vrms
All Analog Inputs with boost	20dB Boost	All	0.10	-	-	Vrms
All Analog Inputs with boost	30dB Boost	All	0.03	-	-	Vrms
All Analog Inputs with boost	40dB Boost	All	0.01	-	-	Vrms
Input Impedance		All	-	50	-	K Ω
Input Capacitance		All	-	15	-	pF
Analog Mixer						
SNR - CD to Ports A,B, & D Line-Out (Note 4)		All		90		dB
THD+N - CD to Ports A,B, & D Line-Out (Note 3)	-3dB Input	All		70		dB
SNR - All Line-In to A,B, & D Line-Out (Note 4)		All		90		dB
THD+N - All Line-In to A,B, & D Line-Out (Note 3)	-3dB Input	All		70		dB
SNR - Analog PC Beep to Ports A,B, & D Line-Out (Note 4)		All		85		dB
THD+N - Analog PC Beep to Ports A,B, & D Line-Out (Note 3)	-3dB Input	All		70		dB
Analog to Digital Converter						
Resolution		All		24		Bits
Dynamic Range, All Analog Inputs to A/D (Note 1)	High Pass Filer Enabled, 1 Vrms Input, No boost	All	88	90		dB
SNR All Analog Inputs to A/D (Note 4)	High Pass Filter enabled	All	88	90		dB
THD+N All Analog Inputs to A/D (Note 3)	High Pass Filter enabled, -3dBV input Level	All		85		dB
Analog Frequency Response (Note 2)		All	10	-	30,000	Hz
A/D Digital Filter Pass Band (Note 5)		All	20	-	19,200	Hz
A/D Digital Filter Transition Band		All	19,200	-	28,800	Hz

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
A/D Digital Filter Stop Band		All	28,800	-	-	Hz
A/D Digital Filter Stop Band Rejection (Note 6)		All	-100	-	-	dB
Group Delay (48 KHz sample rate)		All	-	-	1	ms
Any Analog Input to ADC Crosstalk	10 KHz Signal Frequency	All	-	-85	-	dB
Any Analog Input to ADC Crosstalk	1 KHz Signal Frequency	All	-	-80	-	dB
Spurious Tone Rejection		All	-	-100	-	dB
Attenuation, Gain Step Size ANALOG		All	-	1.5	-	dB
Interchannel Gain Mismatch ADC		All	-	-	0.5	dB
Noise Floor when 40dB Mic Boost Enabled		All			0.01	mV
40dB Mic Boost Enabled SNR	5 mV Input	All		60		dB
40dB Mic Boost Enabled THD+N	5 mV Input	All		55		dB
Power Supply						
Power Supply Rejection Ratio	1 KHz	All	-	-70	-	dB
Power Supply Rejection Ratio	20 KHz	All	-	-40	-	dB
D0 Didd	3.3 V			75	90	mA
D0 Aidd	5.0 V, 4.5 V, & 4.0 V, 3.3 V			85		mA
D1 Didd	3.3 V			75	90	mA
D1 Aidd	5.0 V, 4.5 V, & 4.0 V, 3.3 V			85		mA
D2 Didd	3.3 V			23	30	mA
D2 Aidd	5.0 V, 4.5 V, & 4.0 V, 3.3 V			58		mA
D3 Didd	3.3 V			23	30	mA
D3 Aidd	5.0 V, 4.5 V, & 4.0 V, 3.3 V			37		mA
One Stereo ADC Didd	3.3 V			8	10	mA
One Stereo ADC Aidd	5.0 V, 4.5 V, & 4.0 V, 3.3 V			10		mA
One Stereo DAC Didd	3.3 V			3	5	mA
One Stereo DAC Aidd	5.0 V, 4.5 V, & 4.0 V, 3.3 V			2		mA
CD Input						
CD Common Mode Rejection (CMR)		All	50	55		dB
Voltage Reference Outputs						
VREFout (Note 8)		All	-	0.5 X AVdd	-	V
VREFILT (VAG)		All		0.45 X AVdd		V
Phased Locked Loop						

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
PLL lock time		All		96	200	μsec
PLL (or Azalia Bit CLK) 24 MHz clock jitter		All		150	500	psec
Digital to Analog Converters						
Resolution		All		24		Bits
SNR - DAC to All Line-Out Ports (Note 4)	Analog Mixer Disabled, PCM data	5 V 4.5 V 4.0 V 3.3 V		105 101 100 98		dB
THD+N - DAC to All Line-Out Ports (Note 3)	Analog Mixer Disabled, -3dB Signal, PCM data	5 V 4.5 V 4.0 V 3.3 V		90 88 86 84		dB
SNR - DAC to All Line-Out Ports (Note 4)	Analog Mixer Enabled, PCM data	5 V 4.5 V 4.0 V 3.3 V		90 88 87 85		dB
THD+N - DAC to All Line-Out Ports (Note 3)	Analog Mixer Enabled, -3dB Signal, PCM data	5 V 4.5 V 4.0 V 3.3 V		80 78 77 75		dB
Dynamic Range: DAC to All Line Out Ports (Note2)	-60dB signal level	5 V 4.5 V 4.0 V 3.3 V	-	95 93 92 90	-	dB
SNR - DAC to All Headphone Ports (Note 4)	Analog Mixer Disabled, 10KΩ load, PCM data	5 V 4.5 V 4.0 V 3.3 V		105 101 100 98		dB

- Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
- ± 3dB limits for Line Output & 0 dB gain, at -20dBV
- Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
- Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
- Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
- Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
- The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
- Can be set to 0.5 or 0.8 AVdd.

3. DETAILED DESCRIPTION

3.1. Universal Jacks™

SigmaTel's Universal Jacks™ technology allows for the greatest flexibility in board design and implementation.

For the STAC9227/9228/9228D family the Universal Jacks™ capabilities are as follows¹:

- Ports A, B, and D support²:
 - Headphone Out
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40 dB Microphone boost³:
- Ports C, E, F, G, H support²:
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40 dB Microphone boost³:
 - Ports G & H do not have VrefOut Support

Note¹: On the STAC9227/9228/9228D family, only one function can be selected on each pin pair at a time. For example, a pin pair cannot be configured as an input and output at the same time. Configuration can be changed at any time.

Note²: Three Headphones should not be used simultaneously. Performance degradation will occur when using two Headphones simultaneously. See electrical specifications for details.

Note³: When the 40dB microphone boost feature is enabled, gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

3.1.1. Audio Jack Presence Detect

SENSE_A pin is used to detect the presence of plugs in ports A, B, C, and D. SENSE_B pin is used to detect the presence of plugs in ports E, F, G, and H. Refer to the reference design for port detect circuitry. Select the precision of the resistors used as follows:

AVDD Nominal Voltage (+/-5%)	Resistor Tolerance Sense A (If Port D is used)	Resistor Tolerance Sense A (If Port D is not used)	Resistor Tolerance Sense B (If Port H is used)	Resistor Tolerance Sense B (If Port H is not used)
5 V	1%	1%	1%	1%
4.5 V	1%	1%	1%	1%
4 V	0.50%	1%	0.50%	1%
3.3 V	0.10%	1%	0.10%	1%

3.2. Impedance Sense

Impedance Sense is accomplished by on-chip circuitry that measures the impedance at the pin of the chip and compares it to internal reference impedance. Below is a table that contains the bin information and codes returned when the pin widget impedance field in the Port Pin Sense widget is read. Please note that even under the best conditions, there is no method to guarantee 100% impedance sensing due to variations in external circuitry and impedance overlap of devices that can be plugged into a jack. The impedance sense table reflects both standard Line Out and Headphone output drivers. Please reference the HD Audio Universal Jack Application Note on the SigmaTel Extranet for more information.

Table 1: Impedance Sense

Bins	Return Hex Code	Impedance Level (Ohms)	General Device Detected
000b	0064h	Impedance < 300 Ω	Passive Speakers, Headset Speakers
001b	012Ch	Impedance = 300 Ω +/- 25%	Some Headset Speakers
010b	028Ah	300 Ω > Impedance < 1275 Ω	Some Microphones
011b	03E8h	Impedance = 1275 Ω +/- 25%	Microphones
100b	07D0h	1275 Ω > Impedance < 2000 Ω	Microphones
101b	0BB8h	Impedance = 2000 Ω +/- 25%	Amplified Speakers
110b	2710h	> 2000 Ω	Amplified Speakers, Line In
111b	2710h	> 2000 Ω	Amplified Speakers, Line In

3.3. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz and 96 KHz, and implements internal Jack Detect.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to accept consumer SPDIF voltage levels directly eliminates the need for costly external receiver ICs. Advanced features such as record slot select and SPDIF_IN routing to the DAC allows for simultaneous record and play.

3.4. SPDIF Output

SPDIF Output can operate at 44.1 KHz, 48 KHz, 88.2 KHz, and 96 KHz, as defined in the Intel High Definition Audio Specification, with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

3.5. Digital Microphone Support (STAC9228X/D)

The digital microphone interface permits connection of a digital microphone(s) to the STAC9228 via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that

carry individual channels of digital microphone data to the STAC927x family. In the event that a single microphone is used, the data is routed to both ADC channels.

The DMIC_CLK output is programmable from 1.176 MHz to 4.704 MHz in 1.176 MHz increments, and is synchronous to the 24 MHz internal clock. The default frequency is 2.352 MHz.

The STAC927x family supports the following digital microphone configurations:

Table 2. Valid Digital Microphone Configurations

Digital Mics	Date Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, 1, or 2	Available on either DMIC_0 or DMIC_1 Both ADC Channels produce data, may be in phase or out by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 OR Single Edge on DMIC_0 and 1	0, 1, or 2	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, 1, or 2	Requires both DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge	0, 1, or 2	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 3. DMIC_CLK, DMIC_0 and DMIC_1 Operation During Power States

Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D2	Yes	Clock Disabled	Input Disabled	DMIC_CLK Remains Low
D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK Remains Low
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

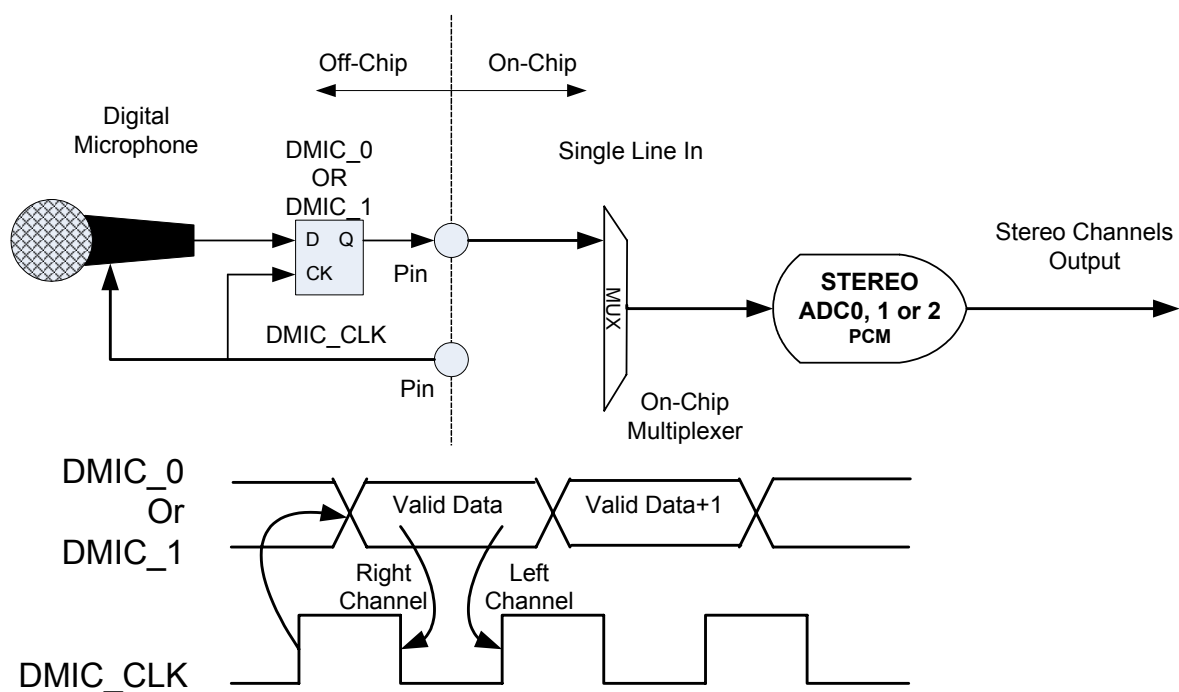


Figure 1. Single Digital Microphone (data is ported to both left and right channels)

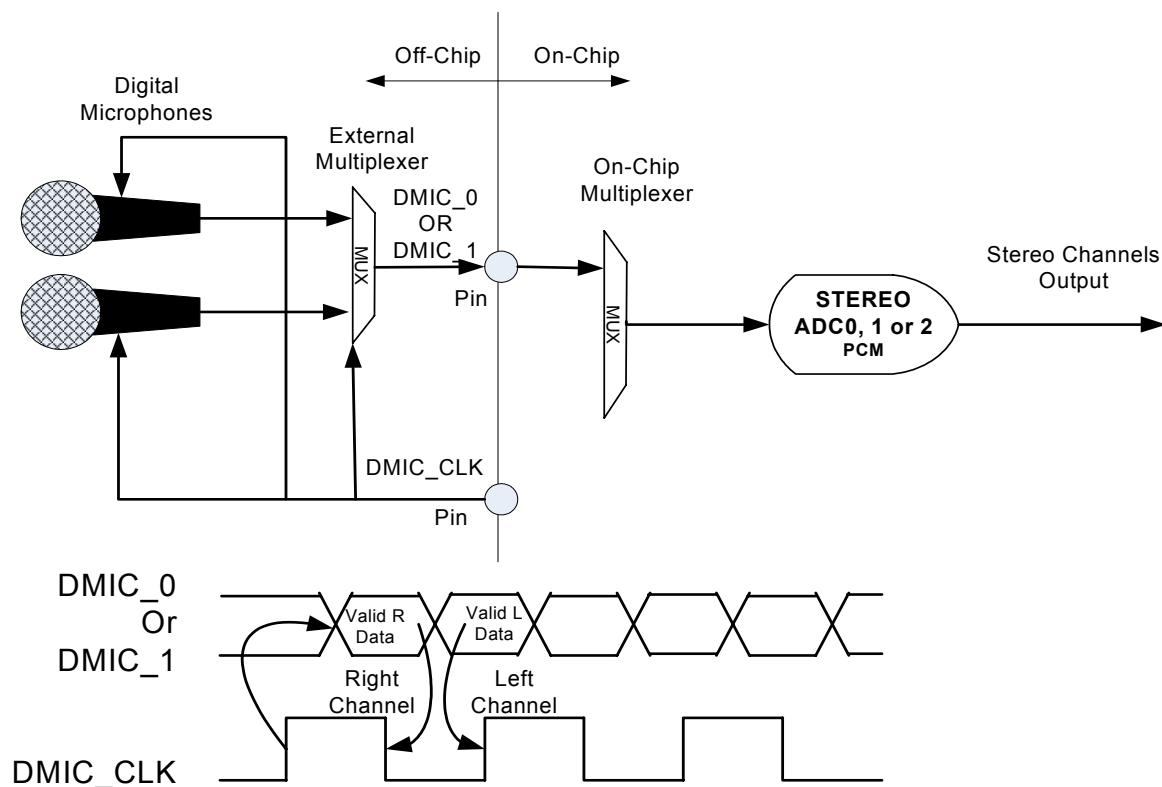


Figure 2. Stereo Digital Microphone Configuration

Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

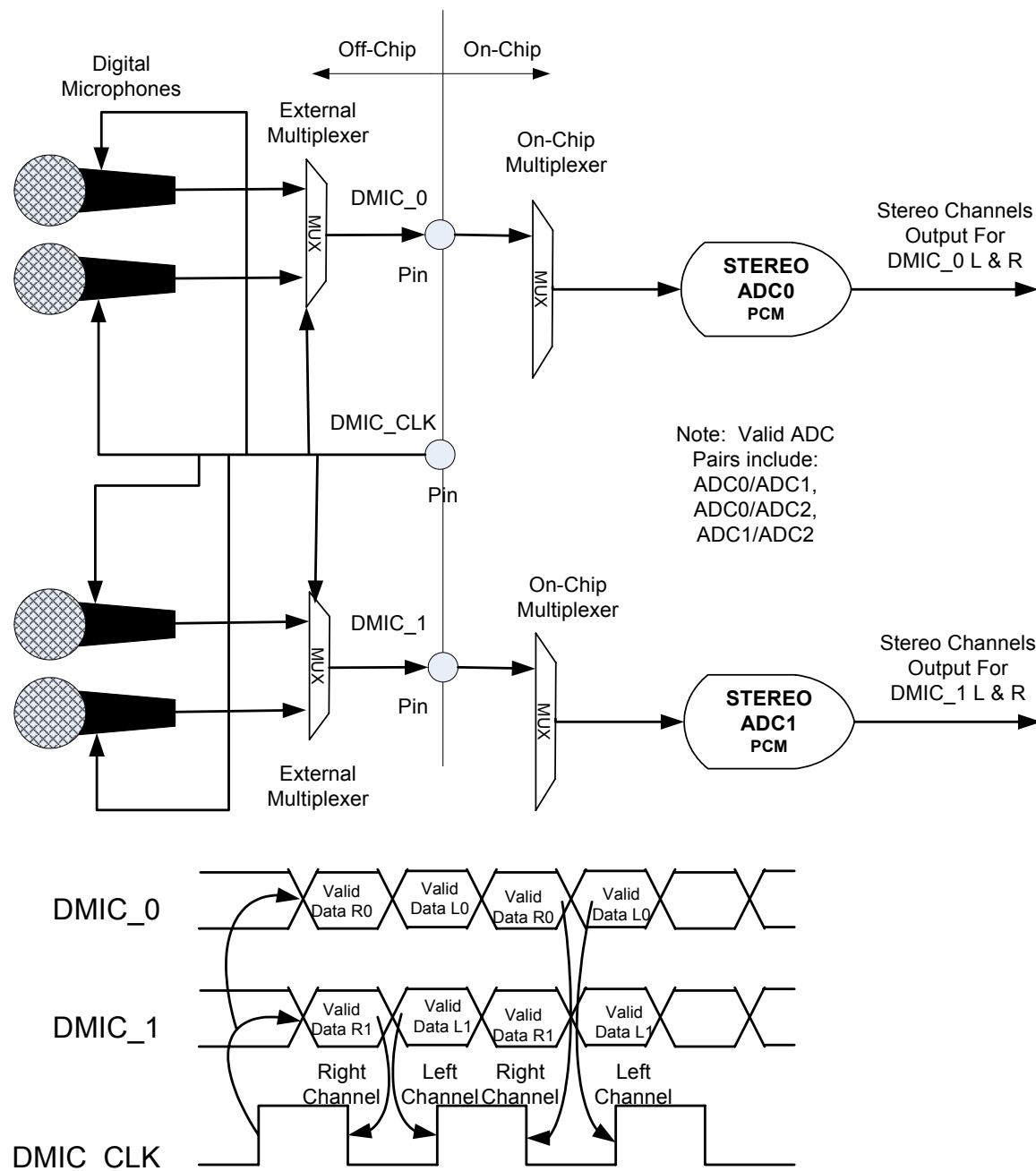


Figure 3. Quad Digital Microphone Configuration

Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

3.6. Analog PC-Beep

PC-Beep is NOT supported during Link Reset.

3.7. Headphone Drivers (Restrictions)

Three Headphones should not be used simultaneously. Performance degradation will occur when using two Headphones simultaneously. See electrical specifications for details.

3.8. Device IDs

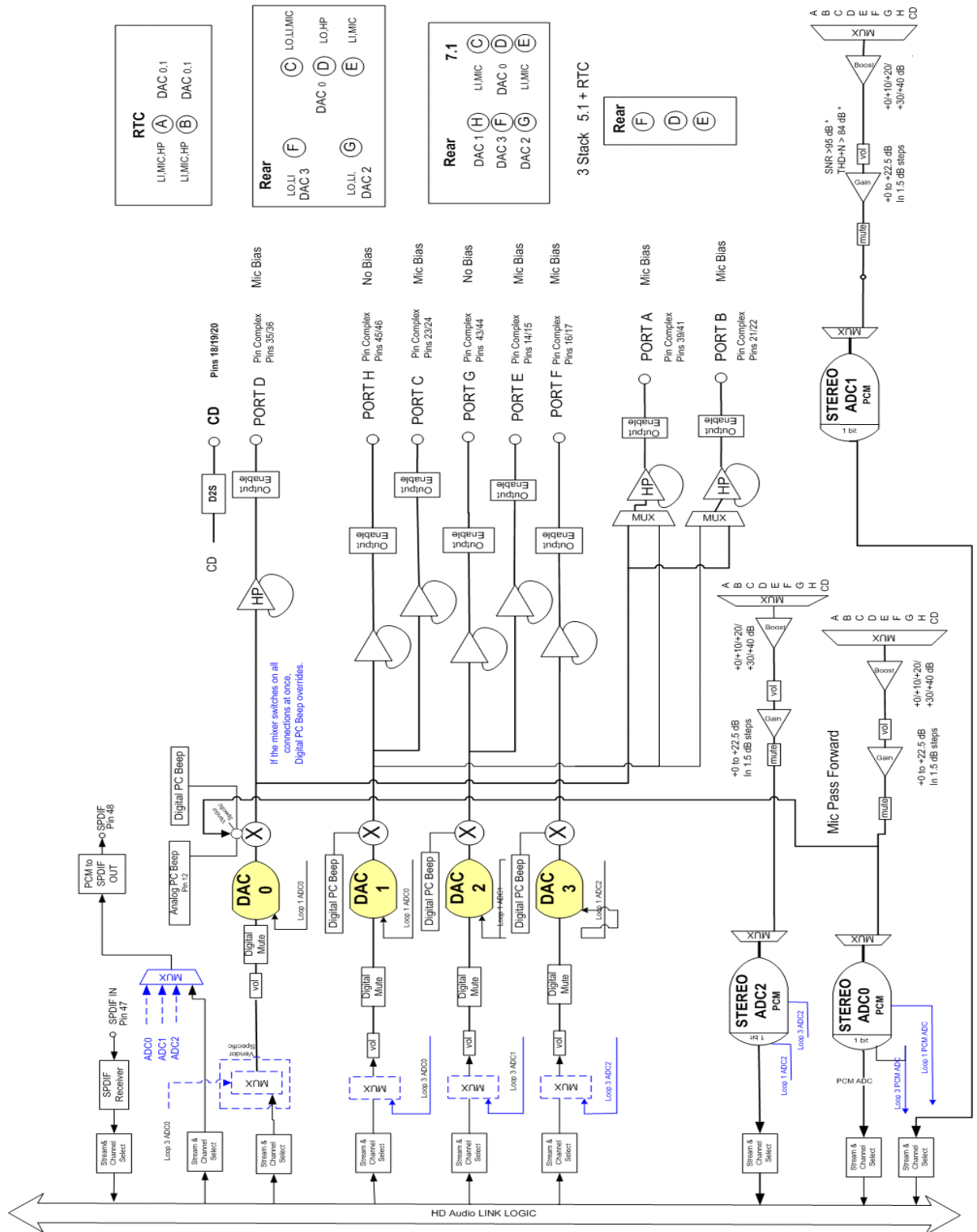
Table 4. Device IDs

Part Number	DAC SNR dB	VID	DID	Rev ID	Step ID	SSID*	Assm ID*	Dolby	Dig Mic	Volume or DMIC
STAC9228X	95	8384h	7616h	01h	01h	000001h	00h	No	Yes	Selectable
STAC9228D	95	8384h	7617h	01h	01h	000001h	00h	HT/SR	Yes	Selectable
STAC9227X	95	8384h	7618h	01h	01h	000001h	00h	No	No	Selectable

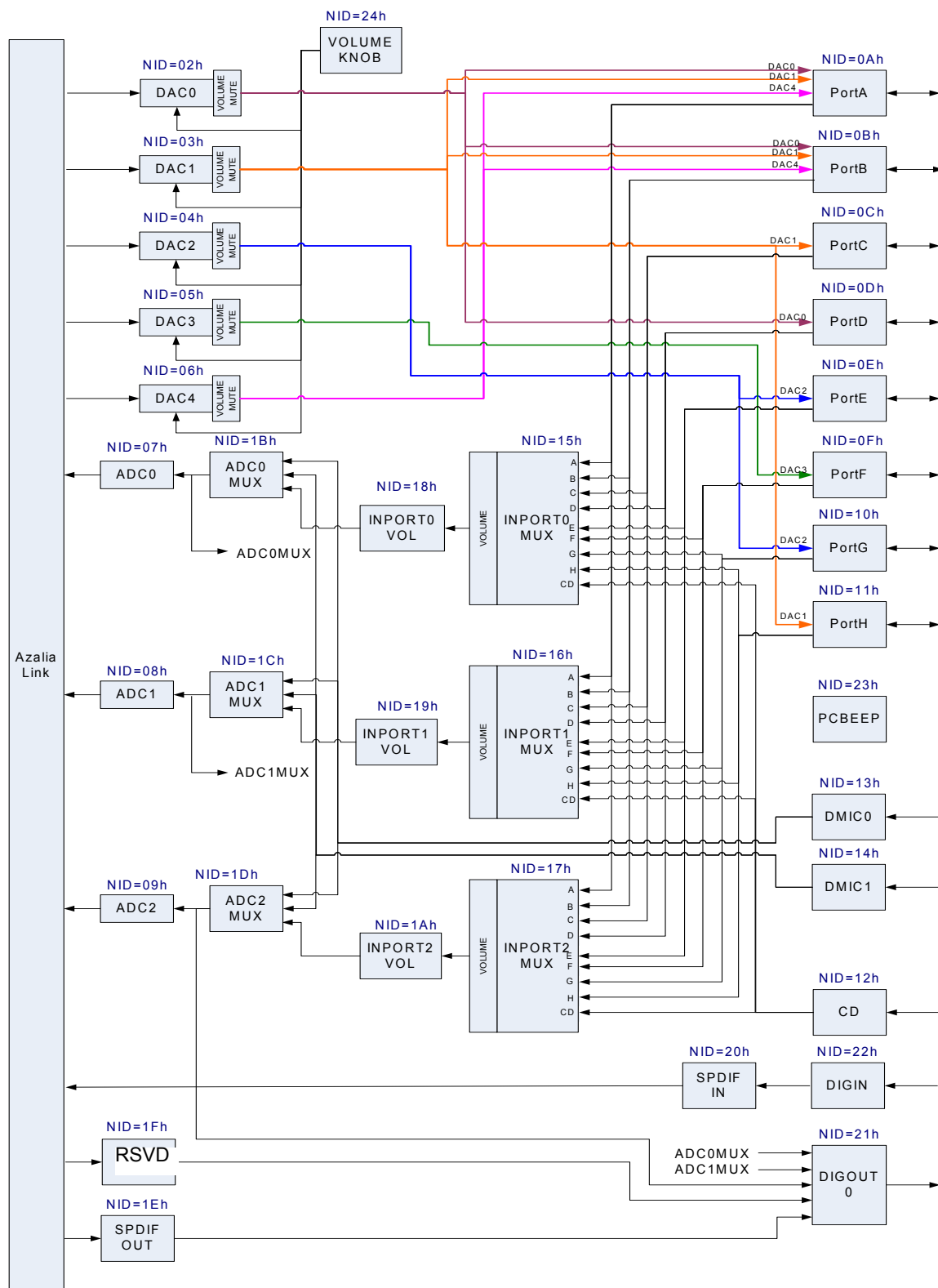
Note: SVIDs, SSIDs and Assembly IDs are read/writable by BIOS. All other ID fields are read-only.

Note: HT/SR refers to Home Theater/Sound Room

4. FUNCTIONAL BLOCK DIAGRAMS



5. WIDGET DIAGRAM



5.1. Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings.

Table 5. Pin Configuration Default Settings

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
DigInPin	Not Connected 01b	Mainboard Rear 1h	SPDIF In Ch	RCA 4h	Gray 2h	Jack Detect Override = 1	9h	0h
DigOutPin	Connect to Jack 00b	Mainboard Rear 1h	SPDIF Out 4h	RCA 4h	Gray 2h	Jack Detect Override = 0	7h	0h
PortAPin	Connect to Jack 00b	Mainboard Front 2h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override = 0	2h	0h
PortBPin	Connect to Jack 00b	Mainboard Front 2ht	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override = 0	8h	0h
PortCPin	Connect to Jack 00b	Mainboard Rear 1h	Line In 8h	1/8 inch Jack 1h	Blue 3h	Jack Detect Override = 0	4h	Eh
PortDPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Green 4h	Jack Detect Override = 0	1h	0h
PortEPin	Connect to Jack 00b	Mainboard Rear 1h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override = 0	4h	0h
PortFPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Black 1h	Jack Detect Override = 0	1h	2h
PortGPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Orange 6h	Jack Detect Override = 0	1h	1h
PortHPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Gray 2h	Jack Detect Override = 0	1h	Fh
CDPin	Not Connected 01b	Internal 01000b	CD 3h	ATAPI Internal 3h	Unknown 0h	Jack Detect Override = 1	Fh	0h
DigMicPin	Not Connected 01b	Internal 01000b	Mic In Ah	Unknown 0h	Unknown 0h	Jack Detect Override = 1	Fh	0h
DigMicPin	Not Connected 01b	Internal 01000b	Mic In Ah	Unknown 0h	Unknown 0h	Jack Detect Override = 1	Fh	0h

6. WIDGET INFORMATION FOR THE STAC9227/9228/9228D

Table 6. High Definition Audio Widget List

ID	Widget Name	Description
00h	Root	Root Node
01h	Audio Function Group	Audio Function Group
02h	DAC0	Stereo Output Converter to DAC
03h	DAC1	Stereo Output Converter to DAC
04h	DAC2	Stereo Output Converter to DAC
05h	DAC3	Stereo Output Converter to DAC
06h	DAC4	Stereo Output Converter to DAC
07h	ADC0	Stereo Input Converter to ADC
08h	ADC1	Stereo Input Converter to ADC
09h	ADC2	Stereo Input Converter to ADC
0Ah	Port A	Port A Pin Widget (Configurable as HP, Line In, Line Out, Mic)
0Bh	Port B	Port B Pin Widget (Configurable as HP, Line In, Line Out, Mic)
0Ch	Port C	Port C Pin Widget (Configurable as Line In, Line Out, Mic)
0Dh	Port D	Port D Pin Widget (Configurable as HP, Line In, Line Out, Mic)
0Eh	Port E	Port E Pin Widget (Configurable as Line In, Line Out, Mic)
0Fh	Port F	Port F Pin Widget (Configurable as Line In, Line Out, Mic)
10h	Port G	Port G Pin Widget (Configurable as Line In, Line Out, Mic)
11h	Port H	Port H Pin Widget (Configurable as Line In, Line Out, Mic)
12h	CD	CD Pin Widget
13h	DigMic0	Digital Microphone 0 Pin Widget
14h	DigMic1	Digital Microphone 1 Pin Widget
15h	InPort0Mux	ADC0 Input Port Mux
16h	InPort1Mux	ADC1 Input Port Mux
17h	InPort2Mux	ADC2 Input Port Mux
18h	InPort0Vol	ADC0 Input Port Volume
19h	InPort1Vol	ADC1 Input Port Volume
1Ah	InPort2Vol	ADC2 Input Port Volume
1Bh	ADC0Mux	ADC0 Mux
1Ch	ADC1Mux	ADC1 Mux
1Dh	ADC2Mux	ADC2 Mux
1Eh	SPDIF_OUT	Stereo Output for SPDIF_Out
1Fh	RSVD	Reserved
20h	SPDIF_IN	Stereo Input for SPDIF_In

Table 6. High Definition Audio Widget List

ID	Widget Name	Description
21h	DigOut	Digital Output Pin
22h	DigIn	Digital Microphone Input Pin
23h	PCBEEP	Digital PC Beep
24h	VolumeKnob	Master Volume Controls

6.1. Root Node (NID = 0x00)

6.1.1. Root ID

Table 7. Root ID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table.

Table 8. Root ID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID.
[15:8]	DeviceFix	R	0x76	Fixed portion of Device ID.
[7:0]	DeviceProg	R	0x10	Dependent of device- See device ID table in section 5.8.

6.1.2. Root RevID

Table 9. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table.

Table 10. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant Azalia spec.
[19:16]	Minor	R	0x0	Minor rev number of compliant Azalia spec.
[15:12]	VendorFix	R	0x0	Fixed portion of Vendor's rev number for this device.
[11:8]	VendorProg	R	0x1	Vendor's rev number for this device.

Table 10. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7:4]	SteppingFix	R	0x0	Fixed portion of vendor stepping number within the Vendor RevID.
[3:0]	SteppingProg	R	0x1	vendor stepping number within the Vendor RevID.

6.1.3. Root NodeInfo

Table 11. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table.

Table 12. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

6.2. AFG Node (NID = 0x01)

6.2.1. AFG Reset

Table 13. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table.
Set1	7FF	See bits [7:0] of bitfield table.	0000_0000h

Table 14. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

6.2.2. AFG NodeInfo

Table 15. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table.

Table 16. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x2	Starting node number for function group subordinate nodes.
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x23	Total number of nodes.

6.2.3. AFG Type

Table 17. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table.

Table 18. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:9]	Rsvd	R	0x0	Reserved
[8]	UnSol	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7:0]	NodeType	R	0x01	Node type = Audio Function Group

6.2.4. AFG Cap

Table 19. AFG Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table.

Table 20. AFG Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15:12]	Rsvd2	R	0x0	Reserved
[11:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the Azalia link.
[7:4]	Rsvd1	R	0x0	Reserved
[3:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the Azalia link and when it appears as an analog signal at the pin.

6.2.5. AFG PCMCap

Table 21. AFG PCMCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

Table 22. AFG PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) supported

6.2.6. AFG Stream

Table 23. AFG Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

Table 24. AFG Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x0	No support for non-PCM data.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.2.7. AFG InAmpCap

Table 25. AFG InAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table.

Table 26. AFG InAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x5	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x0E	Number of steps in the gain range = 15 (0dB to 22.5 dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.2.8. AFG SupPwrState**Table 27. AFG SupPwrState Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table.

Table 28. AFG SupPwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	D3Sup	R	0x1	Power State D3 is supported. Allows for lowest possible power consuming state under software control (and still properly respond to a subsequent Power State command).
[2]	D2Sup	R	0x1	Power State D2 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10ms.
[1]	D1Sup	R	0x1	Power State D1 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10ms, excepting analog pass-through circuits which must remain fully on.
[0]	D0Sup	R	0x1	Power State D0 is supported. Node power state is fully on.

6.2.9. AFG GPIOCnt**Table 29. AFG GPIOCnt Command Verb Format**

	Verb ID	Payload	Response
Get	F00	11	See bitfield table.

Table 30. AFG GPIOCnt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	GPIWake	R	0x1	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPIUnsol	R	0x1	Unsolicited Response capability. Assuming the Unsolicited Enable Mask controls are enabled, GPIO's configured as inputs can generate an Unsolicited Response on the link when there is a change in level on the pin.
[29:24]	Rsvd	R	0x0	Reserved
[23:16]	NumGPIs	R	0x00	Number of GPI pins supported by function
[15:8]	NumGPOs	R	0x00	Number of GPO pins supported by function
[7:0]	NumGPIOs	R	0x03 = 48pin	Number of GPIO pins supported by function

6.2.10. AFG OutAmpCap

Table 31. AFG OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 32. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x02	Size of each step in the gain range = 0.75dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x7F	Number of steps in the gain range = 128 (-96dB to +0dB)

Table 32. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x7F	0dB-step is programmed with this offset

6.2.11. AFG PwrState

Table 33. AFG PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 34. AFG PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x2	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x2	PS-Set: Current power setting of referenced node. 0: All Powered-On 1: D1 = > PR0, PR1 2: D2 = > PR0, PR1, PR2, PR6, EAPD 3: D3 = > PR6, PR5, PR3, PR2, PR1, PR0, EAPD Note: PR4 is not mapped in Azalia

6.2.12. AFG UnsolResp

Table 35. AFG UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 36. AFG Unsolicited Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x0	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.2.13. AFG GPIO

Table 37. AFG GPIO Command Verb Format

	Verb ID	Payload	Response
Get	F15	00	See bitfield table.
Set1	715	See bits [7:0] of bitfield table.	0000_0000h

Table 38. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Data4	RW	0x0	Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[3]	Data3	RW	0x0	Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[2]	Data2	RW	0x0	Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

Table 38. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Data1	RW	0x0	Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[0]	Data0	RW	0x0	Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

6.2.14. AFG GPIOEn

Table 39. AFG GPIOEn Command Verb Format

	Verb ID	Payload	Response
Get	F16	00	See bitfield table.
Set1	716	See bits [7:0] of bitfield table.	0000_0000h

Table 40. AFG GPIOEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Mask4	RW	0x0	Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[3]	Mask3	RW	0x0	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0x0	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

Table 40. AFG GPIOEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Mask1	RW	0x0	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0x0	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

6.2.15. AFG GPIODir

Table 41. AFG GPIODir Command Verb Format

	Verb ID	Payload	Response
Get	F17	00	See bitfield table.
Set1	717	See bits [7:0] of bitfield table.	0000_0000h

Table 42. AFG GPIODir Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Control4	RW	0x0	Direction control for GPIO4 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[3]	Control3	RW	0x0	Direction control for GPIO3 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[2]	Control2	RW	0x0	Direction control for GPIO2 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[1]	Control1	RW	0x0	Direction control for GPIO1 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[0]	Control0	RW	0x0	Direction control for GPIO0 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output

6.2.16. AFG GPIOWakeEn

Table 43. AFG GPIOWakeEn Command Verb Format

	Verb ID	Payload	Response
Get	F18	00	See bitfield table.
Set1	718	See bits [7:0] of bitfield table.	0000_0000h

Table 44. AFG GPIOWakeEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	W4	RW	0x0	Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[3]	W3	RW	0x0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[2]	W2	RW	0x0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[1]	W1	RW	0x0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[0]	W0	RW	0x0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = when Azalia link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.

6.2.17. AFG GPIOUnsol**Table 45. AFG GPIOUnsol Command Verb Format**

	Verb ID	Payload	Response
Get	F19	00	See bitfield table.
Set1	719	See bits [7:0] of bitfield table.	0000_0000h

Table 46. AFG GPIOUnsol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	EnMask4	RW	0x0	Unsolicited enable mask for GPIO4. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[3]	EnMask3	RW	0x0	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[2]	EnMask2	RW	0x0	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[1]	EnMask1	RW	0x0	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[0]	EnMask0	RW	0x0	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.

6.2.18. AFG GPIOSticky

Table 47. AFG GPIOSticky Command Verb Format

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table.
Set1	71A	See bits [7:0] of bitfield table.	0000_0000h

Table 48. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Mask4	RW	0x0	GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[3]	Mask3	RW	0x0	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[2]	Mask2	RW	0x0	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

Table 48. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Mask1	RW	0x0	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[0]	Mask0	RW	0x0	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

6.2.19. AFG SubID

Table 49. AFG SubID Command Verb Format

	Verb ID	Payload	Response
Get	F20	00	See bitfield table.
Set1	720	See bits [7:0] of bitfield table.	0000_0000h
Set2	721	See bits [7:0] of bitfield table.	0000_0000h
Set3	722	See bits [7:0] of bitfield table.	0000_0000h
Set4	723	See bits [7:0] of bitfield table.	0000_0000h

Table 50. AFG SubID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Subsys3	RW	0x00	Subsystem ID. (Any non-zero value)
[23:16]	Subsys2	RW	0x00	
[15:8]	Subsys1	RW	0x01	
[7:0]	Assembly	RW	0x00	Assembly ID. (Not applicable to CODEC vendors)

6.2.20. AFG TCKT

Table 51. AFG TCKT Command Verb Format

	Verb ID	Payload	Response
Get	FE5	00	See bitfield table.
Set1	7E5	See bits [7:0] of bitfield table.	0000_0000h

Table 52. AFG TCKT Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	AnaD3Enable	RW	0x0	D3 enable signal for analog
[6:0]	TCKT	RW	0x0	Test circuit (default reset on) TBD [6:0]

6.2.21. AFG Sply

Table 53. AFG Sply Command Verb Format

	Verb ID	Payload	Response
Get	FE6	00	See bitfield table.
Set1	7E6	See bits [7:0] of bitfield table.	0000_0000h

Table 54. AFG Sply Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd	R	0x0	Reserved
[6:5]	IBIAS	RW	0x0	00 = Normal Current; 01 = 80% nominal Analog Current; 10 = 120%nominal Analog Current; 11 = 140% nominal Analog Current

Table 54. AFG Sply Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	PinLvl	RW	0x1	0 = low-level SPDIF Input (special buffer for low level signals) 1 = standard SPDIF Input (for high level signals)
[3:0]	SplyOvr	RW	0x0	Supply Override Control. See Table below: [0] = invert ADC supply; [1] = invert DAC supply; [2] = supply value; [3] = supply override enable

6.2.22. AFG DACMode

Table 55. AFG DACMode Command Verb Format

	Verb ID	Payload	Response
Get	FEB	00	See bitfield table.
Set1	7EB	See bits [7:0] of bitfield table.	0000_0000h

Table 56. AFG DACMode Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	ADCMixDAC	RW	0x0	Enable mixing of ADC with DAC signal (for karaoke)
[5]	FadeFast	RW	0x0	Gain ramps at the maximum rate
[4]	FadeLog	RW	0x0	Gain ramping is dB linear instead of voltage linear over time
[3:0]	Rsvd	R	0x0	Reserved

6.2.23. AFG GPIOIrty

Table 57. AFG GPIOIrty Command Verb Format

	Verb ID	Payload	Response
Get	FEE	00	See bitfield table.
Set1	7EE	See bits [7:0] of bitfield table.	0000_0000h

Table 58. AFG GPIOIrty Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	GP4	RW	0x1	GPIO4 Polarity; If configured as an output: 0 = inverting, 1 = non-inverting; If configured as a non-sticky input: 0 = inverting, 1 = non-inverting; If configured as a sticky input: 0 = falling events will be detected, 1 = rising events will be detected.
[3]	GP3	RW	0x1	GPIO3 Polarity; If configured as an output: 0 = inverting, 1 = non-inverting; If configured as a non-sticky input: 0 = inverting, 1 = non-inverting; If configured as a sticky input: 0 = falling events will be detected, 1 = rising events will be detected.
[2]	GP2	RW	0x1	GPIO2 Polarity; If configured as an output: 0 = inverting, 1 = non-inverting; If configured as a non-sticky input: 0 = inverting, 1 = non-inverting; If configured as a sticky input: 0 = falling events will be detected, 1 = rising events will be detected.

Table 58. AFG GPIOIrty Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	GP1	RW	0x1	GPIO1 Polarity; If configured as an output: 0 = inverting, 1 = non-inverting; If configured as a non-sticky input: 0 = inverting, 1 = non-inverting; If configured as a sticky input: 0 = falling events will be detected, 1 = rising events will be detected.
[0]	GP0	RW	0x1	GPIO0 Polarity; If configured as an output: 0 = inverting, 1 = non-inverting; If configured as a non-sticky input: 0 = inverting, 1 = non-inverting; If configured as a sticky input: 0 = falling events will be detected, 1 = rising events will be detected.

6.2.24. AFG GPIODrive

Table 59. AFG GPIODrive Command Verb Format

	Verb ID	Payload	Response
Get	FEF	00	See bitfield table.
Set1	7EF	See bits [7:0] of bitfield table.	0000_0000h

Table 60. AFG GPIODrive Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	OD4	RW	0x0	GPIO4 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[3]	OD3	RW	0x0	GPIO3 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).

Table 60. AFG GPIODrive Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	OD2	RW	0x0	GPIO2 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[1]	OD1	RW	0x0	GPIO1 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[0]	OD0	RW	0x0	GPIO0 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).

6.2.25. AFG DMic

Table 61. AFG DMic Command Verb Format

	Verb ID	Payload	Response
Get	FF0	00	See bitfield table.
Set1	7F0	See bits [7:0] of bitfield table.	0000_0000h

Table 62. AFG DMic Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3:2]	PhAdj	RW	0x0	Selects what phase of the DigMic clock the data should be latched: 0 = rising edge 1 = center of high 2 = falling edge 3 = center of low
[1:0]	Rate	RW	0x2	Selects the DigMic rate: 0 = 4.704 MHz 1 = 3.528 MHz 2 = 2.352 MHz 3 = 1.176 MHz

6.3. DAC0 Node (NID = 0x02)

6.3.1. DAC0 Cnvtr

Table 63. DAC0 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 64. DAC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 64. DAC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.3.2. DAC0 OutAmpRight

Table 65. DAC0 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 66. DAC0 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.3.3. DAC0 OutAmpLeft

Table 67. DAC0 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 68. DAC0 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.3.4. DAC0 WCap

Table 69. DAC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 70. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 70. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvr	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.3.5. DAC0 PwrState

Table 71. DAC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 72. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.3.6. DAC0 CnvtrID

Table 73. DAC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 74. DAC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.3.7. DAC0 LR

Table 75. DAC0 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 76. DAC0 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.4. DAC1 Node (NID = 0x03)

6.4.1. DAC1 Cnvtr

Table 77. DAC1 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 78. DAC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 78. DAC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.4.2. DAC1 OutAmpRight

Table 79. DAC1 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 80. DAC1 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.4.3. DAC1 OutAmpLeft

Table 81. DAC1 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 82. DAC1 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.4.4. DAC1 WCap

Table 83. DAC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 84. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 84. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.4.5. DAC1 PwrState

Table 85. DAC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 86. DAC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.4.6. DAC1 CnvtrID

Table 87. DAC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 88. DAC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.4.7. DAC1 LR

Table 89. DAC1 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 90. DAC1 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.5. DAC2 Node (NID = 0x04)

6.5.1. DAC2 Cnvtr

Table 91. DAC2 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 92. DAC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 92. DAC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.5.2. DAC2 OutAmpRight

Table 93. DAC2 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 94. DAC2 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.5.3. DAC2 OutAmpLeft

Table 95. DAC2 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 96. DAC2 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.5.4. DAC2 WCap

Table 97. DAC2 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 98. DAC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 98. DAC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.5.5. DAC2 PwrState

Table 99. DAC2 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 100. DAC2 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.5.6. DAC2 CnvtrID

Table 101. DAC2 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 102. DAC2 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.5.7. DAC2 LR

Table 103. DAC2 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 104. DAC2 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.6. DAC3 Node (NID = 0x05)

6.6.1. DAC3 Cnvtr

Table 105. DAC3 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 106. DAC3 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 106. DAC3 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.6.2. DAC3 OutAmpRight

Table 107. DAC3 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 108. DAC3 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.6.3. DAC3 OutAmpLeft

Table 109. DAC3 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 110. DAC3 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.6.4. DAC3 WCap

Table 111. DAC3 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 112. DAC3 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 112. DAC3 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvr	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.6.5. DAC3 PwrState

Table 113. DAC3 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 114. DAC3 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.6.6. DAC3 CnvtrID**Table 115. DAC3 CnvtrID Command Verb Format**

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 116. DAC3 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.6.7. DAC3 LR**Table 117. DAC3 LR Command Verb Format**

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 118. DAC3 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.7. DAC4 Node (NID = 0x06)

6.7.1. DAC4 Cnvtr

Table 119. DAC4 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 120. DAC4 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 120. DAC4 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.7.2. DAC4 OutAmpRight

Table 121. DAC4 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 122. DAC4 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.7.3. DAC4 OutAmpLeft

Table 123. DAC4 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 124. DAC4 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.7.4. DAC4 WCap

Table 125. DAC4 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 126. DAC4 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	DAC4 Enabled = 0x0 DAC4 Disabled = 0xF	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping

Table 126. DAC4 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.7.5. DAC4 PwrState

Table 127. DAC4 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 128. DAC4 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.7.6. DAC4 CnvtrID**Table 129. DAC4 CnvtrID Command Verb Format**

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 130. DAC4 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.7.7. DAC4 LR**Table 131. DAC4 LR Command Verb Format**

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 132. DAC4 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.8. ADC0 Node (NID = 0x07)

6.8.1. ADC0 Cnvtr

Table 133. ADC0 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 134. ADC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 134. ADC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.8.2. ADC0 WCap

Table 135. ADC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 136. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.

Table 136. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.8.3. ADC0 ConLst

Table 137. ADC0 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 138. ADC0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.8.4. ADC0 ConLstEntry

Table 139. ADC0 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 140. ADC0 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x1B	ADC0Mux widget

6.8.5. ADC0 ProcState

Table 141. ADC0 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.
Set1	703	See bits [7:0] of bitfield table.	0000_0000h

Table 142. ADC0 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.8.6. ADC0 PwrState

Table 143. ADC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 144. ADC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.8.7.

Table 145. ADC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 146. ADC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.9. ADC1 Node (NID = 0x08)

6.9.1. ADC1 Cnvtr

Table 147. ADC1 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 148. ADC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 148. ADC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.9.2. ADC1 WCap

Table 149. ADC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 150. ADC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.

Table 150. ADC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.9.3. ADC1 ConLst

Table 151. ADC1 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 152. ADC1 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.9.4. ADC1 ConLstEntry

Table 153. ADC1 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 154. ADC1 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x1C	ADC1Mux widget

6.9.5. ADC1 ProcState

Table 155. ADC1 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.
Set1	703	See bits [7:0] of bitfield table.	0000_0000h

Table 156. ADC1 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.9.6. ADC1 PwrState

Table 157. ADC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 158. ADC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.9.7. ADC1 CnvtrID

Table 159. ADC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 160. ADC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.10. ADC2 Node (NID = 0x09)

6.10.1. ADC2 Cnvtr

Table 161. ADC2 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 162. ADC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 162. ADC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.10.2. ADC2 WCap

Table 163. ADC2 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 164. ADC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response

Table 164. ADC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.10.3. ADC2 ConLst

Table 165. ADC2 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 166. ADC2 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.10.4. ADC2 ConLstEntry

Table 167. ADC2 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 168. ADC2 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x1D	ADC2Mux widget

6.10.5. ADC2 ProcState

Table 169. ADC2 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.
Set1	703	See bits [7:0] of bitfield table.	0000_0000h

Table 170. ADC2 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.10.6. ADC2 PwrState

Table 171. ADC2 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 172. ADC2 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.10.7. ADC2 CnvtrID

Table 173. ADC2 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 174. ADC2 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.11. SPDIFOut Node (NID = 0x1E)

6.11.1. SPDIFOut Cnvtr

Table 175. SPDIFOut Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 176. SPDIFOut Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	FrmtNonPCM	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 176. SPDIFOut Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.11.2. SPDIFOut WCap

Table 177. SPDIFOut WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 178. SPDIFOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter

Table 178. SPDIFOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.11.3. SPDIFOut PCM

Table 179. SPDIFOut PCM Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

Table 180. SPDIFOut PCM Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported

Table 180. SPDIFOut PCM Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

6.11.4. SPDIFOut Stream

Table 181. SPDIFOut Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

Table 182. SPDIFOut Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.11.5. SPDIFOut CnvtrID**Table 183. SPDIFOut CnvtrID Command Verb Format**

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 184. SPDIFOut CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.11.6. SPDIFOut DigCnvtr**Table 185. SPDIFOut DigCnvtr Command Verb Format**

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.
Set1	70D	See bits [7:0] of bitfield table.	0000_0000h
Set2	70E	See bits [7:0] of bitfield table.	0000_0000h

Table 186. SPDIFOut DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	Rsvd1	R	0x0	Reserved
[14:8]	CC	RW	0x00	CC[6:0] - Category Code
[7]	L	RW	0x0	L - Generation Level
[6]	PRO	RW	0x0	PRO - Professional

Table 186. SPDIFOut DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	AUDIO	RW	0x0	/AUDIO - Non-Audio
[4]	COPY	RW	0x0	COPY - Copyright
[3]	PRE	RW	0x0	PRE - Preemphasis
[2]	VCFG	RW	0x0	VCFG - Validity Config
[1]	V	RW	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

6.12. SPDIFIn Node (NID = 0x20)

6.12.1. SPDIFIn Cnvtr

Table 187. SPDIFIn Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 188. SPDIFIn Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	FrmtNonPCM	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz

Table 188. SPDIFIn Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.12.2. SPDIFIn WCap

Table 189. SPDIFIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 190. SPDIFIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1 = Enabled 0xF = Disabled	Widget type = Audio Input
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	Unsolicited Response is not supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.12.3. SPDIFIn PCMCap

Table 191. SPDIFIn PCMCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

Table 192. SPDIFIn PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x0	192.0 KHz rate (4/1*48 KHz) NOT supported
[9]	R10	R	0x0	176.4 KHz rate (4/1*44.1 KHz) NOT supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x0	88.2 KHz rate (2/1*44.1 KHz) NOT supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

6.12.4. SPDIFIn Stream

Table 193. SPDIFIn Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

Table 194. SPDIFIn Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.12.5. SPDIFIn ConLst

Table 195. SPDIFIn ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 196. SPDIFIn ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.12.6. SPDIFIn ConLstEntry

Table 197. SPDIFIn ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 198. SPDIFIn ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 198. SPDIFIn ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x22	DigIn pin widget

6.12.7. SPDIFIn CnvtrID

Table 199. SPDIFIn CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 200. SPDIFIn CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.12.8. SPDIFIn DigCnvtr

Table 201. SPDIFIn DigCnvtr Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.
Set1	70D	See bits [7:0] of bitfield table.	0000_0000h
Set2	70E	See bits [7:0] of bitfield table.	0000_0000h

Table 202. SPDIFIn DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:15]	Rsvd2	R	0x0	Reserved
[14:8]	CC	R	0x00	CC[6:0] - Category Code
[7]	L	R	0x0	L - Generation Level
[6]	PRO	R	0x0	PRO - Professional
[5]	AUDIO	R	0x0	/AUDIO - Non-Audio
[4]	COPY	R	0x0	COPY - Copyright
[3]	PRE	R	0x0	PRE - Preemphasis
[2]	Rsvd1	R	0x0	Reserved (VCFG bit applies only to output streams)
[1]	V	R	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

6.12.9. SPDIFIn VCSR0

Table 203. SPDIFIn VCSR0 Command Verb Format

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.
Set1	7E0	See bits [7:0] of bitfield table.	0000_0000h

Table 204. SPDIFIn VCSR0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	RcvSmplRate	R	0x0	Recovered sample rate base 0 = 48 KHz 1 = 44.1 KHz
[30:28]	RcvRateMult	R	0x0	Recovered sample rate multiplier 000 = 1X 001 = 2X, all others reserved
[27:26]	Rsvd	R	0x0	Reserved

Table 204. SPDIFin VCSR0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[25:22]	OrigFS	R	0x0	Original sample rate (IEC spec).
[21:20]	CA	R	0x0	Clock accuracy 00 = Level II 01 = Level I 10 = Level III 11 = Reserved
[19:16]	FS	R	0x0	Sample Rate 0000 = 44.1 KHz 0010 = 48 KHz 0011 = 32 KHz All other combinations are reserved and shall not be used until further defined (IEC spec).
[15:12]	CN	R	0x0	Channel Number (audio channel) 0000 = do not take into account 0001 = A (left channel for stereo channel format) 0010 = B (right channel for stereo channel format) 0011 = C 1111 = O
[11:9]	SmplWrdL	R	0x0	Sample Word Length [2:0] If MaxWrdL = 1: 000 = unspecified 001 = 20 bits 010 = 22 bits 011 = reserved 100 = 23 bits 101 = 24 bits 110 = 21 bits 111 = reserved If MaxWrdL = 0: 000 = unspecified 001 = 16 bits 010 = 18 bits 011 = reserved 100 = 19 bits 101 = 20 bits 110 = 17 bits 111 = reserved
[8]	MaxWrdL	R	0x0	Max Word Length 0 = maximum audio sample word length is 20 bits 1 = maximum audio sample word length is 24 bits
[7]	NOBLKCH	RW	0x0	0 = normal behavior 1 = disable block size checking for spdif_in.

Table 204. SPDIFIn VCSR0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	VI	RW	0x0	0 = Respond to SPDIF_IN Valid tag 1 = Ignore SPDIF_IN valid tag
[5]	AMuteDis	RW	0x0	0 = Auto mute when SPDIF stream marked non PCM 1 = Auto Mute disabled.
[4:3]	SPL	RW	0x0	SPDIF_IN Parity Limit: Loss of DPLL Lock after: 00 = 4 parity errors 01 = 3 parity errors 10 = 2 parity errors 11 = 1 parity errors NEW LOCATION -- was at Register 72h, Page 0, D13:12, moved as part of SPDIF In consolidation
[2]	SPRun	R	0x0	SPDIF IN Running 0 = no signal on pin 47 1 = signal on pin 47 NEW LOCATION -- was at Register 72h, Page 0, D2, moved as part of SPDIF In consolidation
[1]	SIPER	RW	0x0	SPDIF_IN PARITY ERROR. Set to clear. 'Overlaps SIPERSTAT'. Overlaps SIPERSTAT.
[0]	COPYINV	RW	0x0	Copyright invert bit.

6.13. PortA Node (NID = 0x0A)

6.13.1. PortA WCap

Table 205. PortA WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 206. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget

Table 206. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.13.2. PortA PinCap

Table 207. PortA PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 208. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin

Table 208. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.13.3. PortA ConLst

Table 209. PortA ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 210. PortA ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03 = Enabled 0x02 = Disabled	Number of NID entries in connection list.

6.13.4. PortA ConLstEntry**Table 211. PortA ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 212. PortA ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x06 = Enabled 0x00 = Disabled	DAC4 Converter widget
[15:8]	ConL1	R	0x03	DAC1 Converter widget
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.13.5. PortA ConSelectCtrl**Table 213. PortA ConSelectCtrl Command Verb Format**

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 214. PortA ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.13.6. PortA PinWCntrl**Table 215. PortA PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 216. PortA PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.13.7. PortA Unsolicited Response

Table 217. PortA Unsolicited Response Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 218. PortA Unsolicited Response Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.13.8. PortA ChSense**Table 219. PortA ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 220. PortA ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.13.9. PortA ConfigDefault**Table 221. PortA ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 222. PortA ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x02	Port Connectivity = Jack; Location = Mainboard front.
[23:16]	Config3	RW	0x21	Default Device = HP Out; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x40	Color = Green; Misc = No jack detect override.
[7:0]	Config1	RW	0x20	Association = 2h; Sequence = 0h.

6.14. PortB Node (NID = 0x0B)

6.14.1. PortB WCap

Table 223. PortB WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 224. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported

Table 224. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.14.2. PortB PinCap

Table 225. PortB PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 226. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.

Table 226. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphDrvCap	R	0x1	Pin has a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.14.3. PortB ConLst

Table 227. PortB ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 228. PortB ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03 = Enabled DAC4 0x02 = Disabled DAC4	Number of NID entries in connection list.

6.14.4. PortB ConLstEntry

Table 229. PortB ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 230. PortB ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x06 = Enabled 0x00 = Disabled	DAC4 Converter widget
[15:8]	ConL1	R	0x03	DAC1 Converter widget
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.14.5. PortB ConSelectCtrl

Table 231. PortB ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 232. PortB ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.14.6. PortB PinWCntrl

Table 233. PortB PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 234. PortB PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.14.7. PortB Unsolicited Response

Table 235. PortB Unsolicited Response Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 236. PortB Unsolicited Response Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.14.8. PortB ChSense**Table 237. PortB ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 238. PortB ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.14.9. PortB ConfigDefault**Table 239. PortB ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 240. PortB ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x02	Port Connectivity = Jack; Location = Mainboard front.
[23:16]	Config3	RW	0xA1	Default Device = Mic In; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x90	Color = Pink; Misc = No jack detect override.
[7:0]	Config1	RW	0x80	Association = 8h; Sequence = 0h.

6.15. PortC Node (NID = 0x0C)

6.15.1. PortC WCap

Table 241. PortC WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 242. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported

Table 242. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.15.2. PortC PinCap

Table 243. PortC PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 244. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.

Table 244. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.15.3. PortC ConLst

Table 245. PortC ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 246. PortC ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.15.4. PortC ConLstEntry

Table 247. PortC ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 248. PortC ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 248. PortC ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x03	DAC1 Converter widget

6.15.5. PortC PinWCntrl

Table 249. PortC PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 250. PortC PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.15.6. PortC UnsolResp

Table 251. PortC UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 252. PortC Unsolicited Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.15.7. PortC ChSense**Table 253. PortC ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 254. PortC ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.15.8. PortC ConfigDefault**Table 255. PortC ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 256. PortC ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0x81	Default Device = Line In; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x30	Color = Blue; Misc = No jack detect override.
[7:0]	Config1	RW	0x4E	Association = 4h; Sequence = Eh.

6.16. PortD Node (NID = 0x0D)**6.16.1. PortD WCap****Table 257. PortD WCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 258. PortD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.16.2. PortD PinCap

Table 259. PortD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 260. PortD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.16.3. PortD ConLst

Table 261. PortD ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 262. PortD ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.16.4. PortD ConLstEntry**Table 263. PortD ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 264. PortD ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.16.5. PortD PinWCntrl**Table 265. PortD PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 266. PortD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled

Table 266. PortD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.16.6. PortD UnsolResp

Table 267. PortD UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 268. PortD UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.16.7. PortD ChSense

Table 269. PortD ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

Table 269. PortD ChSense Command Verb Format

	Verb ID	Payload	Response
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 270. PortD ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.16.8. PortD ConfigDefault

Table 271. PortD ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 272. PortD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0x01	Default Device = Line Out; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x40	Color = Green; Misc = No jack detect override.
[7:0]	Config1	RW	0x10	Association = 1h; Sequence = 0h.

6.17. PortE Node (NID = 0x0E)

6.17.1. PortE WCap

Table 273. PortE WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 274. PortE WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported

Table 274. PortE WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.17.2. PortE PinCap

Table 275. PortE PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 276. PortE PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.

Table 276. PortE PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.17.3. PortE ConLst

Table 277. PortE ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 278. PortE ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.17.4. PortE ConLstEntry

Table 279. PortE ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 280. PortE ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 280. PortE ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x04	DAC2 Converter widget

6.17.5. PortE PinWCntrl

Table 281. PortE PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 282. PortE PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.17.6. PortE UnsolResp

Table 283. PortE UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 284. PortE Unsolicited Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.17.7. PortE ChSense**Table 285. PortE ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 286. PortE ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.17.8. PortE ConfigDefault**Table 287. PortE ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 288. PortE ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0xA1	Default Device = Mic In; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x90	Color = Pink; Misc = No jack detect override.
[7:0]	Config1	RW	0x40	Association = 4h; Sequence = 0h.

6.18. PortF Node (NID = 0x0F)**6.18.1. PortF WCap****Table 289. PortF WCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 290. PortF WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.18.2. PortF PinCap

Table 291. PortF PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 292. PortF PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.18.3. PortF ConLst

Table 293. PortF ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 294. PortF ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved

Table 294. PortF ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.18.4. PortF ConLstEntry

Table 295. PortF ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 296. PortF ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x05	DAC3 Converter widget

6.18.5. PortF PinWCntrl

Table 297. PortF PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 298. PortF PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled

Table 298. PortF PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.18.6. PortF UnsolResp

Table 299. PortF UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 300. PortF UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.18.7. PortF ChSense**Table 301. PortF ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 302. PortF ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.18.8. PortF ConfigDefault**Table 303. PortF ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 304. PortF ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0x01	Default Device = Line Out; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x10	Color = Black; Misc = No jack detect override.
[7:0]	Config1	RW	0x12	Association = 1h; Sequence = 2h.

6.19. PortG Node (NID = 0x10)

6.19.1. PortG WCap

Table 305. PortG WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 306. PortG WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported

Table 306. PortG WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.19.2. PortG PinCap

Table 307. PortG PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 308. PortG PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.

Table 308. PortG PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.19.3. PortG ConLst

Table 309. PortG ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 310. PortG ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.19.4. PortG ConLstEntry

Table 311. PortG ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 312. PortG ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 312. PortG ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x04	DAC2 Converter widget

6.19.5. PortG PinWCntrl

Table 313. PortG PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 314. PortG PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	R	0x0	Vref Out not supported on this Port

6.19.6. PortG UnsolResp

Table 315. PortG UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 316. PortG Unsolicited Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.19.7. PortG ChSense**Table 317. PortG ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 318. PortG ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.19.8. PortG ConfigDefault**Table 319. PortG ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 320. PortG ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0x01	Default Device = Line Out; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x60	Color = Orange; Misc = No jack detect override.
[7:0]	Config1	RW	0x11	Association = 1h; Sequence = 1h.

6.20. PortH Node (NID = 0x11)**6.20.1. PortH WCap****Table 321. PortH WCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 322. Porth WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.20.2. Porth PinCap

Table 323. Porth PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 324. PortH PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.20.3. PortH ConLst

Table 325. PortH ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 326. PortH ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.20.4. PortH ConLstEntry**Table 327. PortH ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 328. PortH ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x03	DAC1 Converter widget

6.20.5. PortH PinWCntrl**Table 329. PortH PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 330. PortH PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	R	0x0	Vref Out not supported on this Port

6.20.6. PortH UnsolicitedResponse**Table 331. PortH UnsolicitedResponse Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 332. PortH UnsolicitedResponse Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.20.7. PortH ChSense**Table 333. PortH ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 334. PortH ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1's indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

6.20.8. PortH ConfigDefault

Table 335. PortH ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 336. PortH ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0x01	Default Device = Line Out; Connection Type = 1/8 inch jack.
[15:8]	Config2	RW	0x20	Color = Grey; Misc = No jack detect override.
[7:0]	Config1	RW	0x14	Association = 1h; Sequence = 4h.

6.21. DMic0 Node (NID = 0x13)

6.21.1. DMic0 WCap

Table 337. DMic0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 338. DMic0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4 = Enabled 0xF = Disabled	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream (since the digital microphone input is a SDM signal that needs to be processed by the digital filters, it is not a true bit for bit digital stream like I2S or SPDIF where samples are passed through unchanged)
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp

Table 338. DMic0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.21.2. DMic0 PinCap

Table 339. DMic0 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 340. DMic0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.21.3. DMic0 PinWCntrl**Table 341. DMic0 PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 342. DMic0 PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.21.4. DMic0 ConfigDefault**Table 343. DMic0 ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 344. DMic0 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x50	Port Connectivity = No connection; Location = Internal.
[23:16]	Config3	RW	0xA0	Default Device = Mic In; Connection Type = Unknown.

Table 344. DMic0 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x01	Color = Unknown; Misc = Jack detect override.
[7:0]	Config1	RW	0xF0	Association = Fh; Sequence = 0h.

6.22. DMic1 Node (NID = 0x14)

6.22.1. DMic1 WCap

Table 345. DMic1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 346. DMic1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4 = Enabled 0xF = Disabled	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream (since the digital microphone input is a SDM signal that needs to be processed by the digital filters, it is not a true bit for bit digital stream like I2S or SPDIF where samples are passed through unchanged)
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter

Table 346. DMic1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParamOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.22.2. DMic1 PinCap

Table 347. DMic1 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 348. DMic1 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VRefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HPhnDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.

Table 348. DMic1 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.22.3. DMic1 PinWCntrl

Table 349. DMic1 PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 350. DMic1 PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.22.4. DMic1 ConfigDefault

Table 351. DMic1 ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 352. DMic1 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x50	Port Connectivity = No connection; Location = Internal.
[23:16]	Config3	RW	0xA0	Default Device = Mic In; Connection Type = Unknown.
[15:8]	Config2	RW	0x01	Color = Unknown; Misc = Jack detect override.
[7:0]	Config1	RW	0xF0	Association = Fh; Sequence = 0h.

6.23. DigOut0 Node (NID = 0x21)

6.23.1. DigOut0 WCap

Table 353. DigOut0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 354. DigOut0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No support for swapping left and right channels
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response

Table 354. DigOut0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.23.2. DigOut0 PinCap

Table 355. DigOut0 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 356. DigOut0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.

Table 356. DigOut0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.23.3. DigOut0 ConLst

Table 357. DigOut0 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 358. DigOut0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x05	Number of NID entries in connection list.

6.23.4. DigOut0 ConLstEntry0

Table 359. DigOut0 ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 360. DigOut0 ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x1C	ADC1Mux widget
[23:16]	ConL2	R	0x1B	ADC0Mux widget

Table 360. DigOut0 ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x1F	Reserved Out Converter widget
[7:0]	ConL0	R	0x1E	SPDIF Out Converter widget

6.23.5. DigOut0 ConLstEntry4

Table 361. DigOut0 ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 362. DigOut0 ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL7	R	0x00	No connection
[23:16]	ConL6	R	0x00	No connection
[15:8]	ConL5	R	0x00	No connection
[7:0]	ConL4	R	0x1D	ADC2Mux widget

6.23.6. DigOut0 ConSelectCtrl

Table 363. DigOut0 ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 364. DigOut0 ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:1]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x0	Connection select control index.

6.23.7. DigOut0 PinWCntrl**Table 365. DigOut0 PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 366. DigOut0 PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5:0]	Rsvd1	R	0x0	Reserved

6.23.8. DigOut0 ConfigDefault**Table 367. DigOut0 ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 368. DigOut0 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Port Connectivity = Jack; Location = Mainboard rear.
[23:16]	Config3	RW	0x44	Default Device = SPDIF Out; Connection Type = RCA.

Table 368. DigOut0 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x21	Color = Grey; Misc = Jack detect override.
[7:0]	Config1	RW	0x70	Association = 7h; Sequence = 0h.

6.24. DigIn Node (NID = 0x22)

6.24.1. DigIn WCap

Table 369. DigIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 370. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4 = Enabled 0x8 = Disabled	Widget type = Pin Complex
[19:16]	Delay	R	0x3	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x1	Power State control capability for support of EAPD
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 370. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.24.2. DigIn PinCap

Table 371. DigIn PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 372. DigIn PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x1	This widget controls EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on input pins.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable. (EAPD! = output stream)
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.24.3. DigIn PwrState**Table 373. DigIn PwrState Command Verb Format**

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 374. DigIn PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - EAPD powered down (Hi-Z). 11 - Powered down (default)

6.24.4. DigIn PinWCntrl**Table 375. DigIn PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 376. DigIn PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.24.5. DigIn UnsolicitedResponse**Table 377. DigIn UnsolicitedResponse Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 378. DigIn UnsolicitedResponse Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon lock or loss-of-lock of SPDIF-in clock recovery circuit.
[6]	Rsvd1	R	0x0	Reserved.
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.24.6. DigIn ChSense**Table 379. DigIn ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h

Table 380. DigIn ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex. For this widget, Presence Detect indicates that the SPDIF-in clock recovery circuit has locked onto a valid SPDIF-in sampling frequency. Any change in status will generate an Unsolicited Response, if enabled with verb 708.
[30:0]	Rsvd	R	0x0	Reserved. Impedance sense not supported for this Pin Complex.

6.24.7. DigIn EAPD

Table 381. DigIn EAPD Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 382. DigIn EAPD Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd2	R	0x0	Reserved
[1]	Data	RW	0x0	EAPD value reflected on the EAPD pin. 0 = power down external amp; 1 = power up external amp If PwrState < 0x2. If PwrState > = 0x2, Pin47 is Hi-Z. An external pull-down is required if EAPD must be low when Pin Widget is powered down.
[0]	Rsvd1	R	0x0	Reserved

6.24.8. DigIn ConfigDefault

Table 383. DigIn ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 384. DigIn ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x81	Port Connectivity = No connect; Location = Mainboard rear.
[23:16]	Config3	RW	0xC4	Default Device = SPDIF In; Connection Type = RCA.
[15:8]	Config2	RW	0x20	Color = Grey; Misc = No jack detect override.
[7:0]	Config1	RW	0x90	Association = 9h; Sequence = 0h.

6.25. InPort0Mux Node (NID = 0x15)

6.25.1. InPort0Mux WCap

Table 385. InPort0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 386. InPort0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.25.2. InPort0Mux ConLst

Table 387. InPort0Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 388. InPort0Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x09	Number of NID entries in connection list.

6.25.3. InPort0Mux OutAmpCap

Table 389. InPort0Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 390. InPort0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.25.4. InPort0Mux OutAmpRight

Table 391. InPort0Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 392. InPort0Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.25.5. InPort0Mux OutAmpLeft

Table 393. InPort0Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 394. InPort0Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.25.6. InPort0Mux ConSelectCtrl

Table 395. InPort0Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 396. InPort0Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

6.25.7. InPort0Mux ConLstEntry0

Table 397. InPort0Mux ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 398. InPort0Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x12	CD In
[7:0]	ConL0	R	0x0E	Port E (default)

6.25.8. InPort0Mux ConLstEntry4

Table 399. InPort0Mux ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 400. InPort0Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL7	R	0x10	Port G
[23:16]	ConL6	R	0x0A	Port A

Table 400. InPort0Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL5	R	0x0D	Port D
[7:0]	ConL4	R	0x0C	Port C

6.25.9. InPort0Mux ConLstEntry8

Table 401. InPort0Mux ConLstEntry8 Command Verb Format

	Verb ID	Payload	Response
Get	F02	08	See bitfield table.

Table 402. InPort0Mux ConLstEntry8 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL11	R	0x0	No connection.
[23:16]	ConL10	R	0x0	No connection.
[15:8]	ConL9	R	0x0	No connection.
[7:0]	ConL8	R	0x11	Port H

6.26. InPort1Mux Node (NID = 0x16)

6.26.1. InPort1Mux WCap

Table 403. InPort1Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 404. InPort1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget

Table 404. InPort1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.26.2. InPort1Mux ConLst

Table 405. InPort1Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 406. InPort1Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved

Table 406. InPort1Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x09	Number of NID entries in connection list.

6.26.3. InPort1Mux OutAmpCap

Table 407. InPort1Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 408. InPort1Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.26.4. InPort1Mux OutAmpRight

Table 409. InPort1Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 410. InPort1Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.26.5. InPort1Mux OutAmpLeft

Table 411. InPort1Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 412. InPort1Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.26.6. InPort1Mux ConSelectCtrl

Table 413. InPort1Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 414. InPort1Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

6.26.7. InPort1Mux ConLstEntry0

Table 415. InPort1Mux ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 416. InPort1Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x12	CD In
[7:0]	ConL0	R	0x0E	Port E (default)

6.26.8. InPort1Mux ConLstEntry4

Table 417. InPort1Mux ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 418. InPort1Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL7	R	0x10	Port G
[23:16]	ConL6	R	0x0A	Port A

Table 418. InPort1Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL5	R	0x0D	Port D
[7:0]	ConL4	R	0x0C	Port C

6.26.9. InPort1Mux ConLstEntry8

Table 419. InPort1Mux ConLstEntry8 Command Verb Format

	Verb ID	Payload	Response
Get	F02	08	See bitfield table.

Table 420. InPort1Mux ConLstEntry8 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL11	R	0x0	No connection.
[23:16]	ConL10	R	0x0	No connection.
[15:8]	ConL9	R	0x0	No connection.
[7:0]	ConL8	R	0x11	Port H

6.27. InPort2Mux Node (NID = 0x17)

6.27.1. InPort2Mux WCap

Table 421. InPort2Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 422. InPort2Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget

Table 422. InPort2Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.27.2. InPort2Mux ConLst

Table 423. InPort2Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 424. InPort2Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved

Table 424. InPort2Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x9	Number of NID entries in connection list.

6.27.3. InPort2Mux OutAmpCap

Table 425. InPort2Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 426. InPort2Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.27.4. InPort2Mux OutAmpRight

Table 427. InPort2Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 428. InPort2Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.27.5. InPort2Mux OutAmpLeft

Table 429. InPort2Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 430. InPort2Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.27.6. InPort2Mux ConSelectCtrl

Table 431. InPort2Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 432. InPort2Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

6.27.7. InPort2Mux ConLstEntry0

Table 433. InPort2Mux ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 434. InPort2Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x12	CD In
[7:0]	ConL0	R	0x0E	Port E (default)

6.27.8. InPort2Mux ConLstEntry4

Table 435. InPort2Mux ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 436. InPort2Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL7	R	0x10	Port G
[23:16]	ConL6	R	0x0A	Port A

Table 436. InPort2Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL5	R	0x0D	Port D
[7:0]	ConL4	R	0x0C	Port C

6.27.9. InPort2Mux ConLstEntry8

Table 437. InPort2Mux ConLstEntry8 Command Verb Format

	Verb ID	Payload	Response
Get	F02	08	See bitfield table.

Table 438. InPort2Mux ConLstEntry8 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL11	R	0x0	No connection.
[23:16]	ConL10	R	0x0	No connection.
[15:8]	ConL9	R	0x0	No connection.
[7:0]	ConL8	R	0x11	Port H

6.28. PCBEEP Node (NID = 0x23)

6.28.1. PCBEEP OutAmpLeft

Table 439. PCBEEP OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 440. PCBEEP OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x0	1 = disable Digital PC Beep

Table 440. PCBEEP OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	Gain	RW	0x0	Mono (left) amplifier gain step number

6.28.2. PCBEEP WCap

Table 441. PCBEEP WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 442. PCBEEP WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x7	Widget type = Beep Generator
[19:4]	Rsvd1	R	0x0	Reserved
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	N/A
[0]	Stereo	R	0x0	Mono widget

6.28.3. PCBEEP OutAmpCap

Table 443. PCBEEP OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 444. PCBEEP OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x17	Size of each step in the gain range = 6 dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x03	Number of steps in the gain range = 4 (-18dB to 0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x03	0dB-step is programmed with this offset

6.28.4. PCBEEP Gen

Table 445. PCBEEP Gen Command Verb Format

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table.
Set1	70A	See bits [7:0] of bitfield table.	0000_0000h

Table 446. PCBEEP Gen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:0]	Divider	RW	0x0	Enable internal PC-Beep generation. Divider is 00h - disables internal PC Beep generation and enables normal operation of the CODEC. Divider is not 00h - generates the beep tone on all Pin Complexes that are currently configured as outputs. The Azalia spec states that the beep tone frequency = (48 KHz Azalia SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 KHz (logarithmic scale). Instead, this part generates tones with frequency = $48000 * (257 - \text{Divider}) / 1024$, yielding a linear range from 12 KHz to 93.75 Hz in steps of 46.875 Hz. If JackSenseVSR[Rate2x], then the beep tones generated have frequency = $48000 * (513 - \text{Divider}) / 1024$, yielding a range of 24 KHz to 12093.75 Hz in steps of 46.875 Hz.

6.29. CD Node (NID = 0x12)

6.29.1. CD WCap

Table 447. CD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 448. CD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget

Table 448. CD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amp
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.29.2. CD PinCap

Table 449. CD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 450. CD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved

Table 450. CD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.29.3. CD PinWCntrl

Table 451. CD PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 452. CD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.29.4. CD ConfigDefault

Table 453. CD ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 454. CD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x50	Port Connectivity = No connect; Location = Internal.
[23:16]	Config3	RW	0x33	Default Device = CD; Connection Type = ATAPI internal.
[15:8]	Config2	RW	0x01	Color = Unknown; Misc = Jack detect override.
[7:0]	Config1	RW	0xF0	Association = Fh; Sequence = 0h.

6.30. Reserved Node (NID = 0x1F)

6.31. VolumeKnob Node (NID = 0x24)

6.31.1. VolumeKnob WCap

Table 455. VolumeKnob WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 456. VolumeKnob WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x6 = Enabled 0xF = Disabled	Widget type = Volume Knob Widget
[19:0]	Rsvd1	R	0x0	Reserved. Software assumes capability of unsolicited responses and a connection list for this widget type.

6.31.2. VolumeKnob VolKnobCap

Table 457. VolumeKnob VolKnobCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	13	See bitfield table.

Table 458. VolumeKnob VolKnobCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Delta	R	0x1	Indicates if software can write a base volume to the Volume Control Knob.
[6:0]	NumSteps	R	0x7F	Total number of steps in the range of the volume knob = 128

6.31.3. VolumeKnob ConLst

Table 459. VolumeKnob ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 460. VolumeKnob ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	DAC4 enable = 0x05 DAC4 disable = 0x04	Number of NID entries in connection list.

6.31.4. VolumeKnob ConLstEntry0

Table 461. VolumeKnob ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 462. VolumeKnob ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x05	DAC3
[23:16]	ConL2	R	0x04	DAC2
[15:8]	ConL1	R	0x03	DAC1
[7:0]	ConL0	R	0x02	DAC0

6.31.5. VolumeKnob ConLstEntry4

Table 463. VolumeKnob ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 464. VolumeKnob ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL7	R	0x0	No connection.
[23:16]	ConL6	R	0x0	No connection.

Table 464. VolumeKnob ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL5	R	0x0	No connection.
[7:0]	ConL4	R	0x06 = Enabled 0x00 = Disabled	DAC4

6.31.6. VolumeKnob UnsolicitedResp

Table 465. VolumeKnob UnsolicitedResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 466. VolumeKnob UnsolicitedResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.31.7. VolumeKnob Cntrl

Table 467. VolumeKnob Cntrl Command Verb Format

	Verb ID	Payload	Response
Get	F0F	00	See bitfield table.
Set1	70F	See bits [7:0] of bitfield table.	0000_0000h

Table 468. VolumeKnob Cntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Direct	RW	0x0	Direct = 1 causes the volume control to directly control the hardware volume of the slave amps. Direct = 0 causes unsolicited responses to be generated.
[6:0]	Volume	RW	0x7F	Volume, specified in steps of amplifier gain

6.31.8. VolumeKnob VCSR0

Table 469. VolumeKnob VCSR0 Command Verb Format

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.
Set1	7E0	See bits [7:0] of bitfield table.	0000_0000h

Table 470. VolumeKnob VCSR0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Continuous	RW	0x1	Allow continuous incrementing/ decrementing of the volume knob value.
[2:0]	Rate	RW	0x0	Volume knob update rate, for continuous mode and de-bouncing (2.5 Hz to 20 Hz, in increments of 2.5 Hz)

6.32. InPort0Vol Node (NID = 0x18)

6.32.1. InPort0Vol WCap

Table 471. InPort0Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 472. InPort0Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x1	Input amp is present
[0]	Stereo	R	0x1	Stereo widget

6.32.2. InPort0Vol ConLst

Table 473. InPort0Vol ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 474. InPort0Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.32.3. InPort0Vol InAmpRight

Table 475. InPort0Vol InAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.
Set1	350	See bits [7:0] of bitfield table.	0000_0000h

Table 476. InPort0Vol InAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.32.4. InPort0Vol InAmpLeft

Table 477. InPort0Vol InAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.
Set1	360	See bits [7:0] of bitfield table.	0000_0000h

Table 478. InPort0Vol InAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.32.5. InPort0Vol ConLstEntry

Table 479. InPort0Vol ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 480. InPort0Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x15	InPort0 Mux widget

6.33. InPort1Vol Node (NID = 0x19)

6.33.1. InPort1Vol WCap

Table 481. InPort1Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 482. InPort1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 482. InPort1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x1	Input amp is present
[0]	Stereo	R	0x1	Stereo widget

6.33.2. InPort1Vol ConLst

Table 483. InPort1Vol ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 484. InPort1Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.33.3. InPort1Vol InAmpRight**Table 485. InPort1Vol InAmpRight Command Verb Format**

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.
Set1	350	See bits [7:0] of bitfield table.	0000_0000h

Table 486. InPort1Vol InAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.33.4. InPort1Vol InAmpLeft**Table 487. InPort1Vol InAmpLeft Command Verb Format**

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.
Set1	360	See bits [7:0] of bitfield table.	0000_0000h

Table 488. InPort1Vol InAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.33.5. InPort1Vol ConLstEntry**Table 489. InPort1Vol ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 490. InPort1Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x16	InPort1Mux widget

6.34. InPort2Vol Node (NID = 0x1A)

6.34.1. InPort2Vol WCap

Table 491. InPort2Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 492. InPort2Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping

Table 492. InPort2Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amp
[1]	InAmpPrsnt	R	0x1	Input amp is present
[0]	Stereo	R	0x1	Stereo widget

6.34.2. InPort2Vol ConLst

Table 493. InPort2Vol ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 494. InPort2Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.34.3. InPort2Vol InAmpRight

Table 495. InPort2Vol InAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.
Set1	350	See bits [7:0] of bitfield table.	0000_0000h

Table 496. InPort2Vol InAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.34.4. InPort2Vol InAmpLeft

Table 497. InPort2Vol InAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.
Set1	360	See bits [7:0] of bitfield table.	0000_0000h

Table 498. InPort2Vol InAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.34.5. InPort2Vol ConLstEntry

Table 499. InPort2Vol ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 500. InPort2Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x17	InPort2Mux widget

6.35. ADC0Mux Node (NID = 0x1B)

6.35.1. ADC0Mux WCap

Table 501. ADC0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 502. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.35.2. ADC0Mux ConLst**Table 503. ADC0Mux ConLst Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 504. ADC0Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03 = Enabled 0x01 = Disabled	Number of NID entries in connection list.

6.35.3. ADC0Mux ConSelectCtrl**Table 505. ADC0Mux ConSelectCtrl Command Verb Format**

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 506. ADC0Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.35.4. ADC0Mux ConLstEntry**Table 507. ADC0Mux ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 508. ADC0Mux ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection
[23:16]	ConL2	R	0x14 = Enabled 0x00 = Disabled	DMic1 pin widget
[15:8]	ConL1	R	0x13 = Enabled 0x00 = Disabled	DMic0 pin widget
[7:0]	ConL0	R	0x18	InPort0Vol widget

6.35.5. ADC0Mux LR

Table 509. ADC0Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 510. ADC0Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = swap left and right channels of this Widget.
[1:0]	Rsvd1	R	0x0	Reserved

6.35.6. ADC0Mux OutAmpCap

Table 511. ADC0Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 512. ADC0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x00	Size of each step in the gain range, N/A since there are no steps
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x00	No steps, gain is fixed at 0dB
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.35.7. ADC0Mux OutAmpRight

Table 513. ADC0Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 514. ADC0Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

6.35.8. ADC0Mux OutAmpLeft

Table 515. ADC0Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 516. ADC0Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

6.36. ADC1Mux Node (NID = 0x1C)

6.36.1. ADC1Mux WCap

Table 517. ADC1Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 518. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping

Table 518. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.36.2. ADC1Mux ConLst

Table 519. ADC1Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 520. ADC1Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03 = Enabled 0x1 = Disabled	Number of NID entries in connection list.

6.36.3. ADC1Mux ConSelectCtrl

Table 521. ADC1Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 522. ADC1Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.36.4. ADC1Mux ConLstEntry

Table 523. ADC1Mux ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 524. ADC1Mux ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection
[23:16]	ConL2	R	0x14 = Enabled 0x0 = Disabled	DMic1 pin widget
[15:8]	ConL1	R	0x13 = Enabled 0x0 = Disabled	DMic0 pin widget
[7:0]	ConL0	R	0x19	InPort1Vol widget

6.36.5. ADC1Mux LR

Table 525. ADC1Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 526. ADC1Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = swap left and right channels of this Widget.
[1:0]	Rsvd1	R	0x0	Reserved

6.36.6. ADC1Mux OutAmpCap

Table 527. ADC1Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 528. ADC1Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x00	Size of each step in the gain range, N/A since there are no steps
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x00	No steps, gain is fixed at 0dB
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.36.7. ADC1Mux OutAmpRight

Table 529. ADC1Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 530. ADC1Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

6.36.8. ADC1Mux OutAmpLeft

Table 531. ADC1Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 532. ADC1Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

6.37. ADC2Mux Node (NID = 0x1D)

6.37.1. ADC2Mux WCap

Table 533. ADC2Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 534. ADC2Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParamOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amp is present
[1]	InAmpPrsnt	R	0x0	No input amp
[0]	Stereo	R	0x1	Stereo widget

6.37.2. ADC2Mux ConLst

Table 535. ADC2Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 536. ADC2Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03 = Enabled 0x1 = Disabled	Number of NID entries in connection list.

6.37.3. ADC2Mux ConSelectCtrl

Table 537. ADC2Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 538. ADC2Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.37.4. ADC2Mux ConLstEntry

Table 539. ADC2Mux ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 540. ADC2Mux ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection
[23:16]	ConL2	R	0x14 = Enabled 0x0 = Disabled	DMic1 pin widget

Table 540. ADC2Mux ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x13 = Enabled 0x0 = Disabled	DMic0 pin widget
[7:0]	ConL0	R	0x1A	InPort2Vol widget

6.37.5. ADC2Mux LR

Table 541. ADC2Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 542. ADC2Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = swap left and right channels of this Widget.
[1:0]	Rsvd1	R	0x0	Reserved

6.37.6. ADC2Mux OutAmpCap

Table 543. ADC2Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 544. ADC2Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x00	Size of each step in the gain range, N/A since there are no steps

Table 544. ADC2Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x00	No steps, gain is fixed at 0dB
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.37.7. ADC2Mux OutAmpRight

Table 545. ADC2Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 546. ADC2Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

6.37.8. ADC2Mux OutAmpLeft

Table 547. ADC2Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 548. ADC2Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

7. ORDERING INFORMATION

7.1. STAC9227/9228/9228D Options and Part Order Numbers

Part Order Number	Voltage	SNR	DigMic	Dolby
STAC9228X5TAEyyX	5	95dB	Yes (Muxed)	No
STAC9228D5TAEyyX	5	95dB	Yes (Muxed)	Home Theater/Sound Room
STAC9228X3TAEyyX	3.3	95dB	Yes (Muxed)	No
STAC9228D3TAEyyX	3.3	95dB	Yes (Muxed)	Home Theater/Sound Room
STAC9227X5TAEyyX	5	95dB	No	No
STAC9227X3TAEyyX	3.3	95dB	No	No

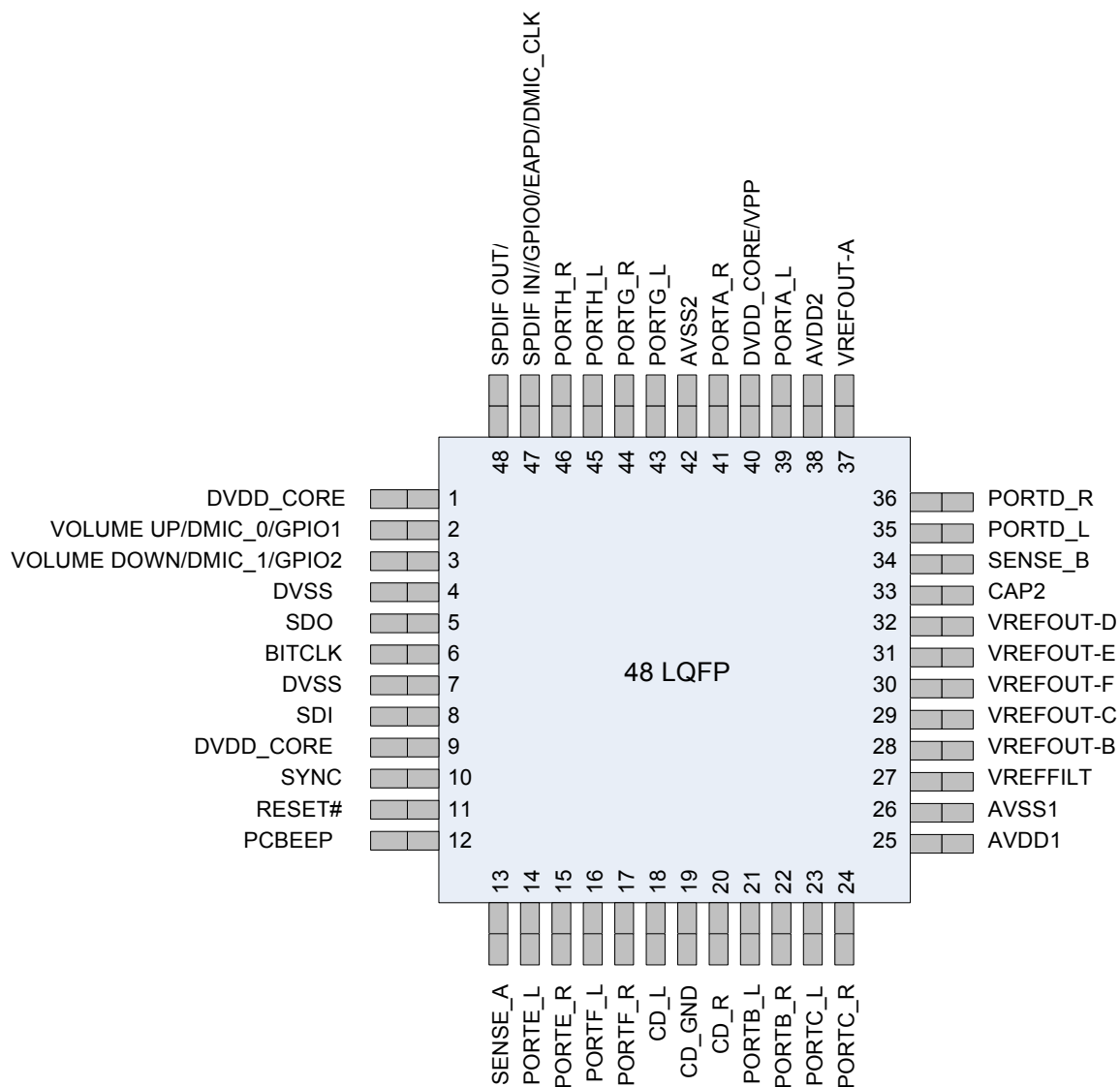
Table 549. STAC9227/9228/9229/9230 Options and Part Order Numbers

Note: When ordering these parts the “yy” will be replaced with the CODEC revision. Add an “R” to the end of any of these part numbers for delivery on Tape and Reel. The minimum order quantity for Tape and Reel is 2,000 units for 48-pin.

8. PIN INFORMATION

8.1. STAC9227/28/29/30 48-Pin LQFP Diagram

Figure 4. 48-Pin LQFP Pinout



Note: DMIC_CLK, DMIC_0, and DMIC_1 is only used on STAC9228X/D. When DMIC_CLK, DMIC_0, and DMIC_1 are unavailable, the pins are N/C

8.2. Pin Table

Table 550. Pin Table

Pin Name	Pin Function	I/O	Internal Pull-up/ Pull-down	Pin Location
DVDD_CORE	Digital Vdd = 3.3 V	I(Digital)	None	1
Volume Up/DMIC0/GPIO1	Volume Control OR Digital Mic 0 Input/General Purpose I/O	I/O(Digital)	Pull-Up 50 K Ω with Volume, GPIO or Pull-down 50 K Ω with Digital Mic	2
Volume Down/DMIC1/GPIO2	Volume Control OR Digital Mic 1 Input/General Purpose I/O	I/O(Digital)	Pull-Up 50 K Ω with Volume, GPIO or Pull-down 50 K Ω with Digital Mic	3
DVSS	Digital Ground	I(Digital)	None	4
SDATA_OUT	HD Audio Serial Data output (inbound stream)	I/O(Digital)	None	5
BIT_CLK	HD Audio Bit Clock	I(Digital)	None	6
DVSS3	Digital Ground	I(Digital)	None	7
SDATA_IN	HD Audio Serial Data (outbound stream)	O(Digital)	None	8
DVDD_CORE	Digital Vdd = 3.3 V	I(Digital)	None	9
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
PCBEEP	PC Beep	I(Analog)	None	12
SENSE_A	Jack insertion detection Ports A,B,C,D	I(Analog)	None	13
PORT-E_L	Input/Output of Left DAC2	I/O(Analog)	None	14
PORT-E_R	Input/Output of Right DAC2	I/O(Analog)	None	15
PORT-F_L	Input/Output of Left DAC3	I/O(Analog)	None	16
PORT-F_R	Input/Output of Right DAC3	I/O(Analog)	None	17
CD-L	CD Audio Left Channel	I(Analog)	None	18
CD-GND	CD Audio Analog Ground	I(Analog)	None	19
CD-R	CD Audio Right Channel	I(Analog)	None	20
PORT-B_L (HP)	Input/Output of Left DAC0,3 & 4	I/O(Analog)	None	21
PORT-B_R (HP)	Input/Output of Right DAC0, 3 & 4	I/O(Analog)	None	22
PORT-C_L	Input/Output of Left DAC1	I/O(Analog)	None	23
PORT-C_R	Input/Output of Right DAC1	I/O(Analog)	None	24
AVDD1	Analog Vdd = 3.3 V to 5 V	I(Analog)	None	25
AVSS1	Analog Ground	I(Analog)	None	26
VREF FILT	Analog Virtual Ground	O(Analog)	None	27
VREFOUT-B	Reference Voltage out drive (intended for mic bias) for Port B	O(Analog)	None	28

Table 550. Pin Table

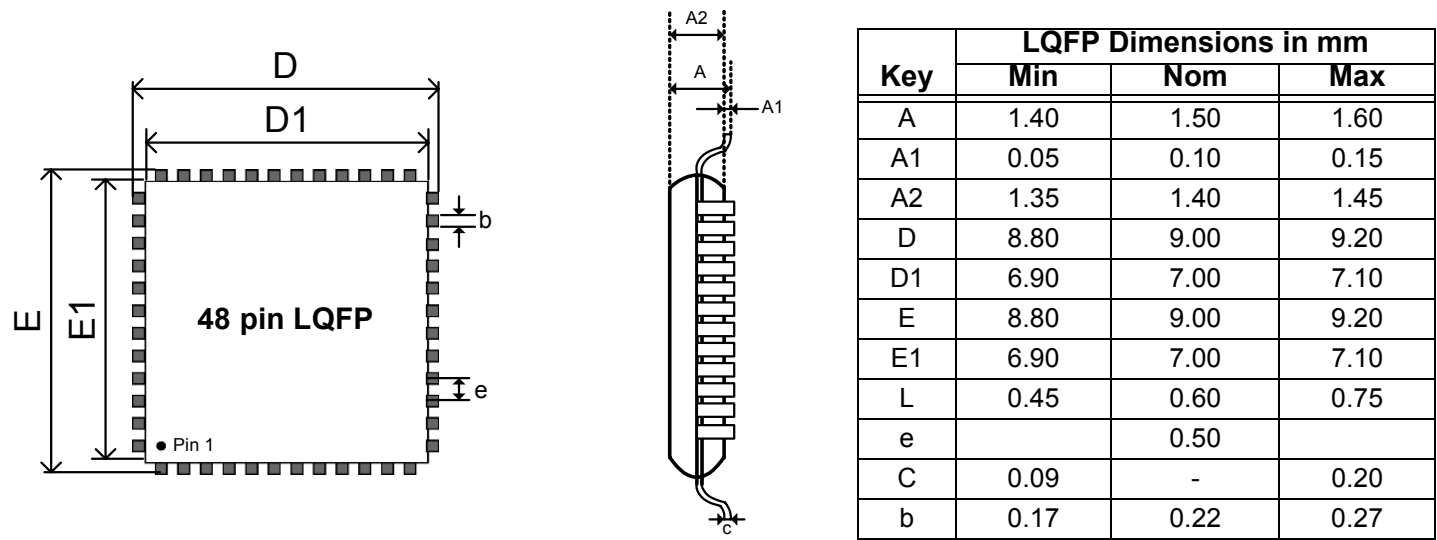
Pin Name	Pin Function	I/O	Internal Pull-up/ Pull-down	Pin Location
VREFOUT-C	Reference Voltage out drive (intended for mic bias) for Port C	O(Analog)	None	29
VREFOUT-F	Reference Voltage out drive (intended for mic bias) for Port F	O(Analog)	None	30
VREFOUT-E	Reference Voltage out drive (intended for mic bias) for Port E	O(Analog)	None	31
VREFOUT-D	Reference Voltage out drive (intended for mic bias) for Port D	O(Analog)	None	32
CAP2	ADC reference Cap	O(Analog)	None	33
SENSE_B	Jack insertion detection Ports E,F,G,H	I(Analog)	None	34
PORT-D_L (HP)	Input/Output of Left DAC0	I/O(Analog)	None	35
PORT-D_R (HP)	Input/Output of Right DAC0	I/O(Analog)	None	36
VREFOUT-A	Reference Voltage out drive (ntended for mic bias) for Port A	O(Analog)	None	37
AVDD2	Analog Vdd = 3.3 V to 5 V	I(Analog)	None	38
PORT-A_L (HP)	Input/Output of Left DAC0,3 & 4	I/O(Analog)	None	39
DVDD_CORE	Digital Vdd = 3.3 V	I(Analog)	None	40
PORT-A_R (HP)	Input/Output of Right DAC0, 3 & 4	I/O(Analog)	None	41
AVSS3	Analog Ground	I(Analog)	None	42
PORT-G_L	Input/Output of Left DAC2	I/O(Analog)	None	43
PORT-G_R	Input/Output of Right DAC2	I/O(Analog)	None	44
PORT-H_L	Input/Output of Left DAC1	I/O(Analog)	None	45
PORT-H_R	Input/Output of Right DAC1	I/O(Analog)	None	46
SPDIFIN/GPIO0/EAPD/DMIC_CLK	SPDIF Input, General Purpose I/O, EAPD, Digital Mic Ouput Clock	I/O(Digital)	Pull-up 50 K Ω or more	47
S/PDIF-OUT	SPDIF digital output (50 K Ω internal pull-down)	O(Digital)	50 K Ω internal pull-down	48

9. PACKAGE OUTLINE AND PACKAGE DIMENSIONS

Package dimensions are kept current with JEDEC Publication No. 95.

9.1. 48-Pin LQFP

Figure 5. 48-Pin LQFP Package Outline and Package Dimensions



10. SOLDER REFLOW PROFILE

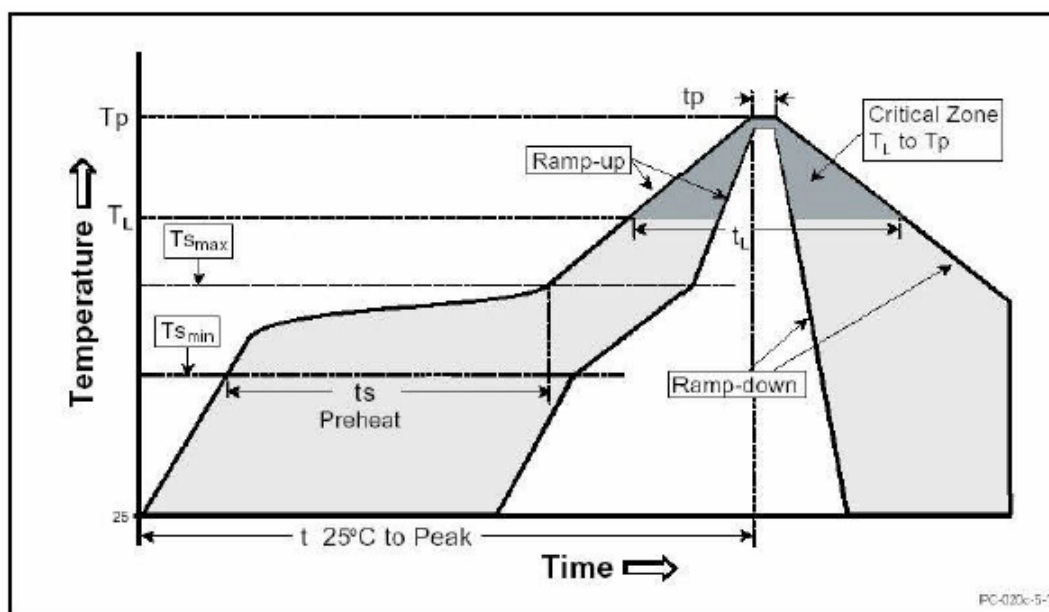
10.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature	Pb Free Assembly
Average Ramp-Up Rate ($T_{s_{max}} - T_p$)	3 °C / second max
Preheat Temperature Min ($T_{s_{min}}$)	150 °C
Preheat Temperature Max ($T_{s_{max}}$)	200 °C
Preheat Time ($t_{s_{min}} - t_{s_{max}}$)	60 - 180 seconds
Time maintained above Temperature (T_L)	217 °C
Time (t_L)	60 - 150 seconds
Peak / Classification Temperature (T_p)	See "Package Classification Reflow Temperatures" on page 229.
Time within 5 °C of actual Peak Temperature (t_p)	20 - 40 seconds
Ramp-Down rate	6 °C / second max
Time 25 °C to Peak Temperature	8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.	

Figure 6. Solder Reflow Profile



10.2. Pb Free Process - Package Classification Reflow Temperatures

Package Type	MSL	Reflow Temperature
LQFP 48-pin	3	260 °C*

11. REVISION HISTORY

Revision	Date	Description of Change
0.3	July 2005	Initial release.
0.5	August 2005	Updated Pin Outs and Pin Tables, Added Updated performance tables to show all voltage options, Updated Diagrams, Added Widget Diagram, Added Pin Configuration Default Register Settings Table, Added Part Numbers. Added 56-QFN Reflow Profile Information. Added Widget Information. Updated ESD Information. Added 40dB Boost Information.
0.7	May 2006	Updated logo. Added ADAT logo. Added Audio Jack Presence Detect section. Updated Power Consumption numbers.
0.82	8 October 2006	Initial release in IDT format.
1.0	March 2007	Removed 56 QFN package option for STAC9230. Corrected the missing "X" in the orderable part number.
1.1	January 2008	Removed STAC9229, STAC9230, STAC9227D options, as EOL issued.

Innovate with IDT audio for high fidelity. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

HA.CM@idt.com

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Europe

IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

