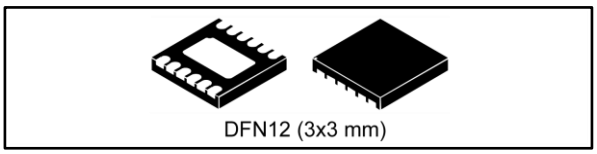
STNS01

Li-Ion linear battery charger with LDO

Datasheet - production data



Features

- Charges single-cell Li-Ion batteries with CC/CV algorithm and charge termination
- Charge current programmable up to 200 mA
- 1% accuracy on floating voltage (4.2 V)
- Integrated 3.1 V LDO regulator
- Automatic power path management
- Battery overcharge protection
- Battery over-discharge protection
- Battery overcurrent protection
- Charging timeout
- Very low battery leakage in over-discharge/shutdown mode
- Low quiescent current
- Charge/fault status output
- Charger enable input
- Available in a DFN12L (3x3x0.75 mm) package

Applications

- Portable MP3 players
- Portable low-power devices
- Fitness portable devices

Description

The STNS01 is a linear charger for single-cell Li-Ion batteries integrating an LDO regulator and several battery protection functions.

The STNS01 uses a CC/CV algorithm to charge the battery; the fast-charge current can be programmed using an external resistor. Pre-charge current and termination current are scaled accordingly. The floating voltage value is 4.2 V.

The input supply voltage is normally used to charge the battery and provide power to the LDO regulator. When a valid input voltage is not present and the battery is not empty, the device automatically switches to battery power.

The STNS01 integrates overcharge, over-discharge and overcurrent protection circuitry to prevent the battery from being damaged under fault conditions. It also features a charger enable input to stop the charging process when battery overtemperature is detected by an external circuitry.

When the shutdown mode is activated, the battery power consumption is reduced to less than 500 nA to maximize battery life during shelf time or shipping. The device is available in the DFN12L (3x3x0.75 mm) package.

Table 1: Device summary

Order code	Package	Packing
STNS01PUR	DFN12L (3x3x0.75 mm)	3000 parts per reel

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1 Application schematic

Figure 1: STNS01 application schematic

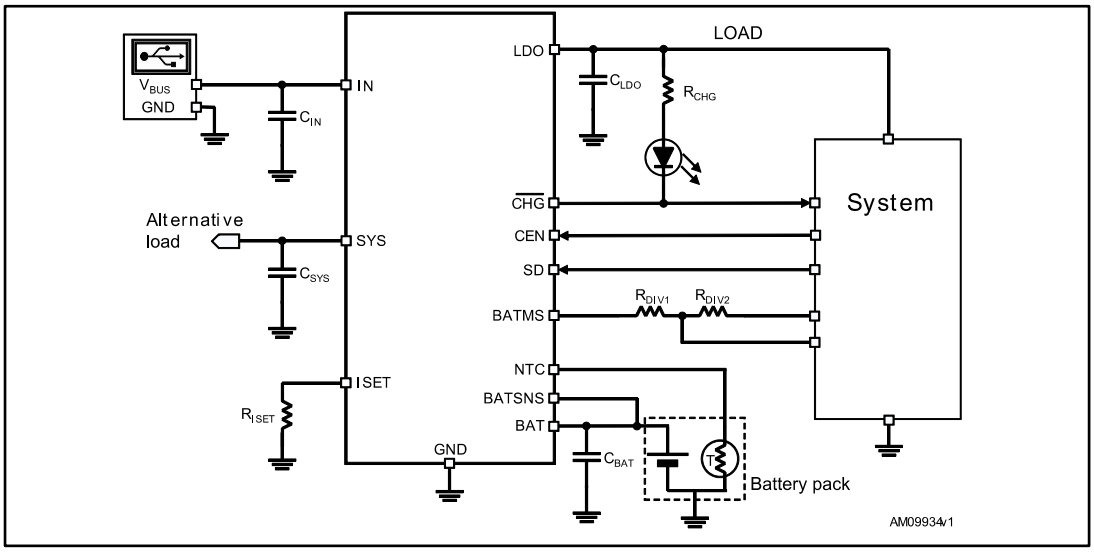
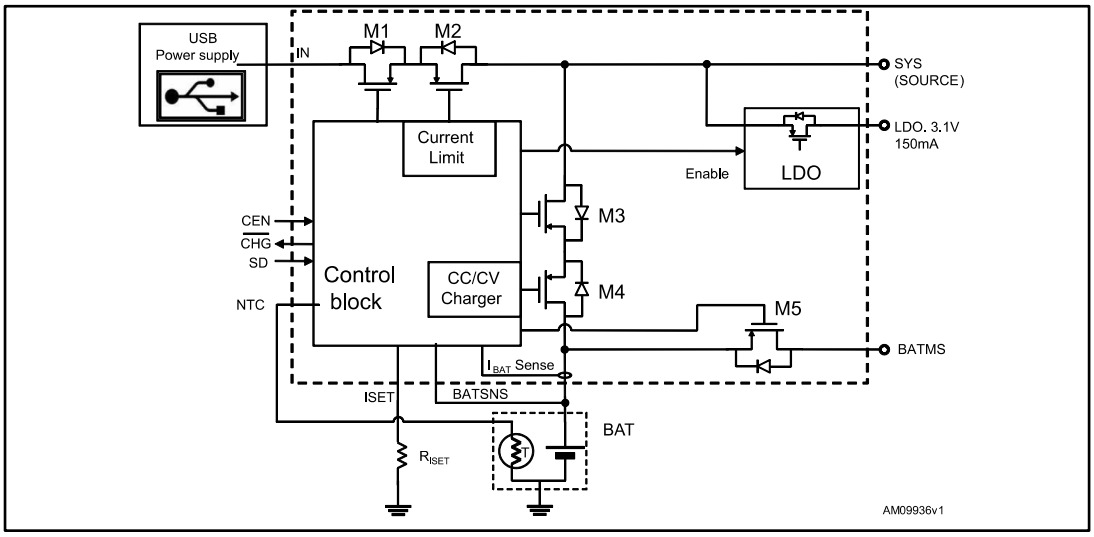


Table 2: List of external components

Symbol	Manufacturer	Value	Description	Size
C_{IN}	Murata	2.2 µF	GRM188R71A225KE15D	0603
C_{SYS}	Murata	2.2 µF	GRM188R71A225KE15D	
C_{LDO}	Murata	2.2 µF	GRM188R71A225KE15D	
R_{ISET}	Any	1 kΩ – 13 kΩ	Resistor	
C_{BAT}	Murata	4.7 µF	GRM188R61A475KE15D	
D1	Any		Diode led	
$R_{DIV1, DIV2}$	Any		Depending on the BATMS status	
R_{CHG}	Any	600 Ω	Resistor	
C_{LDO}		2.2 µF	GRM188R71A225KE15D	

2 Block diagram

Figure 2: STNS01 block diagram



3 Pin configuration

Figure 3: Pin configuration (top view)

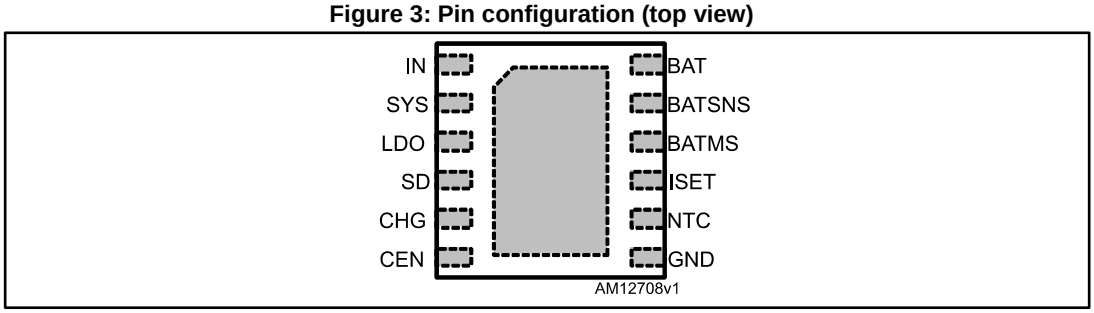


Table 3: Pin description

Pin name	Number	Description
IN	1	Input supply voltage. Bypass this pin to ground with a 2.2 µF capacitor
SYS	2	System output. Bypass this pin to GND with a 2.2 µF ceramic capacitor
LDO	3	3.1 V LDO output. Bypass this pin to ground with a 1 µF ceramic capacitor
SD	4	Shutdown. Active high. 500 kΩ internal pull-down
CHG	5	Charging/fault flag. Active low
CEN	6	Charger enable pin. Active high. 500 kΩ internal pull-up (to LDO)
GND	7	Ground
NTC	8	Battery temperature monitor pin
ISET	9	Fast-charge programming resistor
BATMS	10	Battery voltage measurement pin
BATSNS	11	Battery voltage sensing. Connect as close as possible to the battery positive terminal
BAT	12	Battery positive terminal. Bypass this pin to GND with a 4.7 µF ceramic capacitor
Exposed pad		Connect to GND

4 Maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_{IN}	Input supply voltage pin	DC voltage	-0.3 to +10.0	V
		Non repetitive, 60 s pulse length	-0.3 to +16.0	V
V_{LDO}	LDO output pin voltage	DC voltage	-0.3 to +4.0	V
V_{SYS}	SYS pin voltage	DC voltage	-0.3 to +6.5	V
V_{CHG}	CHG pin voltage	DC voltage	-0.3 to +6.5	V
V_{LGC}	Voltage on logic pins (CEN, SD)	DC voltage	-0.3 to +4.0	V
V_{ISET}	Voltage on ISET pin	DC voltage	-0.3 to +2	V
V_{NTC}	Voltage on NTC pin	DC voltage	-0.3 to 3.1	V
V_{BAT}, V_{BATSNS}	Voltage on BAT, BATSNS pins	DC voltage	-0.3 to +5.5	V
V_{BATMS}	Voltage on BATMS pin	DC voltage	-0.3 to V_{BAT}+0.3	V
ESD	Human body model	JS-001-2010	±2000	V
T_{AMB}	Operating ambient temperature		-40 to +85	°C
T_J	Maximum junction temperature		+125	°C
T_{STG}	Storage temperature		-65 to +150	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	49	°C/W
R_{thJC}	Thermal resistance junction-case	4.2	

5 Electrical characteristics

The values given in the following table are valid for - 40 °C < T_J < + 85 °C, V_{IN} = 5 V, V_{BAT} = 3.6 V, C_{LDO} = 1 µF, C_{BAT} = 4.7 µF, C_{IN} = C_{SYS} = 2.2 µF, R_{ISET} = 1 kΩ, SD = low, CEN = high, unless otherwise specified.

Table 6: Electrical characteristics

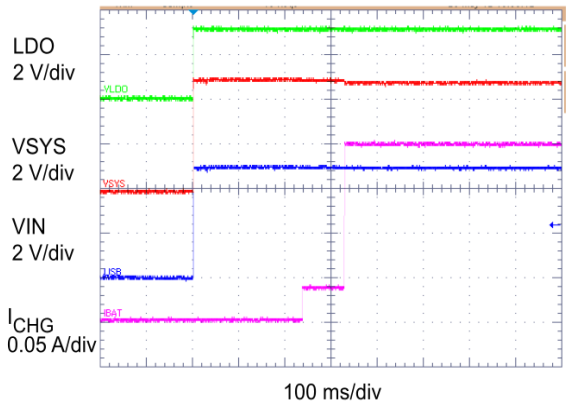
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage	V_{IN} rising	4.55		5.4	V
V_{INOVP}	Input overvoltage protection	V_{IN} rising	5.6	5.9	6.2	V
V_{INOVPH}	Input overvoltage protection hysteresis	V_{IN} falling		200		mV
V_{UVLO}	Undervoltage lock-out	V_{IN} falling	3.95	4.18	4.35	V
V_{UVLOH}	Undervoltage lock-out hysteresis	V_{IN} rising		300		mV
I_{IN}	IN supply current	Charger disabled mode (CEN = low), I_{SYS} = I_{LDO} = 0 A		400		µA
		Charging, V_{HOT} < V_{NTC} < V_{COLD}, including R_{ISET} current		1.4		mA
V_{FLOAT}	Battery floating voltage	I_{BAT} = 1 mA	4.158	4.2	4.242	V
I_{BAT}	BAT pin supply current	Battery-powered mode (V_{IN} < V_{UVLO}), I_{LDO} = 0 A		6	10	µA
		Standby mode, charge terminated		6	10	µA
		Shutdown mode (SD = high)		100	500	nA
		Over-discharge mode (V_{BAT} < V_{ODC}, V_{IN} < V_{UVLO})		100	500	
I_{FAST}	Fast-charge current	R_{ISET} = 500 Ω, constant-current mode I_{LDO} + I_{SYS} < 100 mA		400		mA
		R_{ISET} = 1 kΩ, constant-current mode	180	200	220	
		R_{ISET} = 13 kΩ, constant-current mode	12	15	18	
R_{ISET}	Fast-charge programming resistor range		1		13	kΩ
V_{ISET}	I_{SET} regulated voltage			1		
V_{PRE}	Pre-charge to fast-charge battery voltage threshold	Charger active		3		V
I_{PRE}	Pre-charge current	V_{BAT} < 3 V, charger active		20		%I_{FAST}
I_{END}	End-of-charge current	Charging in CV mode		10		%I_{FAST}
V_{OCHG}	Battery voltage overcharge threshold	V_{BAT} rising	4.245	4.275	4.305	V
V_{ODC}	Battery voltage over-discharge threshold	V_{IN} < V_{UVLO}, I_{LDO} = 100 mA	2.750	2.8	2.850	V
V_{ODCR}	Battery voltage over-discharge release threshold			3.0		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON-IB}	Input to battery on-resistance			1	1.5	Ω
R_{ON-BS}	Battery to SYS on-resistance	I_{SINK} = 100 mA		0.38	0.55	Ω
$R_{ON-BATMS}$	BATSNS to BATMS on-resistance	I_{SINK} = 500 µA		270		Ω
V_{OL}	Output low level (CHG)	I_{SINK} = 5 mA			0.4	V
V_{IL}	Logic low input level (CEN, SD)	V_{LDO} = 3.1 V			0.4	V
V_{IH}	Logic high input level (CEN, SD)		1.6			V
R_{UP}	CEN pull-up resistor		375	500	625	kΩ
R_{DOWN}	SD pull-down resistor		375	500	625	kΩ
V_{LDO}	LDO output voltage	I_{LDO} = 1 mA	3.007	3.1	3.193	V
$\Delta V_{OUT-LOAD}$	LDO static load regulation	I_{LDO} = 1 mA to 150 mA		±0.002		%/mA
I_{SC}	LDO short-circuit current	R_{LOAD} = 0 Ω	250	350		mA
I_{BATOCP}	Battery discharge overcurrent protection	V_{IN}<V_{UVLO} (powered from BAT)	400		650	mA
I_{INLIM}	Input current limitation	V_{SYS}> $V_{ILIMSCTH}$; V_{UVLO} < V_{IN} < V_{INOVP} (powered from IN)		1		A
$I_{ININSCTH}$	Input current limitation in short-circuit conditions	V_{SYS} < $V_{ILIMSCTHINOVP}$ (powered from IN)		400		mA
$V_{ILIMSCT H}$	SYS voltage threshold for input current limitation short-circuit detection	V_{UVLO} < V_{IN} < V_{INOVP}		2		V
V_{SCLDO}	LDO short-circuit protection threshold	V_{IN} < V_{UVLO} or V_{IN} > V_{INOVP} (powered from BAT)		0.7		V
V_{SCSYS}	SYS short-circuit protection threshold	V_{IN} < V_{UVLO} or V_{IN} > V_{INOVP} (powered from BAT)		V_{BAT} - 0.8		V
I_{NTCB}	NTC pin bias current	V_{NTC} = 0.25 V	48	50	52	µA
V_{HOT}	Thermal hot threshold	Increasing NTC temperature	0.234	0.246	0.258	V
V_{COLD}	Thermal cold threshold	Decreasing NTC temperature	1.28	1.355	1.43	V
T_{HYST}	Hot/cold temperature threshold hysteresis	10 kΩ NTC, ß = 3370		3		°C
T_{SD}	Thermal shutdown die temperature			180		°C
T_{FAULT}	CHG pin blinking frequency	Fault condition		1		Hz
t_{CHGD}	Input voltage connection to charging-start delay	V_{BAT} = 3.5 V, R_{NTC} = 10 kΩ, battery detection not included (t_{BDSRC} + t_{BDSNK})		240		ms
t_{OCD}	Overcharge detection delay	V_{BAT}> V_{OCHG}, V_{UVLO}<V_{IN}<V_{INOVP}		1.2		s
t_{ODD}	Over-discharge detection delay	V_{BAT} < V_{ODC} and V_{IN} < V_{UVLO} or V_{IN}> V_{INOVP}		400		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DOD}	Discharge overcurrent detection delay	I_{BAT}> I_{BATOCP}, V_{IN}<V_{UVLO} or V_{IN}> V_{INOVP}		14		ms
t_{PFD}	Pre-charge to fast-charge transition deglitch time	Rising		100		ms
t_{FPD}	Fast-charge to pre-charge fault deglitch time			10		ms
t_{END}	End-of-charge deglitch time			100		ms
t_{PRE}	Pre-charge timeout	V_{BAT} < V_{PRE}, charging		1800		s
t_{FAST}	Fast-charge timeout			36000		s
t_{NTCD}	Battery temperature transition deglitch time			100		ms
t_{PW}	CEN/SD valid input pulse width		30			ms
t_{THPD}	Thermal protection deglitch time			10		ms

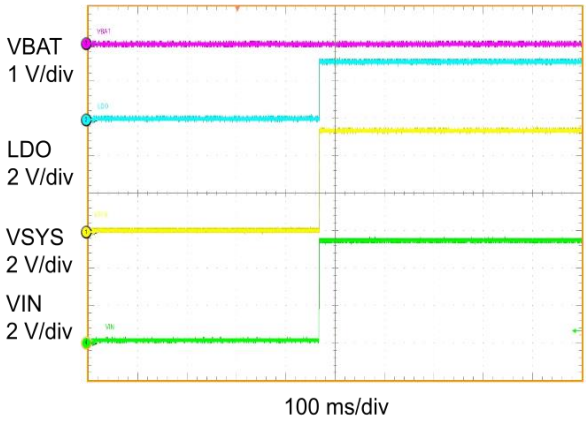
6 Typical performance characteristics (curves)

Figure 4: Start-up



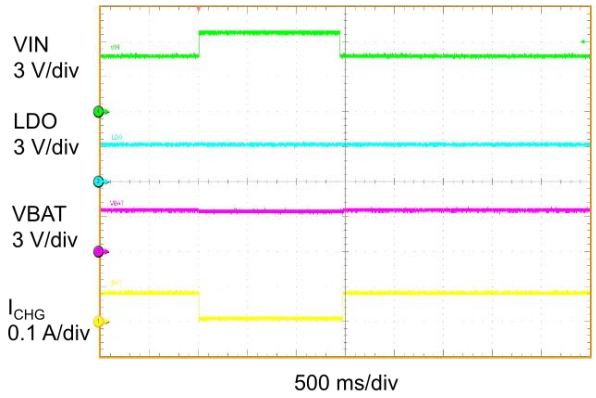
V_{IN} = 0 V to 5 V, V_{BAT} = 3.6 V, I_{CHG} = 200 mA

Figure 5: Start - up VBAT = 0 V



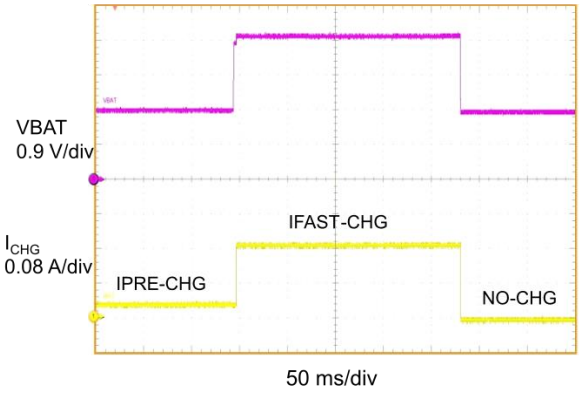
V_{IN} = 0 V to 5 V, V_{BAT} = 30 V, I_{CHG} = 100 mA

Figure 6: Input OVP



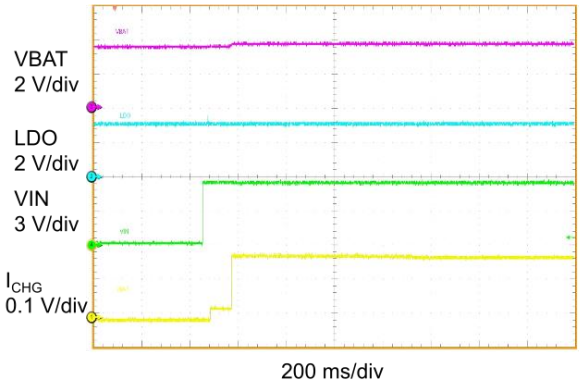
V_{IN} = 5.5 V to 6.8 V, V_{BAT} = 3.6 V, I_{CHG} = 100 mA

Figure 7: IPRE-CHG to IFAST-CHG



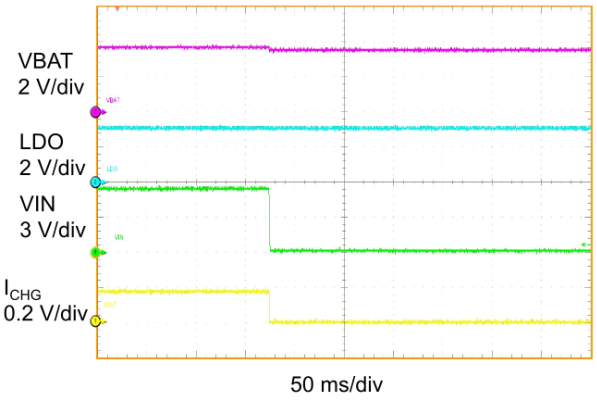
V_{IN} = 5 V, V_{BAT} = 1.8 V - 3.6 V, I_{CHG} = 200 mA

Figure 8: Plug USB



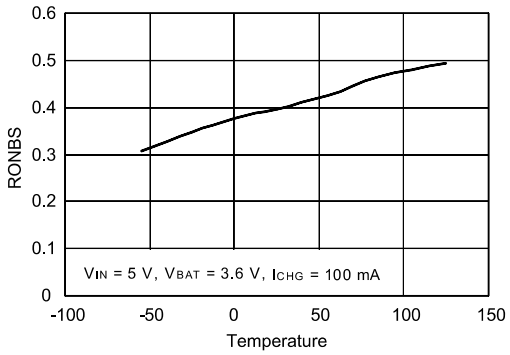
V_{IN} = 0 V to 5 V, V_{BAT} = 3.6 V, I_{CHG} = 200 mA

Figure 9: Unplug USB (battery powered)



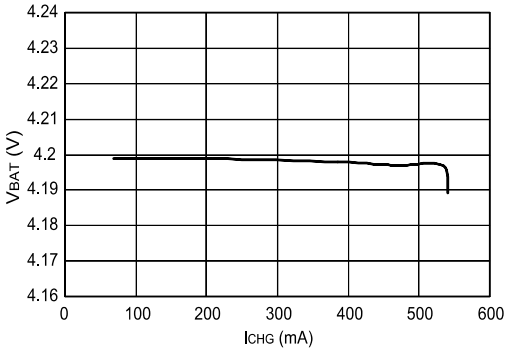
V_{IN} = 5 V to 0 V, V_{BAT} = 3.6 V, I_{CHG} = 200 mA

Figure 10: RON-BS vs. temperature



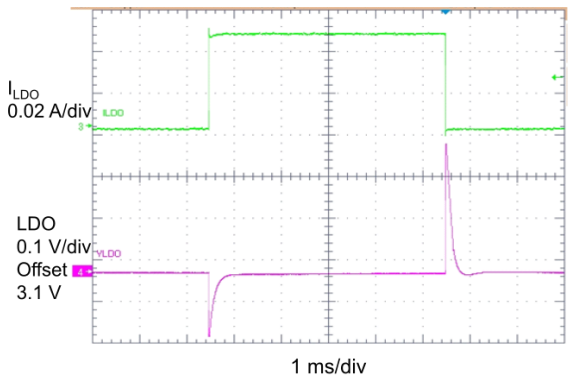
Shutdown mode to battery mode transition. V_{IN} floating

Figure 11: Battery voltage vs. charge current



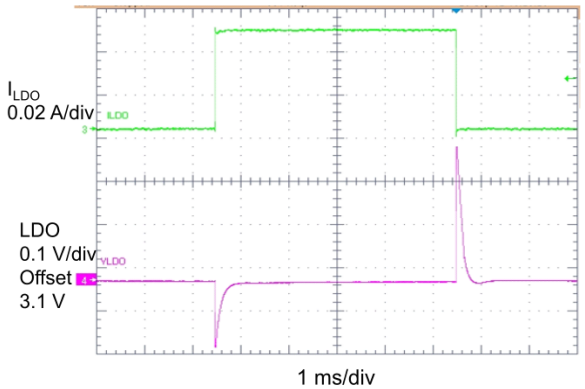
Shutdown mode to V_{IN} mode transition

Figure 12: Load transient LDO pre-chg



V_{IN} = 5 V, V_{BAT} < V_{PRE}, I_{PRE} = 20 mA, I_{LDO} = 0 to 50 mA

Figure 13: Load transient LDO fast-chg



V_{IN} = 5 V, V_{BAT} ≥ V_{PRE}, I_{FAST} = 100 mA, I_{LDO} = 0 to 50 mA

Figure 14: VLDO vs. temperature

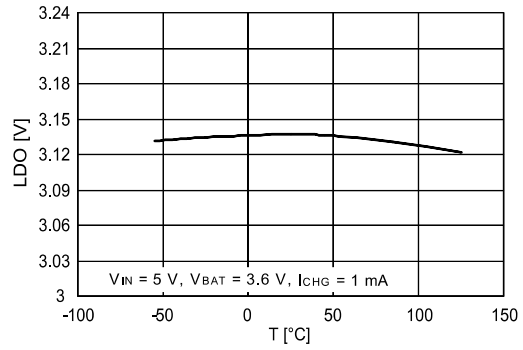
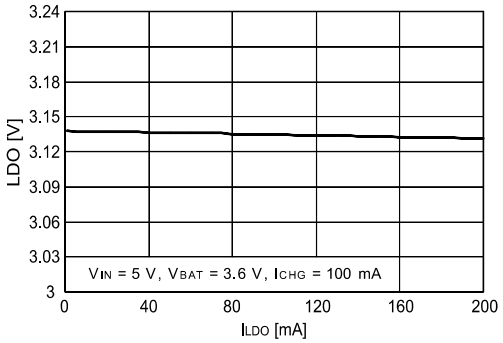


Figure 15: VLDO load static regulation



6.1 IN

5 V input supply voltage.

This pin supplies power to the SYS pin and the battery charger when the input voltage is higher than V_{UVLO} and lower than V_{INOVP}. Bypass this pin to GND with a 2.2 µF ceramic capacitor.

6.2 SYS

LDO input voltage. This pin can be used to supply up to 100 mA to the external devices. The voltage source of this pin can be either IN or BAT depending on the operating conditions. Refer to table below for more details. Bypass this pin to GND with a 2.2 µF ceramic capacitor.

Table 7: SYS pin voltage

V_{IN}	V_{BAT}	V_{SYS}	LDO
> V_{UVLO} and < V_{INOVP}	X (do not care)	V_{IN}(1)	ON
< V_{UVLO}	< V_{ODC}(2)	Not powered	OFF
< V_{UVLO}	< V_{ODC}(2)	V_{BAT}(1)	ON
> V_{INOVP}	< V_{ODC}(2)	Not powered	OFF
> V_{INOVP}	< V_{ODC}(2)	V_{BAT}(1)	ON

Notes:

(1)Voltage drop over internal MOSFETs is not included.

(2)V_{ODCR} if shutdown mode or over-discharge protection has been previously activated.

6.3 LDO

LDO output voltage.

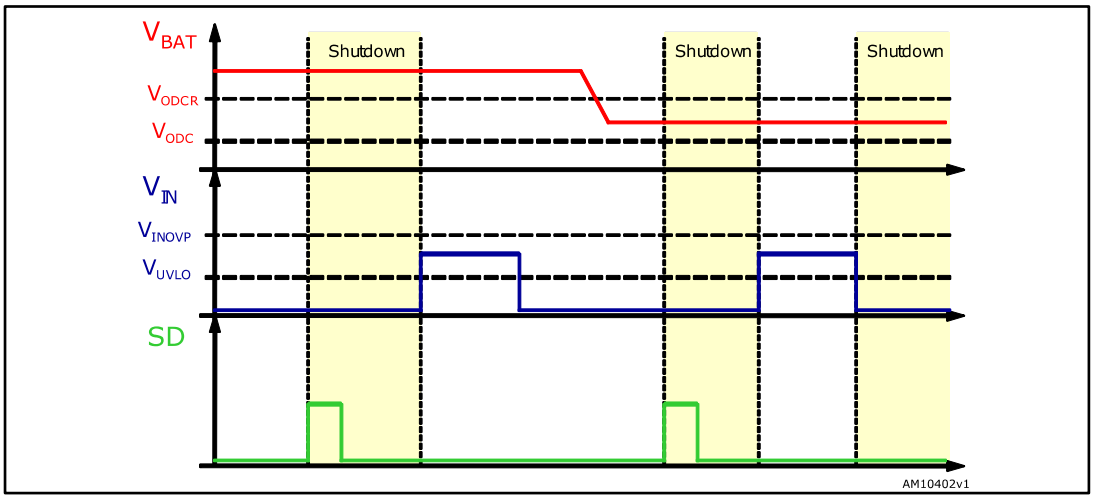
This pin outputs a 3.1 V regulated voltage and can supply up to 100 mA. Bypass this pin to GND with a 1 µF ceramic capacitor.

6.4 SD

Shutdown input. A logic high level on this pin when the input voltage (V_{IN}) is not valid makes the device enter shutdown mode. In this mode the battery drain is reduced to less than 500 nA and the SYS and LDO voltages are not present. Connecting a valid input

voltage (V_{UVLO}<V_{IN}<V_{INOVP}) restores normal operating conditions if the battery voltage is higher than V_{ODCR}. If the device is in shutdown mode and the battery voltage is lower than V_{ODCR}, when a valid input voltage is connected and then disconnected again, the STNS01 does not exit shutdown mode (see figure below). This pin has an internal 500 kΩ pull-down resistor.

Figure 16: Shutdown mode entry and exit (not to scale, deglitch times not included)



6.5 CHG

Active-low open-drain charging/fault flag. This pin is active when the charging process is ongoing and toggles at 1 Hz if a fault condition has been detected. Refer to table below for more details. This pin is active only when a valid voltage is connected to the IN input (V_{UVLO} < V_{IN} < V_{INOVP}).

Table 8: CHG pin state

Device state	CHG pin state
Not charging	High Z
Charging	Low
Battery temperature fault	Toggling
Overcharge fault	Toggling
Charging timeout (pre-charge, fast-charge)	Toggling
Battery voltage below V_{PRE} after the fast-charge starts	Toggling

6.6 CEN

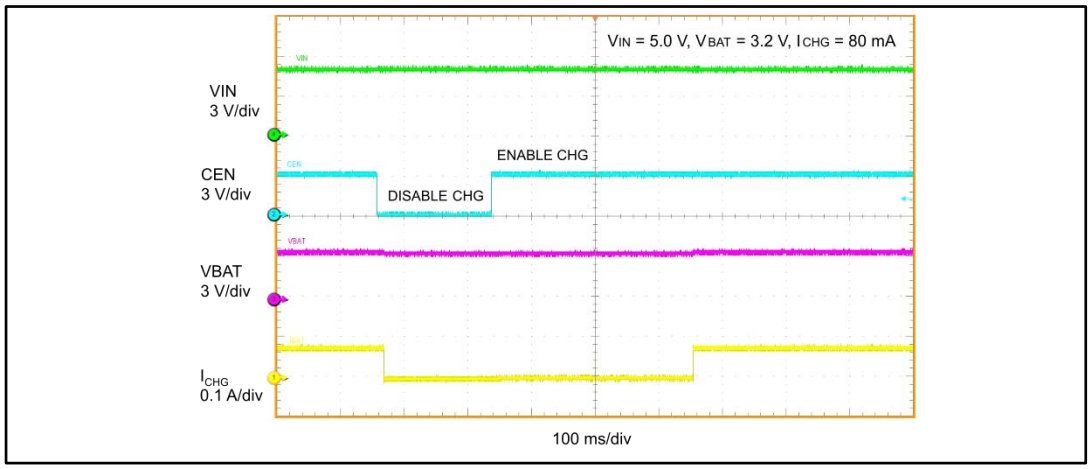
Charger enable pin. A logic low level on this pin disables the battery charger. A transition from high to low and then back to high restarts the charger when the charge cycle has been stopped for one of the following reasons:

- Charging timeout (pre-charge, fast-charge)
- Battery voltage below V_{PRE} after the fast-charge has already started
- End-of-charge

CEN has no effect if the charging cycle has been stopped by a battery overcharge condition.

If the charger is temporarily stopped because of the battery temperature being out of the normal range, a logic low level on the CEN pin disables the charger and resets the charging timeout timers. If CEN is then driven high again the charger is restarted only if a no-fault condition is active (including battery temperature out of range). This pin has an internal 500 kΩ pull-up resistor connected to LDO and must be left floating or tied high at power on.

Figure 17: Charge disable / enable



6.7 GND

The device ground pin.

6.8 NTC

Battery temperature monitoring pin. Connect the battery NTC resistor to this pin. The charging cycle is put on hold when the battery temperature is outside of the safe temperature range (0 °C to 45 °C).

6.9 ISET

Fast-charge current programming pin. Connect a resistor (R_{ISET}) to ground to set the fast-charge current (I_{FAST}) according to the following equation:

$I_{FAST} = V_{ISET} / R_{ISET} * K$

Where V_{ISET} = 1 V and K = 200. Fast-charge currents ranging from 15 mA to 200 mA can be programmed. Pre-charge current and end-of-charge current are scaled accordingly. Charging currents higher than 200 mA can be programmed but the increased voltage drop over internal MOSFETs can limit the minimum input voltage (V_{IN}) needed to obtain full charge.

6.10 BATMS

Battery voltage measurement pin. This pin is internally shorted to the BATSNS pin during normal operating conditions to monitor the battery voltage. The BATMS pin is disconnected from the battery if the LDO output voltage drops to zero (battery discharge overcurrent, battery over-discharge, shutdown mode, short-circuit on SYS or LDO).

6.11 BATSNS

Battery voltage sense pin. This pin is needed to ensure accuracy on the floating voltage and battery voltage protection thresholds. The BATSNS pin must be connected as close as possible to the battery positive terminal.

6.12 BAT

Battery positive terminal connection pin. Bypass this pin to GND with a 4.7 µF ceramic capacitor.

7 Operation description

The STNS01 is a power management IC integrating a battery charger with a power path function, a battery temperature monitoring and a 3.1 V 100 mA LDO.

When a valid input voltage (V_{IN}) is present on the IN pin, after security checks are performed, the battery charger starts charging the battery using a constant-current/constant-voltage charging algorithm. The input voltage (V_{IN}) is considered to be valid if it is higher than V_{UVLO} and lower than V_{INOVP}. The power path architecture allows charging the battery and supplying the system at the same time. When the input voltage is not valid, the LDO (and every external IC connected to SYS) is supplied by the battery through a low resistance path. The device also provides protection to the battery against the following fault conditions:

- Overcharge
- Over-discharge
- Charge overcurrent
- Discharge overcurrent

If a fault condition is detected when the input voltage is valid ($V_{UVLO} < V_{IN} < V_{INOVP}$), the CHG pin starts toggling, to inform the control logic that an error occurred.

The device can also be put in reduced battery drain mode (shutdown, I_{BAT} < 500 nA) to maximize battery life during end-product shipping and shelf time.

7.1 Power-on

When the device is in shutdown mode, the pins LDO and SYS are not supplied. In order to turn the device on a valid input voltage must be connected (V_{IN}). The CEN pin must be floating or tied high during power-on for proper operations.

7.2 Battery charger

The STNS01's battery charger is designed to charge single cell Li-Ion batteries up to 4.2 V using a CC-CV charging algorithm. When a valid input voltage is detected, the STNS01 starts the charge cycle and the CHG pin switches from high impedance to low level. The charging process starts if the battery voltage is higher than V_{BATMIN}. If the battery is deeply discharged (the battery voltage is lower than V_{PRE} and higher than V_{BATMIN}) the charger enters the pre-charge phase and starts charging in constant-current mode using a low current (I_{PRE} = 20% I_{FAST}). If the battery voltage does not reach the V_{PRE} threshold within t_{PRE}, the charging process is stopped and a fault is signaled. When the battery voltage reaches the V_{PRE} threshold, the constant-current fast-charge phase is entered and the charging current is increased to I_{FAST}. The value of I_{FAST} can be programmed from 15 mA to 200 mA using an external resistor as described in the I_{SET} pin description. Once the fast-charge phase has started, if the battery voltage decreases again below V_{PRE}, the charging process is stopped and a fault is signaled. The constant-current fast-charge phase lasts as long as the battery voltage is lower than V_{FLOAT}. When V_{BAT} reaches V_{FLOAT}, the charging algorithm switches to constant-voltage (CV) mode. During the CV mode the battery voltage is regulated to V_{FLOAT} and the charging current starts decreasing. When the charging current reaches the I_{END} threshold (I_{END} = 10% I_{FAST}), the charging process is stopped and the CHG pin is put in high impedance. If the fast-charge phase is not terminated within t_{FAST}, the charging process is stopped and a fault is signaled. The battery temperature is monitored throughout the charging cycle for safety reasons. Refer to figure below for a simplified flowchart of the charging process.

Figure 18: Charging flowchart

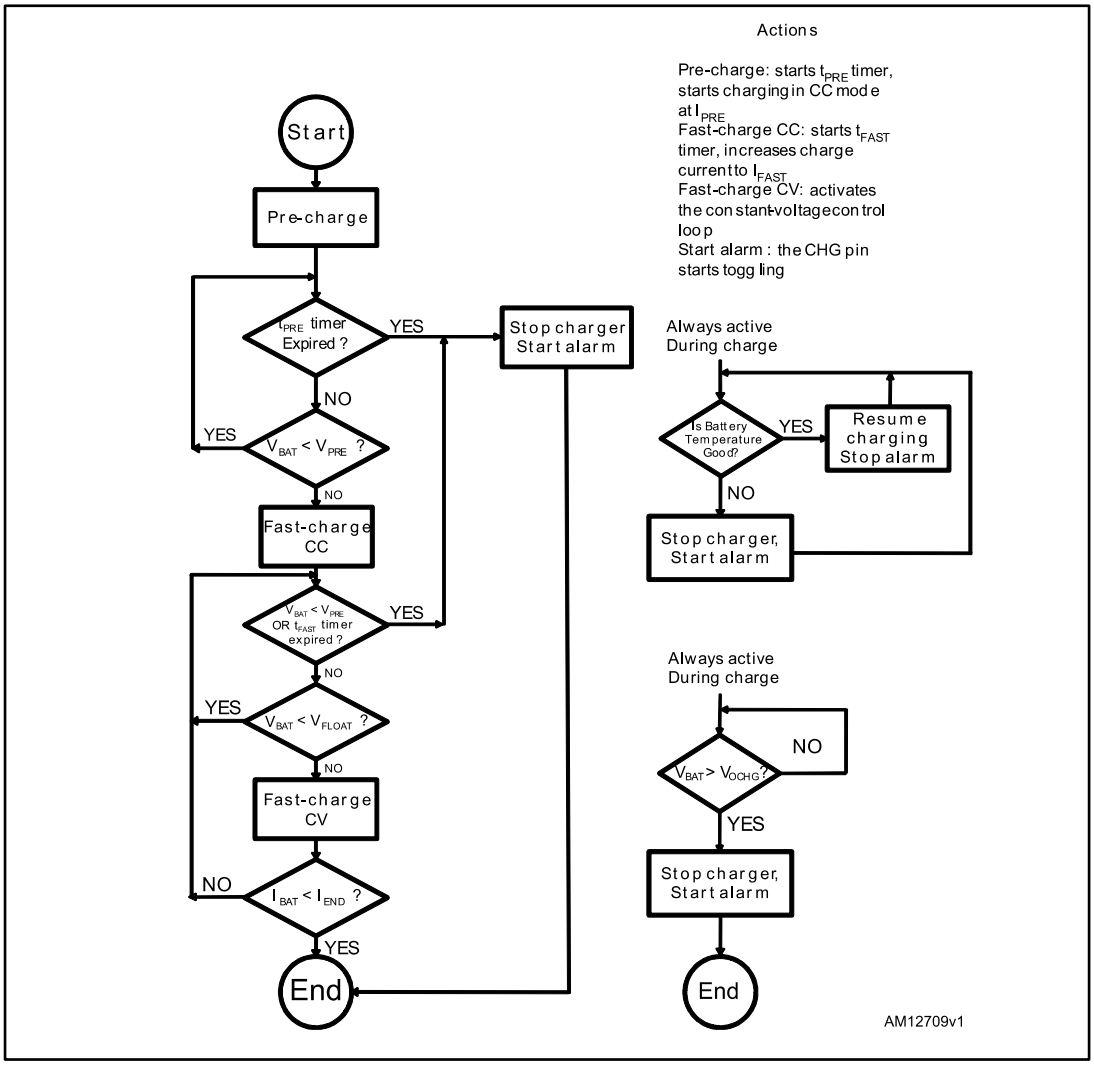


Figure 19: CC-CV charging profile (not to scale)

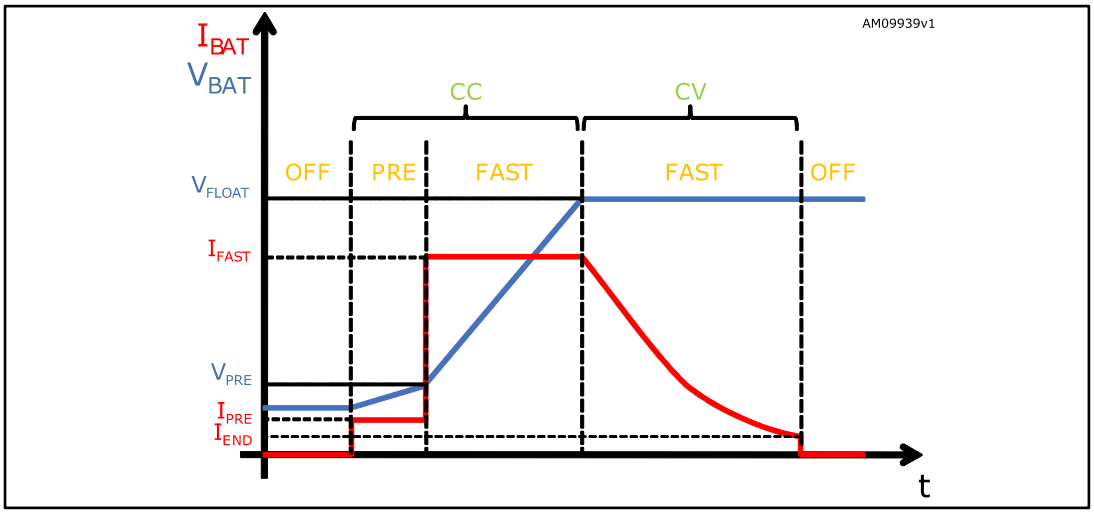
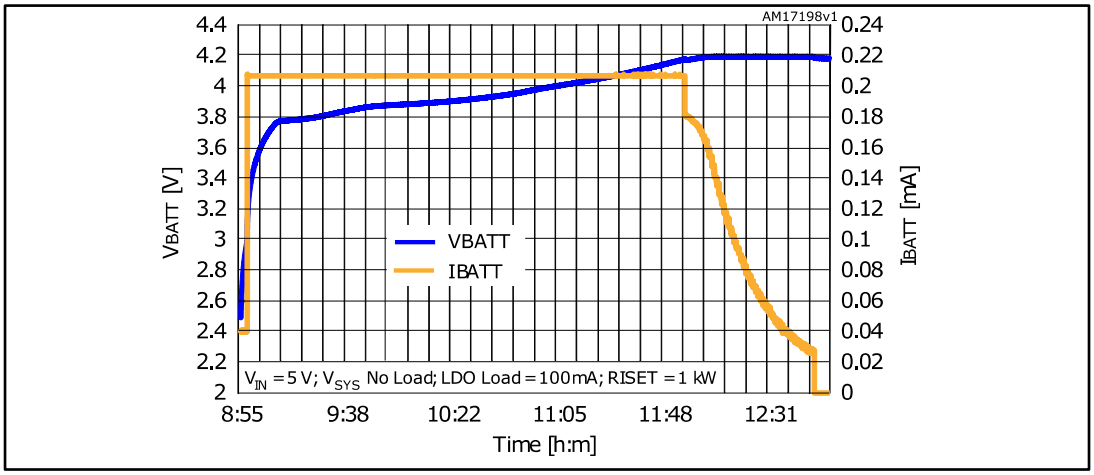


Figure 20: Charging cycle profile



7.3 Battery temperature monitoring

The STNS01 integrates the comparators, biasing circuit and control logic needed to monitor the battery temperature through an external NTC resistor. This feature is active only during the battery charging process in order to save power when the system is supplied from the battery. When the battery temperature goes outside the normal operating range (0 - 45 °C), the charging process is put on hold, the alarm signal is activated (the CHG pin toggles) but the charging timeout timers are kept running.

If the temperature goes back into the normal operating range before the maximum charging time has elapsed, the charging process is resumed from where it left off and the alarm signal is cleared. If the charging timeout expires while the temperature is still outside the normal operating range, the charging process is stopped but can be restarted using the CEN pin. Both temperature thresholds feature a 3 °C hysteresis. The battery temperature monitoring block is designed to work with an NTC thermistor having R_{25} = 10 kΩ and ß = 3370 (e.g. Mitsubishi TH05-3H103F).

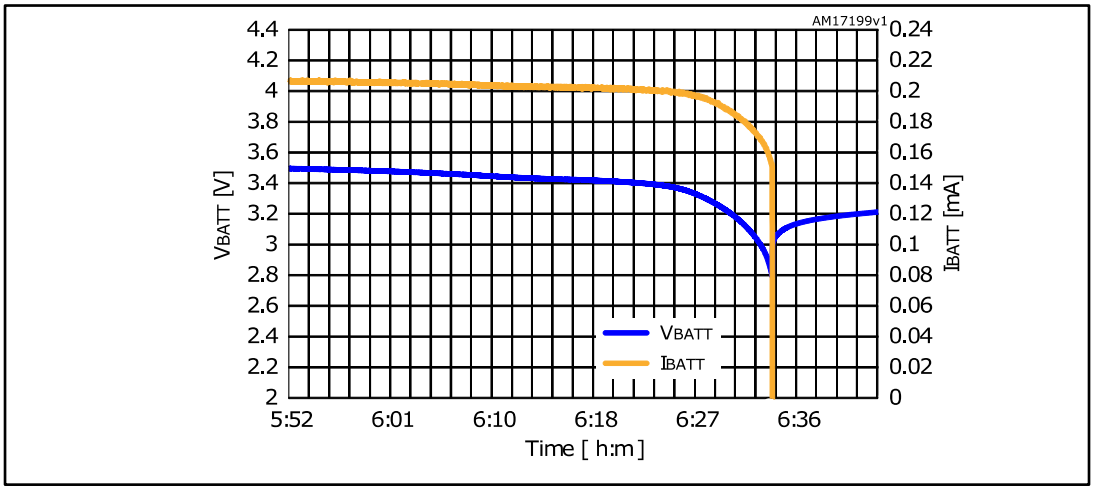
7.4 Battery overcharge protection

The battery overcharge protection is a safety feature, active when a valid input voltage is connected, preventing the battery voltage from exceeding a V_{OCHG} value. Should an overcharge condition be detected, the current path from the input to the battery is blocked and a fault signal is activated (the CHG pin toggles at 8.2 Hz). When the battery voltage goes below V_{OCHG}, normal operations can only be restarted by disconnecting and connecting back again the input voltage (V_{IN}).

7.5 Battery over-discharge protection

When there is no valid input voltage and the device is running on battery power, the battery voltage is monitored to avoid over-discharge. If the battery voltage falls below V_{ODC} for more than t_{ODD}, the device is turned off and battery drain is reduced to less than 500 nA. This condition is called the over-discharge state. When a valid input voltage is connected while in the over-discharge state, the charger and the LDO are activated. If the input voltage is then disconnected, normal operation is restored only if the battery voltage has increased above the over-discharge release threshold (V_{ODCR}), otherwise the STNS01 remains in the battery over-discharge state.

Figure 21: Discharging cycle profile



7.6 Battery discharge overcurrent protection

When the STNS01 is powered from the BAT pin, a discharge overcurrent protection circuit disables the device if the battery current exceeds I_{BATOCP} for more than t_{DOD}. A valid input voltage (VIN) must be connected to restore normal operating conditions.

7.7 Input overcurrent protection

When the STNS01 is powered from the IN pin, a current limitation circuit prevents the input current from increasing up to potentially destructive values. When V_{SYS} is lower than $V_{ILIMSCTH}$, the input current is limited to $I_{INLIMSC}$ in order to have reduced power dissipation in short-circuit conditions. As soon as V_{SYS} increases over $V_{ILIMSCTH}$, the current limitation value is increased to I_{INLIM}.

7.8 SYS and LDO short-circuit protection

In case of an abrupt short-circuit on SYS or LDO, the STNS01 is immediately turned off (no deglitch). This short-circuit protection intervenes when the SYS voltage drops below V_{SCSYS} or the LDO output voltage drops below V_{SCLDO}.

7.9 IN overvoltage protection

The STNS01 is normally powered from the battery when $V_{IN} > V_{INOVP}$ while it is powered from the IN pin when $V_{UVLO} < V_{IN} < V_{INOVP}$. In the latter case, if the input voltage temporarily increases over V_{INOVP} due to a poorly regulated power supply, the STNS01 switches to battery power to protect any external circuit connected to SYS. If the input voltage (VIN) returns into the normal range, the device's supply voltage is switched back to the IN pin.

7.10 Shutdown mode

A high level on the shutdown digital input pin (SD) when no valid input voltage is connected makes the device enter shutdown (low power) mode. Battery drain is then reduced to less than 500 nA. The exit conditions for the shutdown mode are the same as for the over-discharge state (valid VIN connected and $V_{BAT} > V_{ODCR}$).

7.11 Thermal shutdown

The STNS01 is protected against overheating which might be generated by the combination of ambient temperature and internal heating due to power dissipation. When the die temperature exceeds T_{SD} the device is turned off. In order to restore normal operation the input voltage (V_{IN}) must be disconnected and reconnected.

7.12 Reverse current protection

In order to prevent undesired battery discharge, when the input voltage (V_{IN}) is lower than the battery voltage (V_{BAT}), the current path from BAT to IN is blocked.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 DFN12L (3x3x0.75 mm) package information

Figure 22: DFN12L (3x3x0.75 mm) package outline

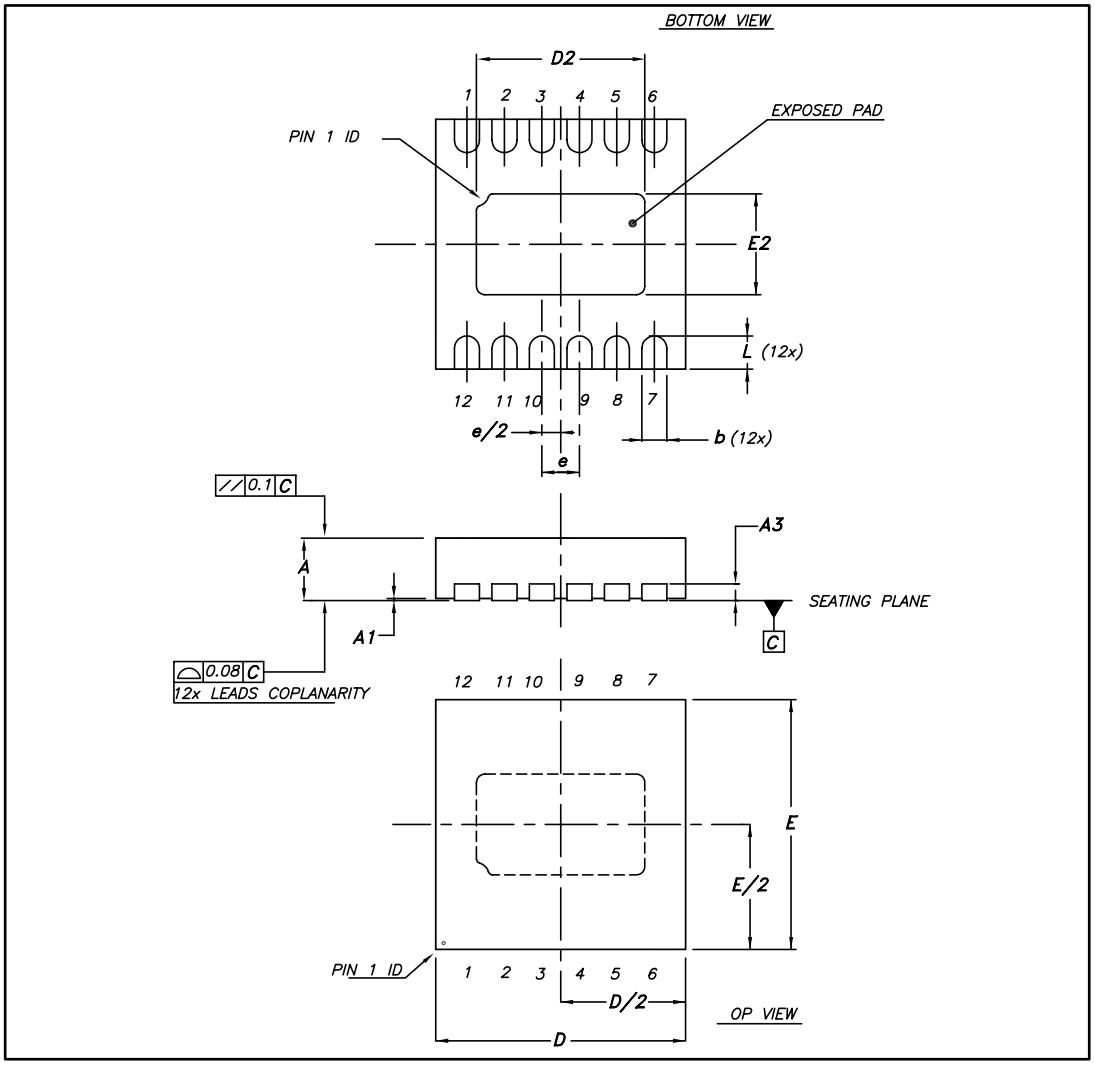
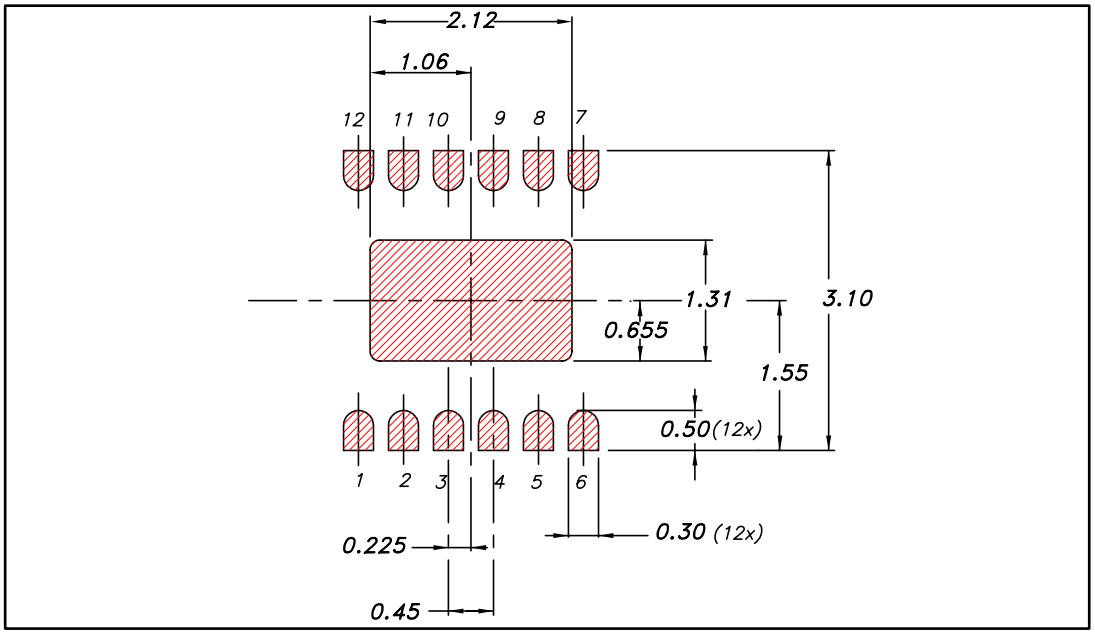


Table 9: DFN12L (3x3x0.75 mm) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3	3.15
D2	1.87	2.02	2.12
E	2.85	3	3.15
E2	1.06	1.21	1.31
e		0.45	
L	0.30	0.40	0.50

Figure 23: DFN12L (3x3x0.75 mm) recommended footprint



8.2 DFN12L (3x3x0.75 mm) packing information

Figure 24: Tape outline

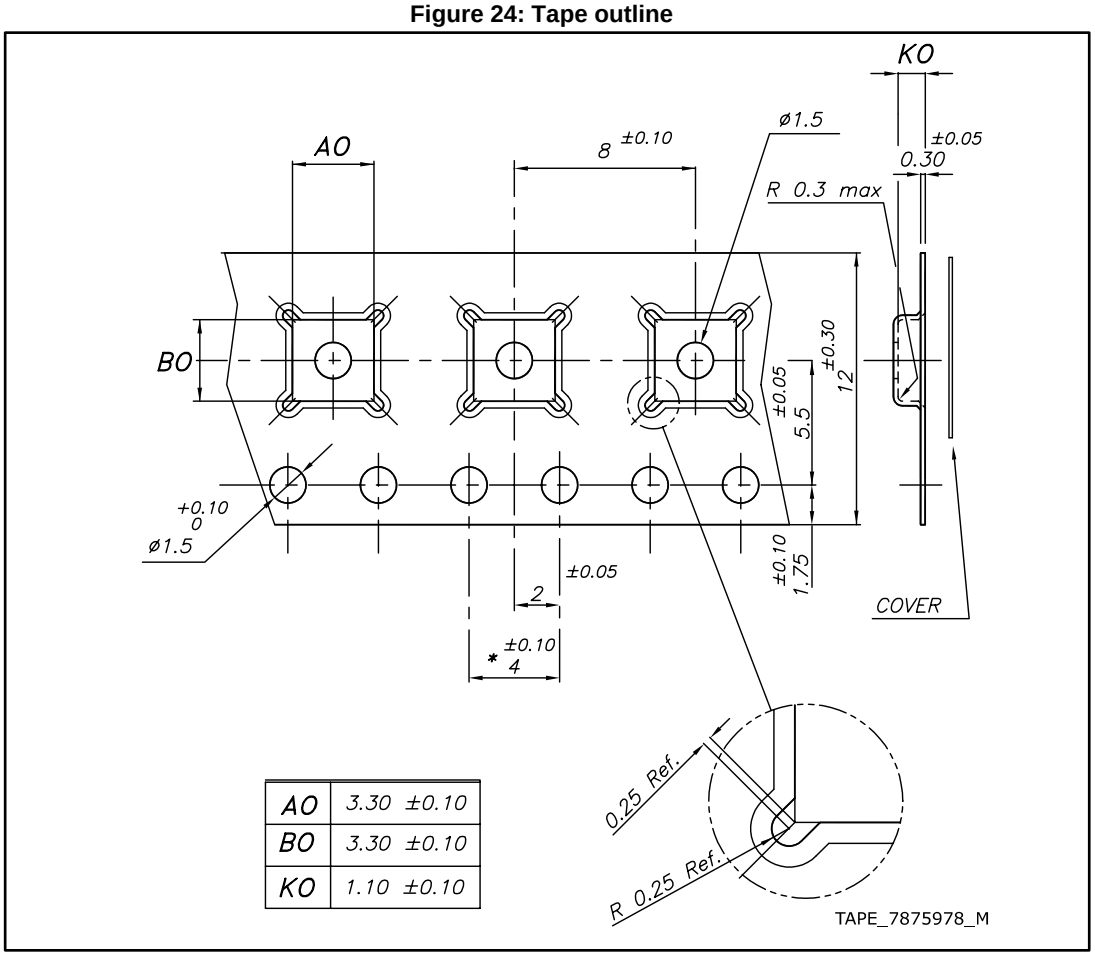
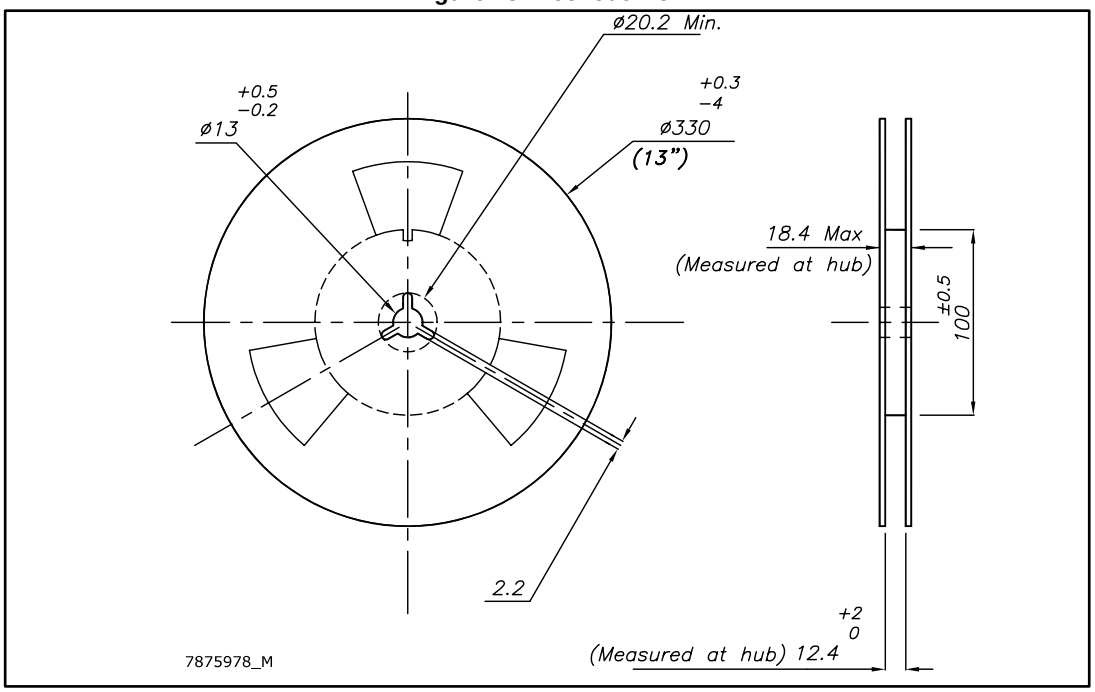


Figure 25: Reel outline



9 Revision history

Table 10: Document revision history

Date	Revision	Changes
17-May-2013	1	Initial release.
15-Jul-2013	2	Updated *Table 6: Electrical characteristics.*
11-May-2017	3	Updated section 5: "Electrical characteristics".
14-Dec-2017	4	Updated *Table 5: "Thermal data"* and *Table 6: "Electrical characteristics"*.

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