



SRAM
AS8S128K32

128K x 32 SRAM
SRAM MEMORY ARRAY

**AVAILABLE AS MILITARY
SPECIFICATIONS**

- SMD 5962-95595: -Q
- SMD 5962-93187: -P or -PN
- MIL-STD-883

FEATURES

- Access times of 15, 17, 20, 25, 35, and 45 ns
- Built in decoupling caps for low noise operation
- Organized as 128K x32; User configured as 256Kx16 or 512K x8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs
- 2V Data Retention, Low power standby

OPTIONS

- Timing
 - 15ns
 - 17ns
 - 20ns
 - 25ns
 - 35ns
 - 45ns

MARKINGS

-15
-17
-20
-25
-35
-45

Q No. 702
P No. 802
PN No. 802

NOTE: PN indicates a no connect on pins 8, 21, 28, 39

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8S128K32 is a 4 Mega-bit CMOS SRAM Module organized as 128Kx32-bits and user configurable to 256Kx16 or 512Kx8. The AS8S128K32 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military temperature grade product is suited for military applications.

The AS8S128K32 is offered in a ceramic quad flatpack module per SMD-5962-95595 with a maximum height of 0.140 inches. This module makes use of a low profile, mutlichip module design.

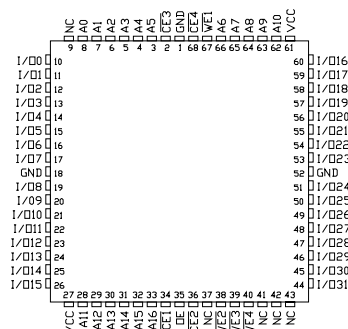
This device is also offered in a 1.075 inch square ceramic pin grid array per SMD 5692-93187, which has a maximum height of 0.195 inches. This package is also a low profile, multi-chip module design reducing height requirements to a minimum.

For more products and information
please visit our web site at
www.austinsemiconductor.com

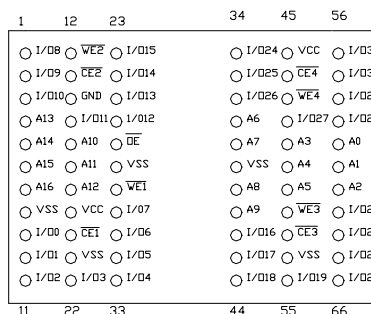
PIN ASSIGNMENT

(Top View)

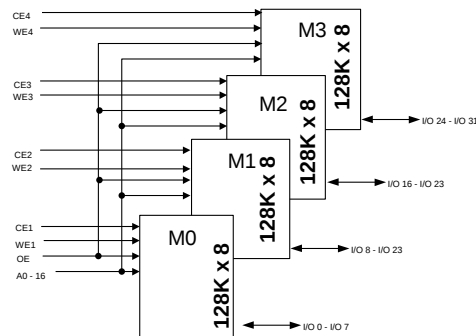
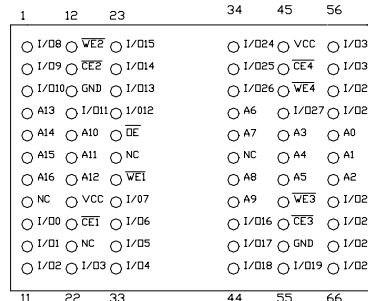
68 Lead CQFP (Q)



66 Lead PGA- Pins 8, 21, 28, 39 are grounds (P)



66 Lead PGA- Pins 8, 21, 28, 39 are no connects (PN)





Austin Semiconductor, Inc.

SRAM

AS8S128K32

ABSOLUTE MAXIMUM RATINGS*

Voltage of V_{CC} Supply Relative to V_{SS}.....-1V to +7V
 Storage Temperature.....-65°C to +150°C
 Short Circuit Output Current(per I/O).....20mA
 Voltage on Any Pin Relative to V_{SS}.....-5V to V_{CC}+1V
 Maximum Junction Temperature**.....+175°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +0.5	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
INPUT LEAKAGE CURRENT ADD, OE	0V < V _{IN} < V _{CC}	I _{L1}	-10	-10	μA	
INPUT LEAKAGE CURRENT WE, CE	0V < V _{IN} < V _{CC}	I _{L2}	-5	5	μA	
OUTPUT LEAKAGE CURRENT I/O	Outputs(s) Disabled 0V < V _{OUT} < V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4	--	V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}	--	0.4	V	1
Supply Voltage		V _{CC}	4.5	5.5	V	1

PARAMETER	CONDITIONS	SYM	MAX						UNITS	NOTES
			-15	-17	-20	-25	-35	-45		
Power Supply Current: Operating	CE ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/t _{RC} (MIN) Outputs Open	I _{CC}	700	650	600	560	520	500	mA	3, 13 ⁽¹⁾
Power Supply Current: Standby	CE ≥ V _{IH} ; V _{CC} = MAX f = MAX = 1/t _{RC} (MIN) Outputs Open	I _{SBT1}	280	220	200	180	160	150	mA	(1)
	CE = OE = V _{IH} ; CMOS Compatible; V _{CC} = MAX f = 5 MHz	I _{SBT2}	100	80	80	60	60	60	mA	(1)
	CE ≥ V _{CC} -0.2V; V _{CC} = MAX V _{IL} ≤ V _{SS} +0.2V; V _{IH} ≥ V _{CC} -0.2V; f = 0 Hz	I _{SBC1}	40	40	40	40	40	40	mA	(2)
	CE > V _{CC} -0.2V; V _{CC} = MAX V _{IL} < V _{SS} +0.2V; V _{IH} > V _{CC} -0.2V; f = 0 Hz "L" Version Only	I _{SBC2}	24	24	24	24	24	24	mA	(2)

NOTE: 1) Address switching sequence A, A+1, A+2, etc.

2) 1/2 input at HIGH, 1/2 input at LOW.



CAPACITANCE TABLE ($V_{IN} = 0V$, $f = 1\text{ MHz}$, $T_A = 25^\circ C$)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_{ADD}	A0 - A18 Capacitance	40	pF	4
C_{OE}	OE\ Capacitance	40	pF	4
C_{WE}, C_{CE}	WE\ and CE\ Capacitance	20	pF	4
C_{IO}	I/O 0- I/O 31 Capacitance	20	pF	4

TRUTH TABLE					
MODE	OE\	CE\	WE\	I/O	POWER
Read	L	L	H	Q	ACTIVE
Write	X	L	L	D	ACTIVE
Standby	X	H	X	HIGH Z	STANDBY
Not Selected	H	L	H	HIGH Z	ACTIVE

ACTEST CONDITIONS

TEST SPECIFICATIONS

Input pulse levels.....VSS to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figures 1

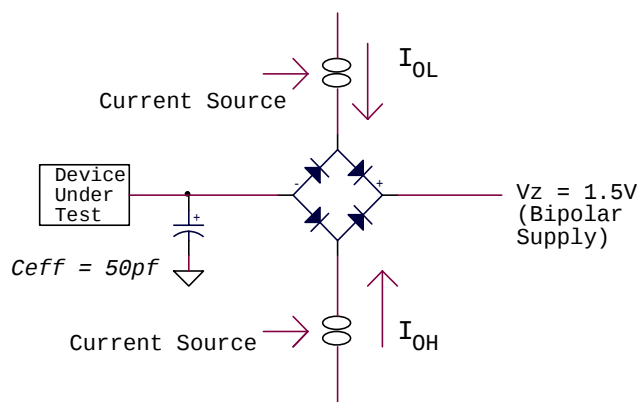


Figure 1

NOTES:

V_z is programable from -2V to +7V.
 I_{OL} and I_{OH} programmable from 0 to 16 mA.
 V_z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.



Austin Semiconductor, Inc.

SRAM

AS8S128K32

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ TA ≤ 125°C; Vcc = 5v ± 10%)

DESCRIPTION		-15		-17		-20		-25		-35		-45			
	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ CYCLE															
READ cycle time	^t RC	15		17		20		25		35		45		ns	
Address access time	^t AA		15		17		20		25		35		45	ns	
Chip enable access time	^t ACE		15		17		20		25		35		45	ns	
Output hold from address change	^t OH	2		2		2		2		2		2		ns	
Chip enable to output in Low-Z	^t LZCE	2		2		2		2		2		2		ns	4, 6, 7
Chip disable to output in High-Z	^t HZCE		7		8		9		10		14		15	ns	4, 6, 7
Chip enable to power-up time	^t PU	0		0		0		0		0		0			4
Chip disable to power-down time	^t PD		15		17		20		25		35		45		4
Output enable access time	^t AOE		6		7		7		8		12		12	ns	
Output enable to output in Low-Z	^t LZOE	0		0		0		0		0		0		ns	4, 6
Output disable to output in High-Z	^t HZOE		6		7		7		9		12		12	ns	4, 6, 7
WRITE CYCLE															
WRITE cycle time	^t WC	15		17		20		25		35		45		ns	
Chip enable to end of write	^t CW	12		12		15		17		20		22		ns	
Address valid to end of write	^t AW	12		12		15		17		20		22		ns	
Address setup time	^t AS	0		0		0		0		0		0		ns	
Address hold from end of write	^t AH	1		1		1		1		1		1		ns	
WRITE pulse width	^t WP1	12 ¹		12 ¹		15		17		20		20		ns	
WRITE pulse width	^t WP2	12 ¹		12 ¹		15		17		20		20		ns	
Data setup time	^t DS	8		9		10		12		15		15		ns	
Data hold time	^t DH	1		1		1		1		1		1		ns	
Write disable to output in Low-z	^t LZWE	2		2		2		2		2		2		ns	4, 6, 7
Write enable to output in High-Z	^t HZWE		7		9		10		11		14		15	ns	4, 6, 7

NOTES:

1) For OE\ = HIGH condition. For OE\ = LOW condition t_{WP1} = t_{WP2} = 15 ns MIN.

**NOTES**

1. All voltages referenced to V_{SS} (GND).
2. -3v for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates.
The specified value applies with the outputs

$$\text{open, and } f = \frac{1}{t_{RC}(\text{MIN})} \text{ Hz.}$$

4. This parameter is sampled.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE} , t_{HZOE} and t_{HZWE} are specified with $C_L = 5\text{pF}$ as in Fig. 2. Transition is measured +/- 200 mV typical from steady state coltage, allowing for actual tester RC time constant.

7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} .

8. $\overline{WE}$ is HIGH for READ cycle.

9. Device is continuously selected. Chip enables and output enable are held in their active state.

10. Address valid prior to or coincident with latest occurring chip enable.

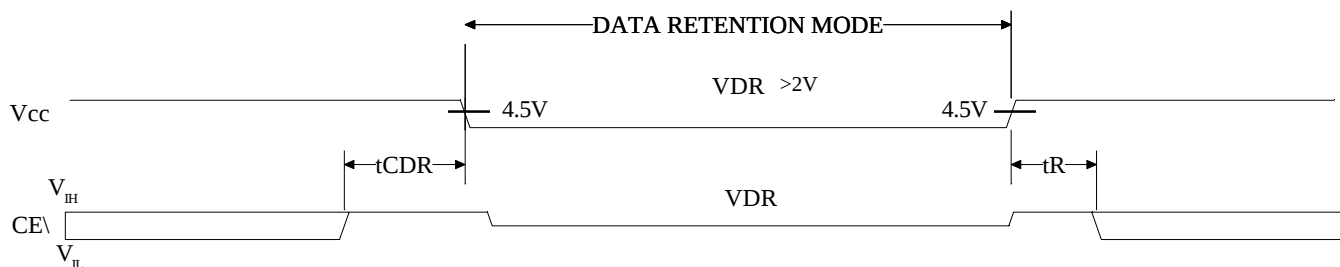
11. t_{RC} = READ cycle time.

12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.

13. 32 bit operation

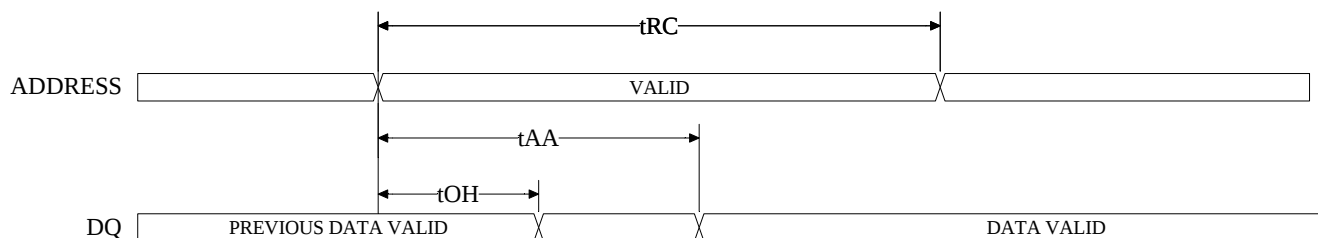
DATA RETENTION ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2	--	V	
Data Retention Current	$CE \geq V_{CC} - 0.2V$	$V_{CC} = 2.0V$	I_{CCDR}	--	6	mA	
	$V_{IN} \geq V_{CC} - 0.2V$	$V_{CC} = 3V$	I_{CCDR}	--	11.6	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0	--	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

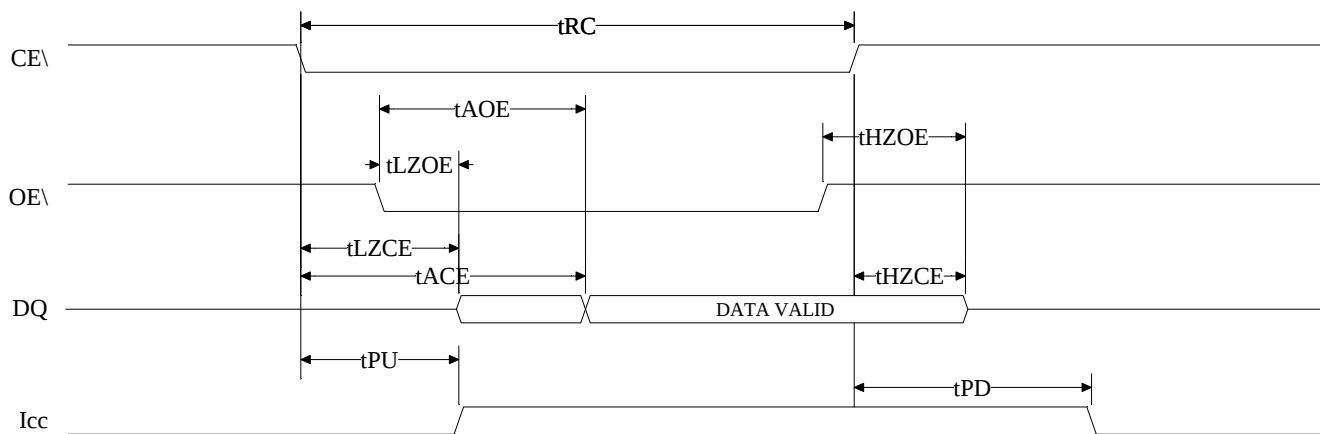
LOW V_{CC} DATA RETENTION WAVEFORM



READ CYCLE NO. 1^(8,9)



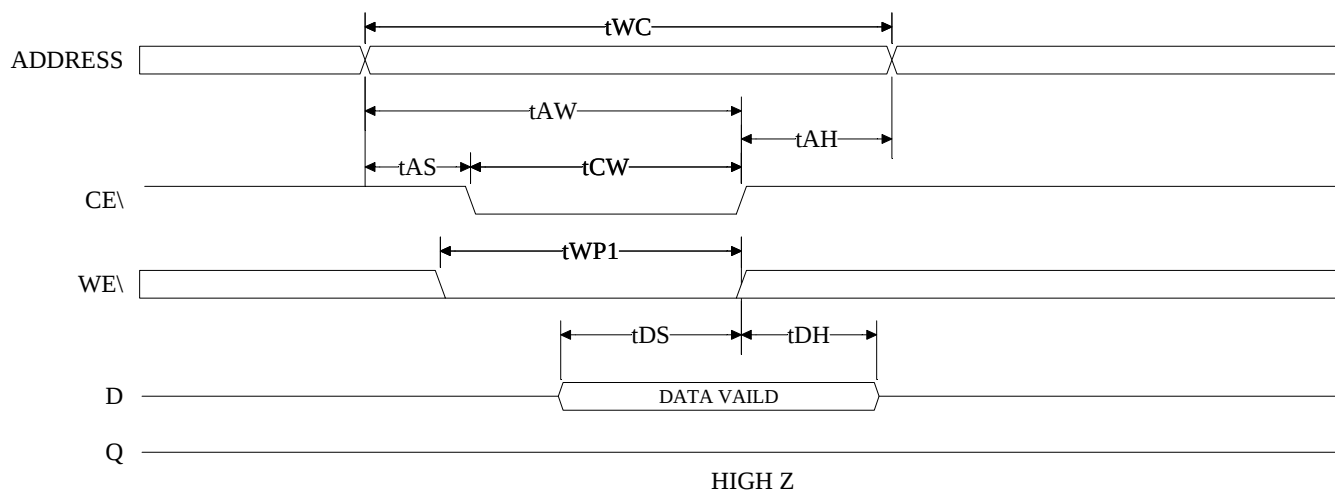
READ CYCLE NO. 2^(7,8,10)





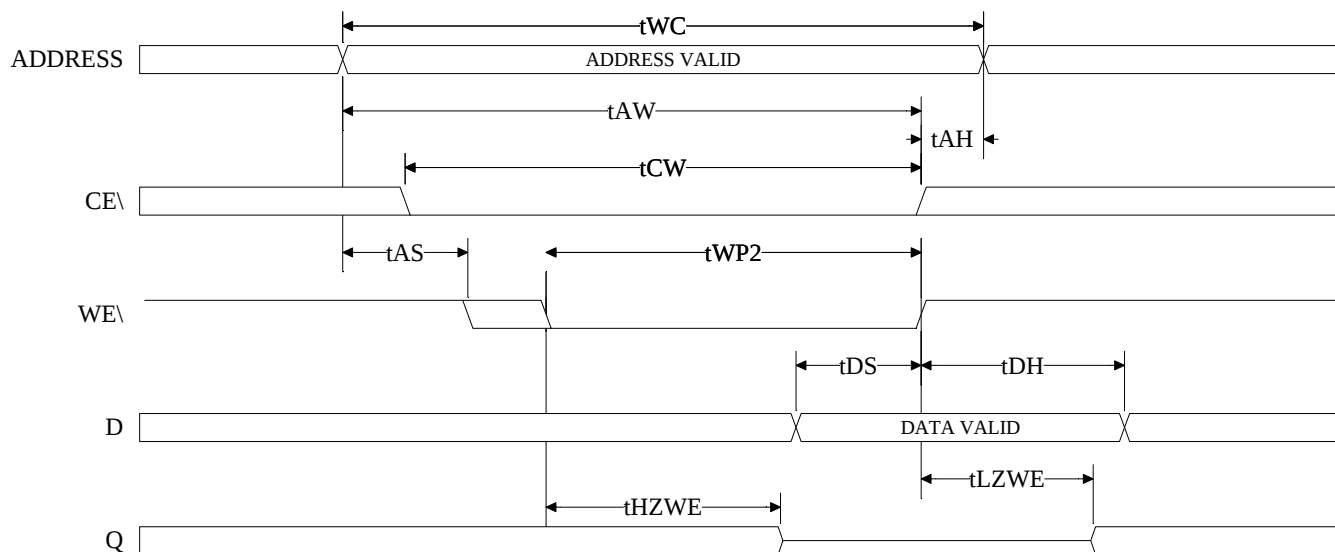
WRITE CYCLE NO. 1

(Chip Enable Controlled)



WRITE CYCLE NO. 2

(Write Enable Controlled)



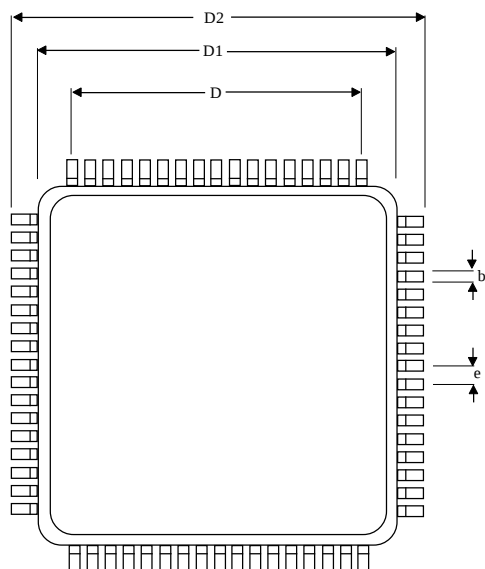


Austin Semiconductor, Inc.

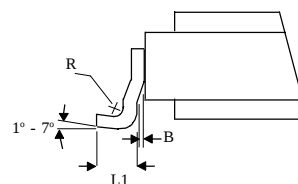
SRAM
AS8S128K32

MECHANICAL DEFINITIONS*

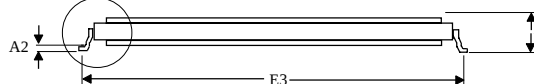
ASI Case #702 (Package Designator Q)
SMD 5962-95595, Case Outline M



DETAIL A



SEE DETAIL A



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.005	0.015
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.010 TYP	
L1	0.035	0.045

*All measurements are in inches.

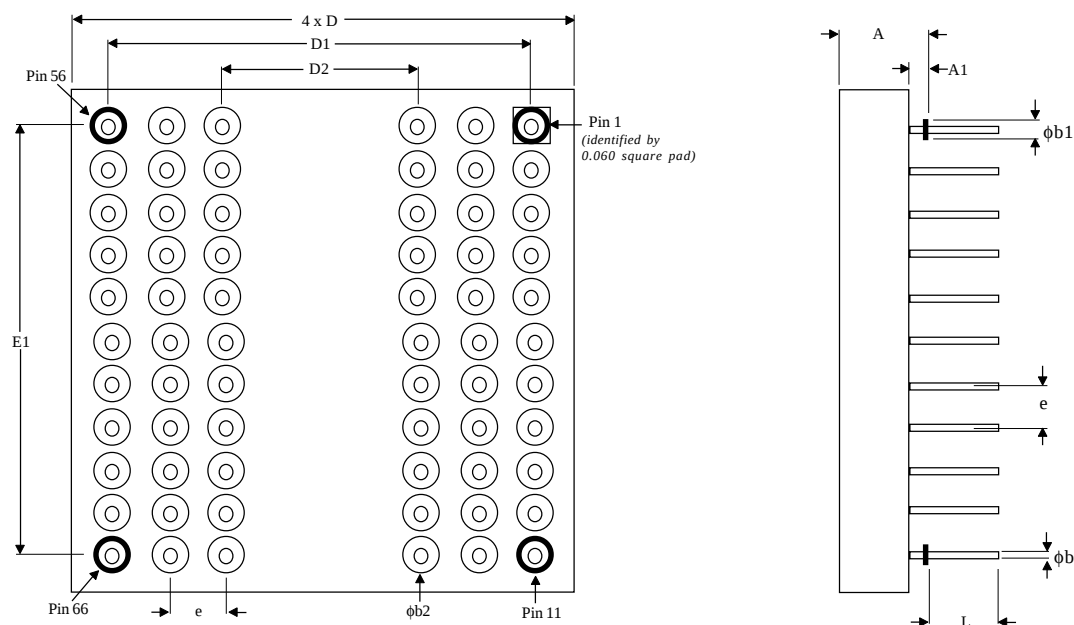


Austin Semiconductor, Inc.

SRAM
AS8S128K32

MECHANICAL DEFINITIONS*

ASI Case #904 (Package Designator P & PN)
SMD 5962-93187, Case Outline 4 and 5



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.135	0.195
A1	0.025	0.035
ϕb	0.016	0.020
$\phi b1$	0.045	0.055
$\phi b2$	0.065	0.075
D	1.064	1.086
D1/E1	1.000 BSC	
D2	0.600 BSC	
e	0.100 BSC	
L	0.145	0.155

*All measurements are in inches.



Austin Semiconductor, Inc.

SRAM
AS8S128K32

ORDERING INFORMATION

EXAMPLE: AS8S128K32Q-25/XT

Device Number	Package Type	Speed ns	Process
AS8S128K32	Q	-15	/*
AS8S128K32	Q	-17	/*
AS8S128K32	Q	-20	/*
AS8S128K32	Q	-25	/*
AS8S128K32	Q	-35	/*
AS8S128K32	Q	-45	/*

EXAMPLE: AS8S128K32PN-20/883C

Device Number	Package Type	Speed ns	Process
AS8S128K32	P	-15	/*
AS8S128K32	PN	-15	/*
AS8S128K32	P	-17	/*
AS8S128K32	PN	-17	/*
AS8S128K32	P	-20	/*
AS8S128K32	PN	-20	/*
AS8S128K32	P	-25	/*
AS8S128K32	PN	-25	/*
AS8S128K32	P	-35	/*
AS8S128K32	PN	-35	/*
AS8S128K32	P	-45	/*
AS8S128K32	PN	-45	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range

XT = Extended Temperature Range

883C = Full Military Processing

-40°C to +85°C

-55°C to +125°C

-55°C to +125°C

PACKAGE NOTES

P = Pins 8, 21, 28, and 39 are grounds.

PN = Pins 8, 21, 28, and 39 are no connects.



ASI TO DSCC PART NUMBER CROSS REFERENCE

ASI Package Designator Q

<u>ASI Part #</u>	<u>SMD Part #</u>
AS8S128K32Q-55/883C	5962-9559505HMA
AS8S128K32Q-55/883C	5962-9559505HMC
AS8S128K32Q-45/883C	5962-9559506HMA
AS8S128K32Q-45/883C	5962-9559506HMC
AS8S128K32Q-35/883C	5962-9559507HMA
AS8S128K32Q-35/883C	5962-9559507HMC
AS8S128K32Q-25/883C	5962-9559508HMA
AS8S128K32Q-25/883C	5962-9559508HMC
AS8S128K32Q-20/883C	5962-9559509HMA
AS8S128K32Q-20/883C	5962-9559509HMC
AS8S128K32Q-17/883C	5962-9559510HMA
AS8S128K32Q-17/883C	5962-9559510HMC

ASI Package Designator P & PN

<u>ASI Part #</u>	<u>SMD Part #</u>	<u>ASI Part #</u>	<u>SMD Part #</u>
AS8S128K32P-55/883C	5962-9318705H5A	AS8S128K32PN-55/883C	5962-9318705H4A
AS8S128K32P-55/883C	5962-9318705H5C	AS8S128K32PN-55/883C	5962-9318705H4C
AS8S128K32P-45/883C	5962-9318706H5A	AS8S128K32PN-45/883C	5962-9318706H4A
AS8S128K32P-45/883C	5962-9318706H5C	AS8S128K32PN-45/883C	5962-9318706H4C
AS8S128K32P-35/883C	5962-9318707H5A	AS8S128K32PN-35/883C	5962-9318707H4A
AS8S128K32P-35/883C	5962-9318707H5C	AS8S128K32PN-35/883C	5962-9318707H4C
AS8S128K32P-25/883C	5962-9318708H5A	AS8S128K32PN-25/883C	5962-9318708H4A
AS8S128K32P-25/883C	5962-9318708H5C	AS8S128K32PN-25/883C	5962-9318708H4C
AS8S128K32P-20/883C	5962-9318709H5A	AS8S128K32PN-20/883C	5962-9318709H4A
AS8S128K32P-20/883C	5962-9318709H5C	AS8S128K32PN-20/883C	5962-9318709H4C
AS8S128K32P-17/883C	5962-9318710H5A	AS8S128K32PN-17/883C	5962-9318710H4A
AS8S128K32P-17/883C	5962-9318710H5C	AS8S128K32PN-17/883C	5962-9318710H4C

Please note, -15 not currently available on the SMD's.