MAC08BT1, MAC08MT1

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed for use in solid state relays, MPU interface, TTL logic and other light industrial or consumer applications. Supplied in surface mount package for use in automated manufacturing.

Features

- Sensitive Gate Trigger Current in Four Trigger Modes
- Blocking Voltage to 600 Volts
- Glass Passivated Surface for Reliability and Uniformity
- Surface Mount Package
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (Sine Wave, 50 to 60 Hz, Gate Open, T_J = 25 to 110°C) MAC08BT1 MAC08MT1	V_{DRM}, V_{RRM}	200 600	V
On−State Current RMS (T_C = 80°C) (Full Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	0.8	A
Peak Non−repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_C = 25°C)	I_{TSM}	8.0	A
Circuit Fusing Considerations (Pulse Width = 8.3 ms)	I^2t	0.4	A^2s
Peak Gate Power (T_C = 80°C, Pulse Width ≤ 1.0 μs)	P_{GM}	5.0	W
Average Gate Power (T_C = 80°C, t = 8.3 ms)	$P_{G(AV)}$	0.1	W
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient PCB Mounted per Figure 1	$R_{\theta JA}$	156	°C/W
Thermal Resistance, Junction−to−Tab Measured on MT2 Tab Adjacent to Epoxy	$R_{\theta JT}$	25	°C/W
Maximum Device Temperature for Soldering Purposes for 10 Secs Maximum	T_L	260	°C

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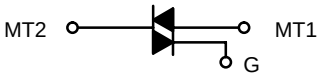
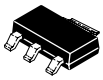
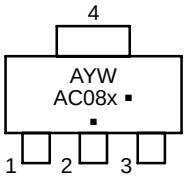
TRIAC
0.8 AMPERE RMS
200 thru 600 VOLTS



MARKING DIAGRAM



SOT−223
CASE 318E
STYLE 11



A = Assembly Location
Y = Year
W = Work Week
AC08X = Device Code
x= B or M
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping†
MAC08BT1	SOT−223	1000 Tape & Reel
MAC08BT1G	SOT−223 (Pb−Free)	1000 Tape & Reel
MAC08MT1	SOT−223	1000 Tape & Reel
MAC08MT1G	SOT−223 (Pb−Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

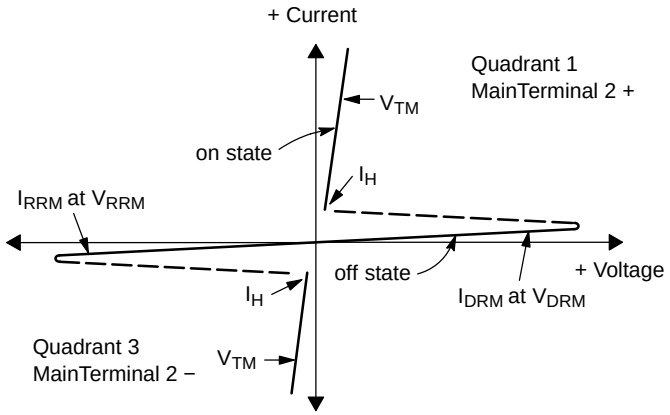
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open)	T_J = 25°C	I_{DRM}, I_{RRM}	−	−	10	μA
	T_J = 110°C		−	−	200	μA
ON CHARACTERISTICS						
Peak On−State Voltage (Note 2) (I_T = ±1.1 A Peak)		V_{TM}	−	−	1.9	V
Gate Trigger Current (Continuous dc) All Quadrants (V_D = 12 Vdc, R_L = 100 Ω)		I_{GT}	−	−	10	mA
Holding Current (Continuous dc) (V_D = 12 Vdc, Gate Open, Initiating Current = ±20 mA)		I_H	−	−	5.0	mA
Gate Trigger Voltage (Continuous dc) All Quadrants (V_D = 12 Vdc, R_L = 100 Ω)		V_{GT}	−	−	2.0	V
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Commutation Voltage (f = 250 Hz, I_{TM} = 1.0 A, Commutating di/dt = 1.5 A/mS On−State Current Duration = 2.0 mS, V_{DRM} = 200 V, Gate Unenergized, T_C = 110°C, Gate Source Resistance = 150 Ω, See Figure 10)		$(dv/dt)_c$	1.5	−	−	V/μs
Critical Rate−of−Rise of Off State Voltage (V_{pk} = Rated V_{DRM}, T_C= 110°C, Gate Open, Exponential Method)		dv/dt	10	−	−	V/μs

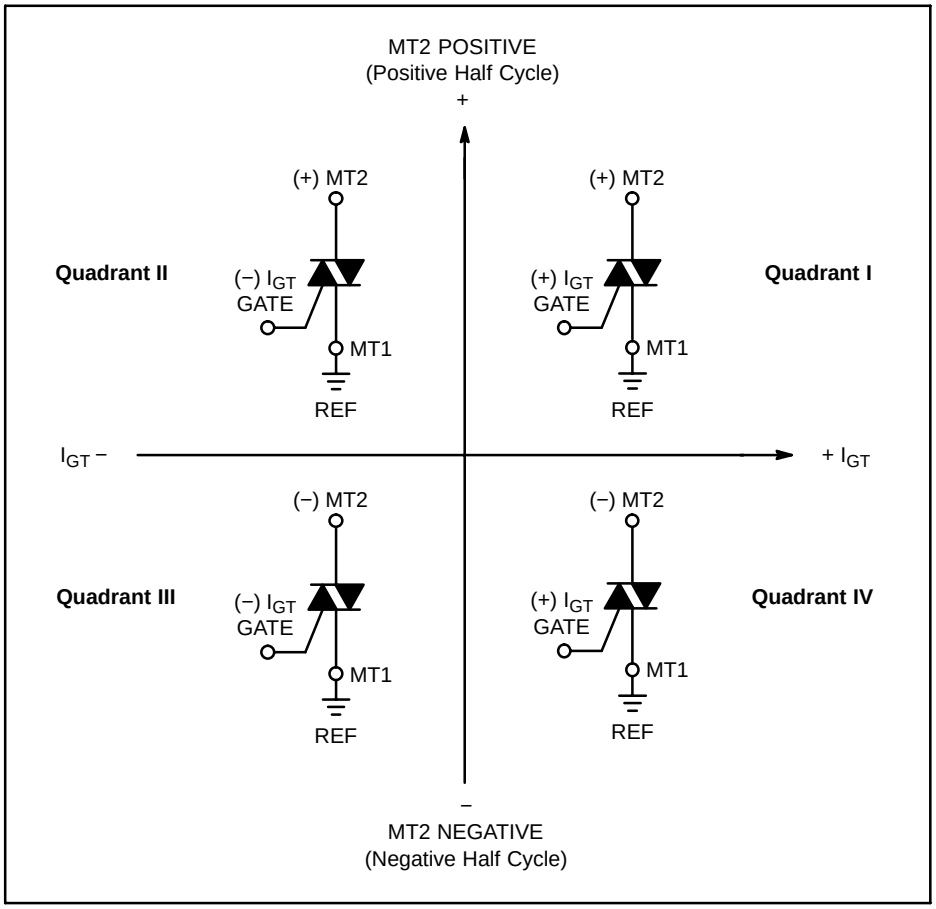
2. Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤2%.

Voltage Current Characteristic of Triacs (Bidirectional Device)

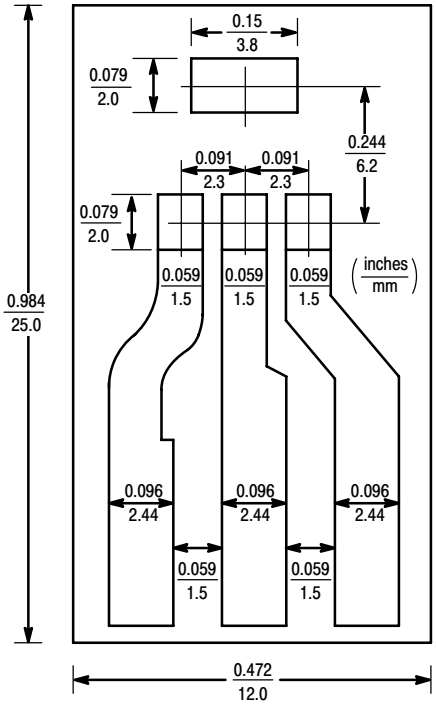
Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.



BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.
BOARD THICKNESS = 65 MIL., FOIL THICKNESS = 2.5 MIL.
MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

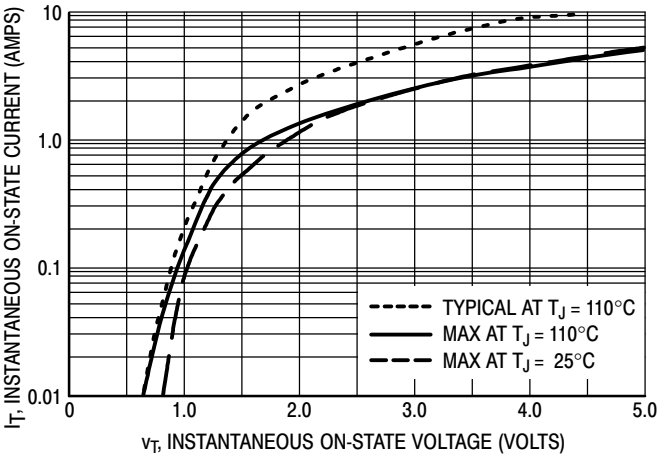


Figure 2. On-State Characteristics

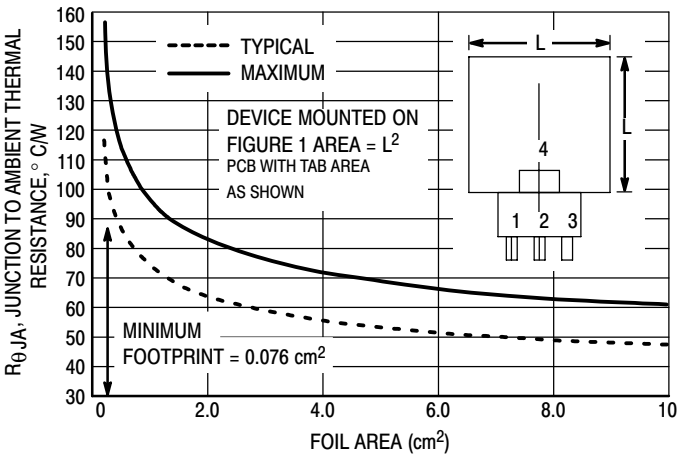


Figure 3. Junction to Ambient Thermal Resistance versus Copper Tab Area

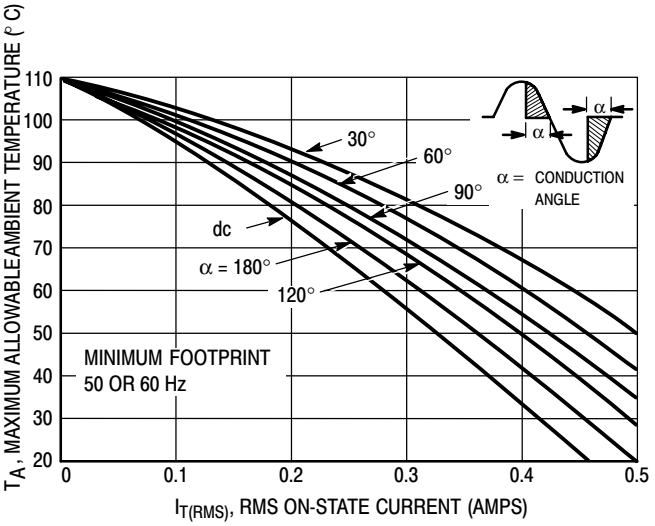


Figure 4. Current Derating, Minimum Pad Size Reference: Ambient Temperature

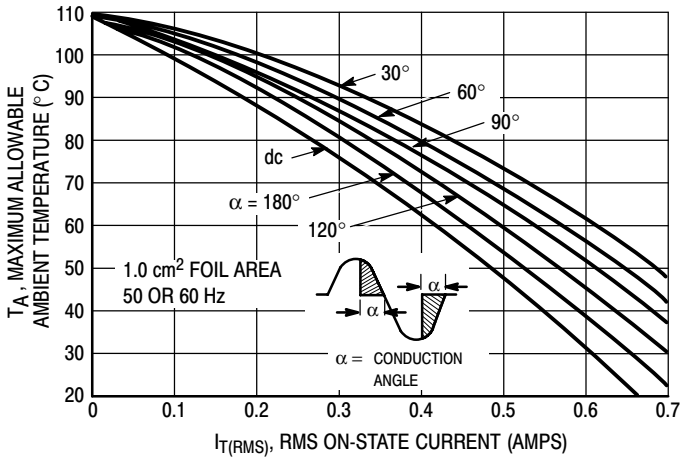


Figure 5. Current Derating, 1.0 cm Square Pad Reference: Ambient Temperature

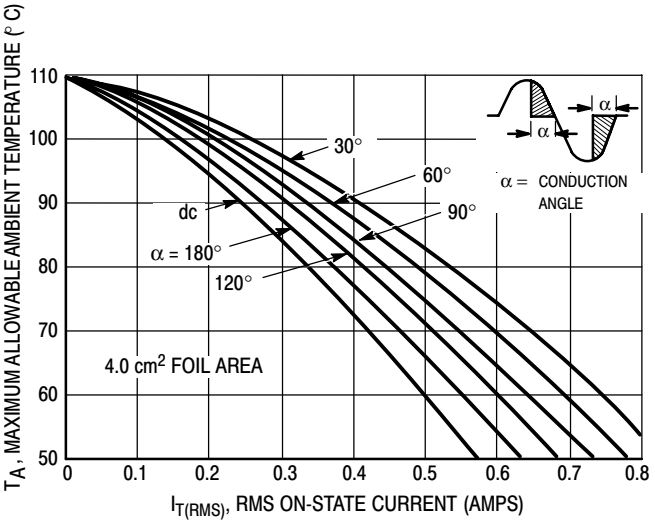


Figure 6. Current Derating, 2.0 cm Square Pad Reference: Ambient Temperature

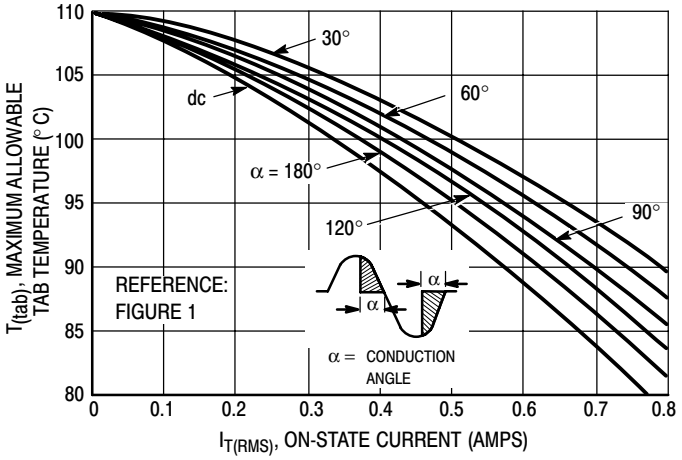


Figure 7. Current Derating Reference: MT2 Tab

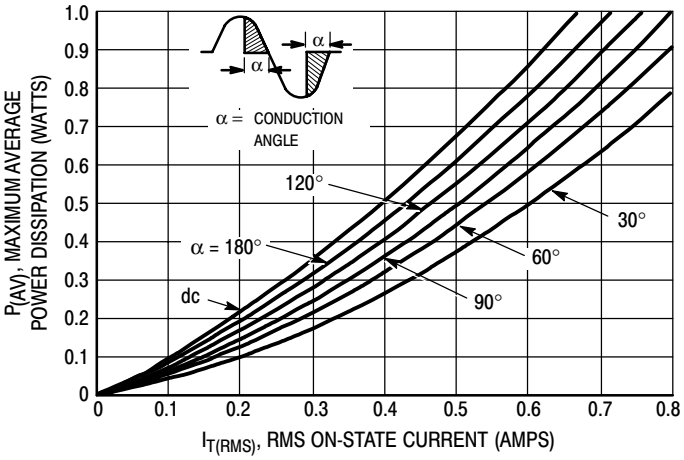


Figure 8. Power Dissipation

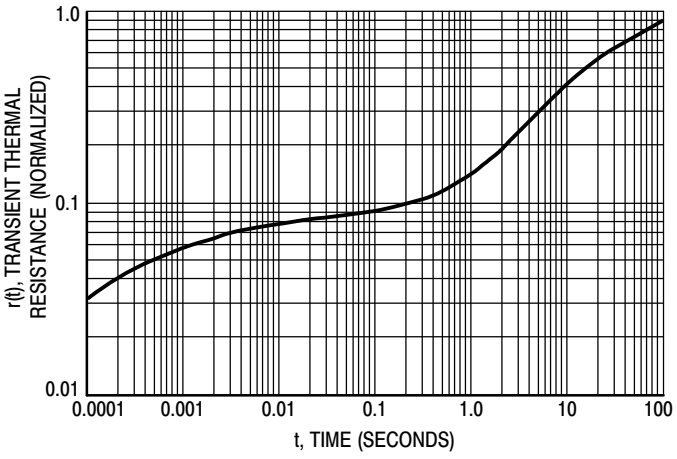
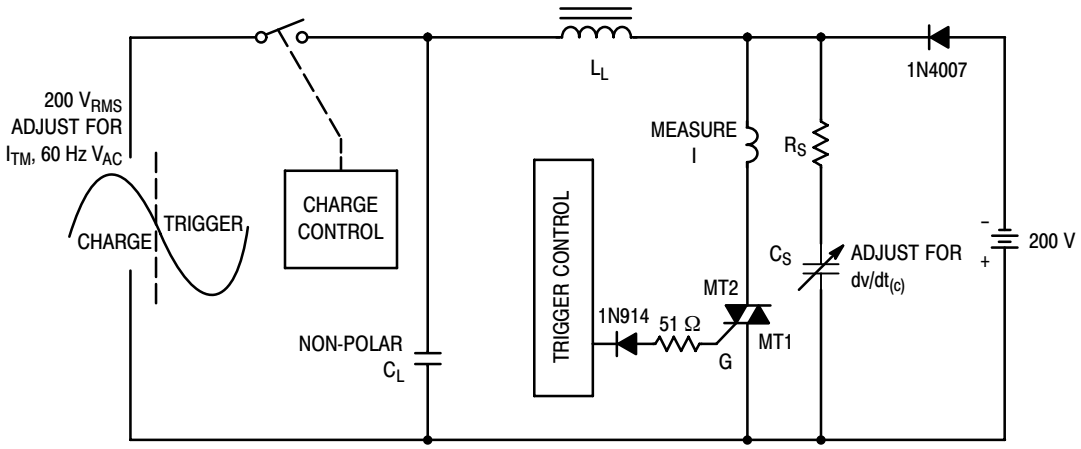


Figure 9. Thermal Response, Device Mounted on Figure 1 Printed Circuit Board



Note: Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 10. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage $(dv/dt)_c$

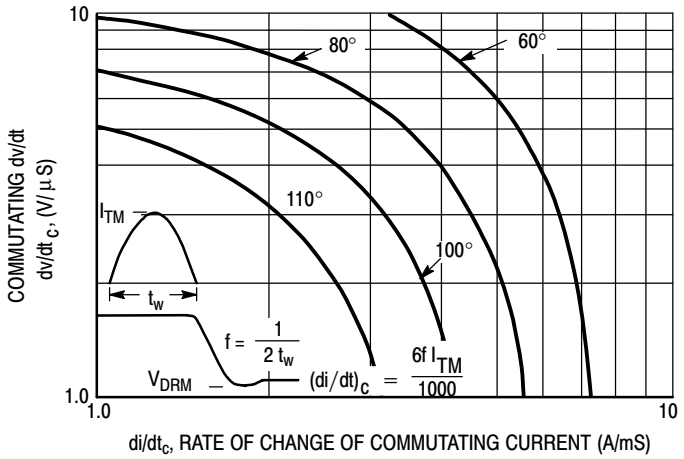


Figure 11. Typical Commutating dv/dt versus Current Crossing Rate and Junction Temperature

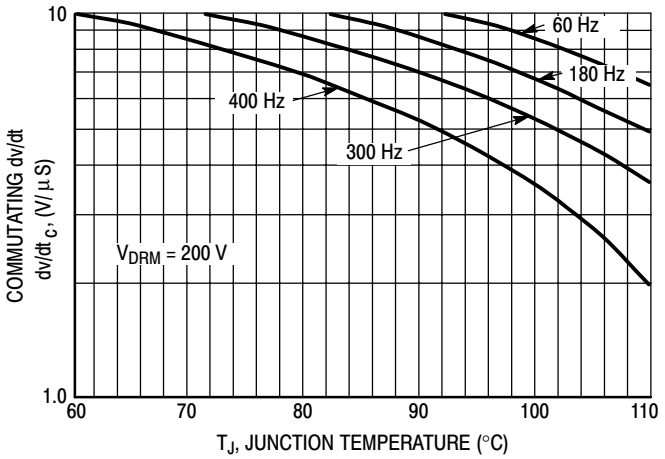


Figure 12. Typical Commutating dv/dt versus Junction Temperature at 0.8 Amps RMS

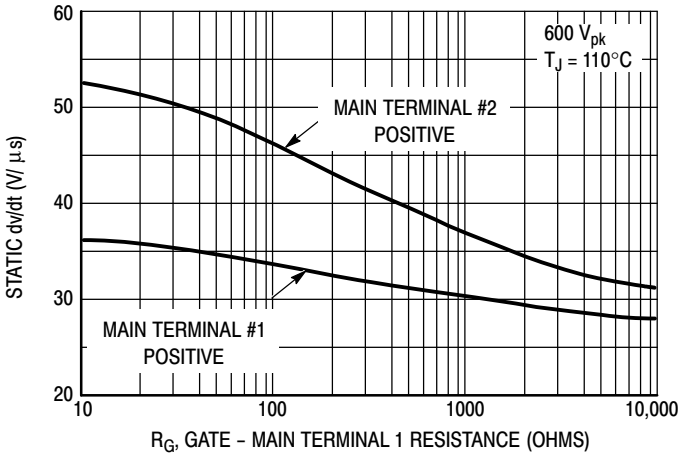


Figure 13. Exponential Static dv/dt versus Gate − Main Terminal 1 Resistance

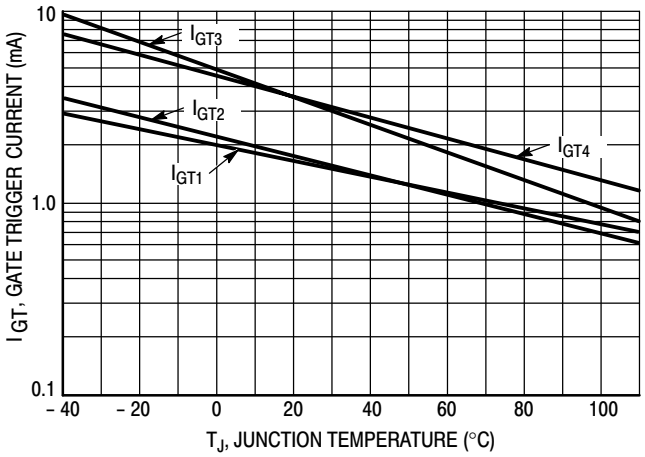


Figure 14. Typical Gate Trigger Current Variation

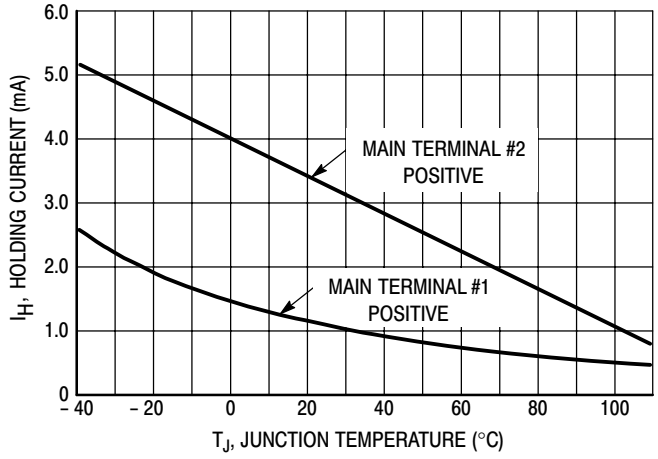


Figure 15. Typical Holding Current Variation

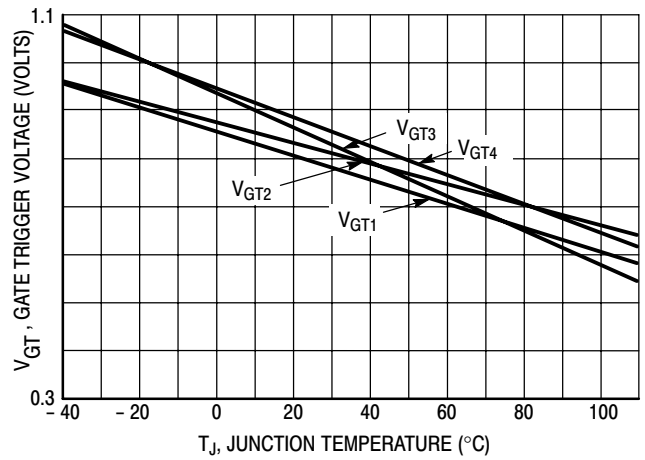
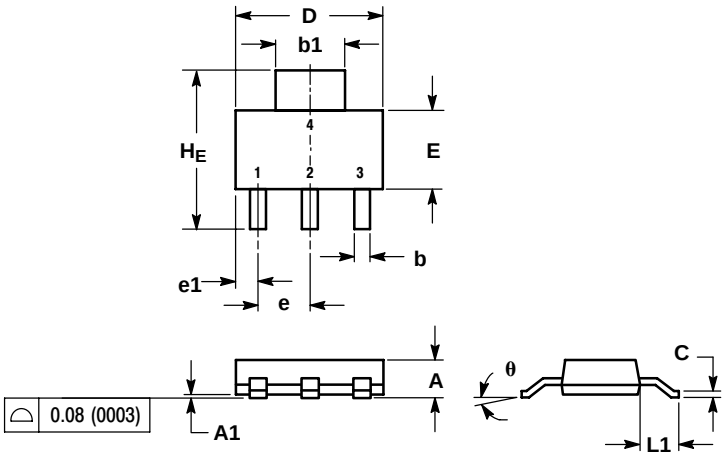


Figure 16. Gate Trigger Voltage Variation

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE L

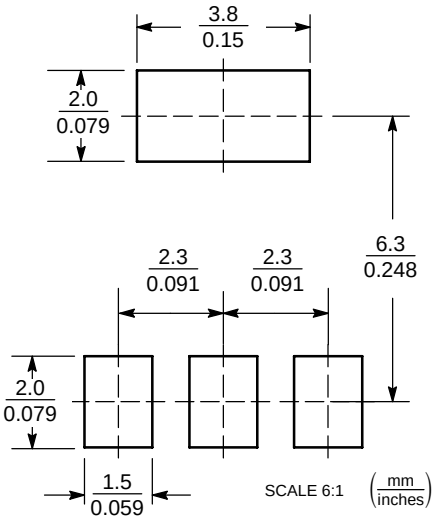


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
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Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Phone: 81−3−5773−3850

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