PRELIMINARY

Analog Signal Input Class D Amplifier for Piezo Speaker

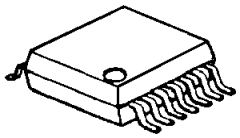
■ GENERAL DESCRIPTION

NJU8752 is a monaural analog signal input class D amplifier for Piezo speaker. The **NJU8752** includes Inversion operational amplifier input circuit, PWM modulator, Output short protector and a low voltage detector. Input part operates on 3.3V(TYP) as power supply and Output part operates up to 13.75V(MAX). Therefore, it drives Piezo speaker with Higher volume and High efficiency.

By using equivalent capacitance of Piezo speaker, the **NJU8752** is configured as a BTL amplifier capable of operating Piezo speaker with the minimum external components. A BTL configuration eliminates the need for external AC coupling capacitors.

Class D achieves high output-efficiency, which leads to low power operation for Piezo speaker, thus the **NJU8752** is ideally suited for battery powered applications.

■ PACKAGE OUTLINE

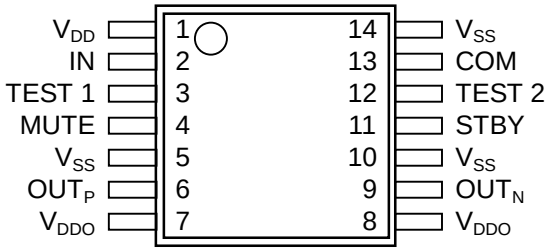


NJU8752V

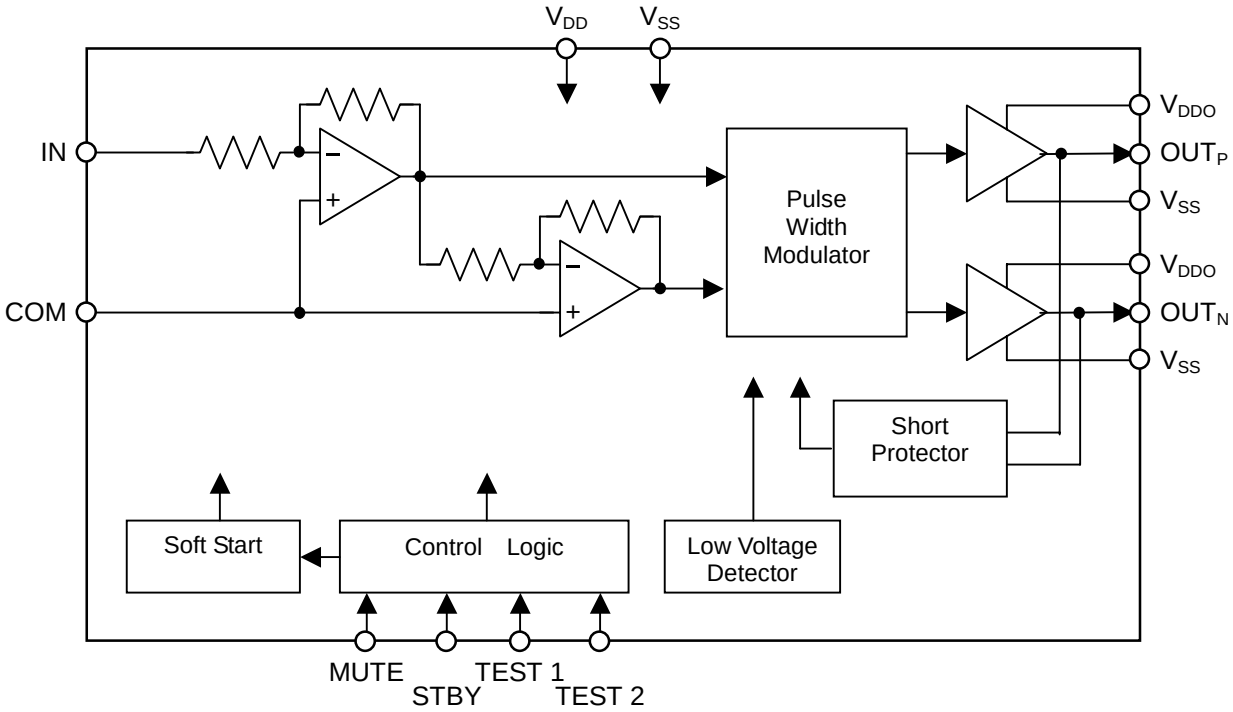
■ FEATURES

- Piezo Speaker Driving
- Analog Audio Signal Input, 1-channel BTL Output
- Standby(Hi-Z), Mute Control
- Built-in Low Voltage Detector
- Built-in Short Protector
- Operating Voltage 3.0 ~ 3.6V(Input)
  9.0 ~ 13.75V(Output)
- C-MOS Technology
- Package Outline SSOP14

■ PIN CONFIGURATION



■ BLOCK DIAGRAM

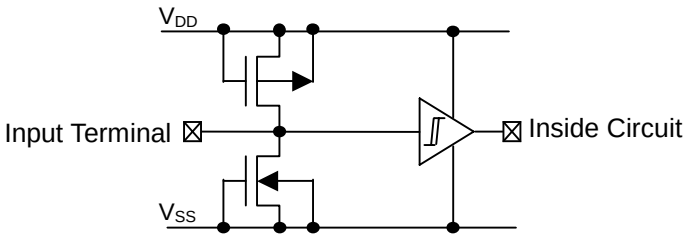


■ PIN DESCRIPTION

No.	SYMBOL	I/O	Function
1	V_{DD}	–	Power Supply: V_{DD}=3.3V
2	IN	I	Signal Input
3	TEST 1	I	Maker test 1 This pin must be connected to GND.
4	MUTE	I	Mute Control Low : Mute ON High : Mute OFF
5	V_{SS}	–	Positive Power GND : V_{SS}=0V
6	OUT_P	O	Positive Output
7	V_{DDO}	–	Positive Output Power Supply : V_{DDO}=5.0V~13.75V
8	V_{DDO}	–	Negative Output Power Supply : V_{DDO}=5.0V~13.75V
9	OUT_N	O	Negative Output
10	V_{SS}	–	Negative Power GND : V_{SS}=0V
11	STBY	I	Standby Control Low : Standby ON High : Standby OFF
12	TEST 2	I	Maker test 2 This pin must be connected to GND.
13	COM	I	Analog common
14	V_{SS}	–	Power GND : V_{SS}=0V

*Pin No. 5(V_{SS}),10(V_{SS}) and 14(V_{SS}) must be used at the same voltage level
*Pin No. 7(V_{DDO}) and 8(V_{DDO}) must be used at the same voltage level.

■ INPUT PINS STRUCTURE(MUTE, STBY, TEST1, TEST2)



■ FUNCTIONAL DESCRIPTION

(1) Output Signal

The OUT_P and OUT_N generate respectively L-channel and R-channel PWM output signals, which will be converted to analog signal via external 2nd-order or higher LC filter. A switching regulator with a high response against a voltage fluctuation is the best selection for the V_{DDP} and V_{DDN}, which are the power supply for output drivers. To obtain better T.H.D. performance, the stabilization of the power is key.

(2) Standby

By setting the STBY pin to “L”, the standby mode is enabled. In the standby mode, the entire functions of the **NJU8752** enter a low-power state, and the output pins(OUT_P and OUT_N) are in high impedance.

(3) Mute

By setting the MUTE pin to “L”, the Mute function is enabled, and output pins(OUT_P and OUT_N) output square wave(Duty: 50%).

(4) Low Voltage Detector

When the power supply voltage drops down to below V_{DD}(MIN), the internal oscillation is halted not to generate unwanted frequency, and the output pins(OUT_P and OUT_N) become in high impedance.

(5) Short Protection Circuit

The short protector, which protects the NJU8752 from high short-circuit current, turns off the output driver. After about 5 seconds from the protection, the **NJU8752** returns to normal operation. The short protector is enabled in response to the following accidents.

-Short between OUT_P and OUT_N
-Short between OUT_P and V_{SS}
-Short between OUT_N and V_{SS}

Note 1) The detectable current and the period for the protection depend on the power supply voltage and ambient temperature.

Note 2) The short protector is not effective for a long term short-circuit but for an instantaneous accident. Continuous high-current may cause permanent damage to the **NJU8752**.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD} V_{DDO}	-0.3 ~ +4.0 -0.3 ~ +15.0	V V
Input Voltage		Vin	-0.3 ~ V_{DD}+0.3	V
Operating Temperature		Topr	-40 ~ +85	°C
Storage Temperature		Tstg	-40 ~ +125	°C
Power Dissipation	SSOP14	P_D	300	MW

Note 1) All voltage are relative to "V_{SS} =0V" reference.
Note 2) The LSI must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.
Note 3) De-coupling capacitors for V_{DD}(Pin 1)-V_{SS}(Pin 14), V_{DDO}(Pin 7)-V_{SS}(Pin 5) and V_{DDO}(Pin 8)-V_{SS}(Pin 10) should be connected for stable operation.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=3.3V, V_{DDO}=12.0V, V_{SS}=0V,
Input Signal=1kHz, Input Signal Level=200mVrms, Frequency Band=20Hz~20kHz,
Load Capacitance=0.8µF, 2nd-order 34kHz LC Filter (Q=0.75))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
V_{DD} Supply Voltage			3.0	3.3	3.6	V	
V_{DDO} Supply Voltage			9.0	12.0	13.75	V	
Output Power Efficiency	Eeff	Output T.H.D.=10%	80	-	-	%	4
Output T.H.D.	T.H.D.	Po= T.B.D	-	-	0.1	%	
Output Power	Po	Output T.H.D.=10%	-	T.B.D	-	W/ch	
S/N	SN	A weight	T.B.D	T.B.D	-	dB	
Dynamic Range	Drange	A weight	T.B.D	T.B.D	-	dB	
Maximum Mute Attenuation	MAT		-90	-	-	dB	
Operating Current(Stanby)	I_{ST}		-	-	10	µA	
Operating Current (No signal input)	I_{DD}	No-load operating No Signal Input	-	-	10	mA	
Input Voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V	
	V_{IL}		0	-	0.3V_{DD}	V	
Input Leakage Current	I_{LK}		-	-	±1.0	µA	

Note 4) Test system of the output T.H.D., S/N, Dynamic Range

The output T.H.D., S/N and dynamic range are tested in the system shown in Figure 1, where a 2nd-order LC LPF and another filter incorporated in an audio analyzer are used.

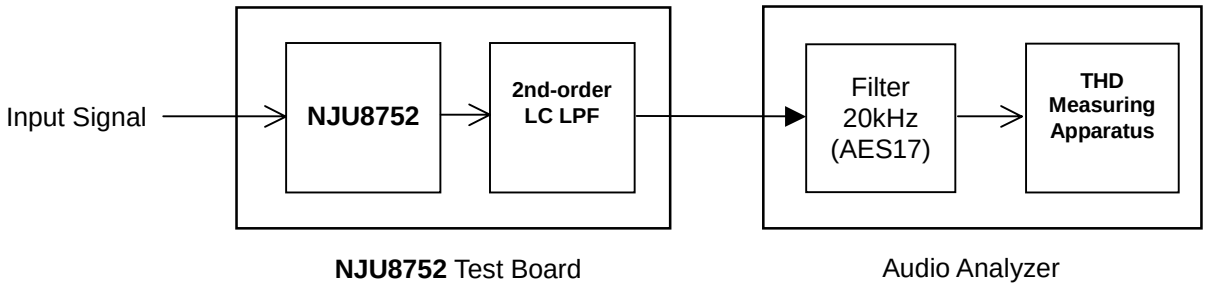


Figure 1. Output T.H.D., S/N and Dynamic Range Test System

2nd-order LPF : fc=34kHz / Refer to “Typical Application Circuit”.
Filters : 22Hz HPF + 20kHz LPF(AES17)
(with the A-Weight filter for S/N and Dynamic-range tests)

■ TYPICAL APPLICATION CIRCUIT

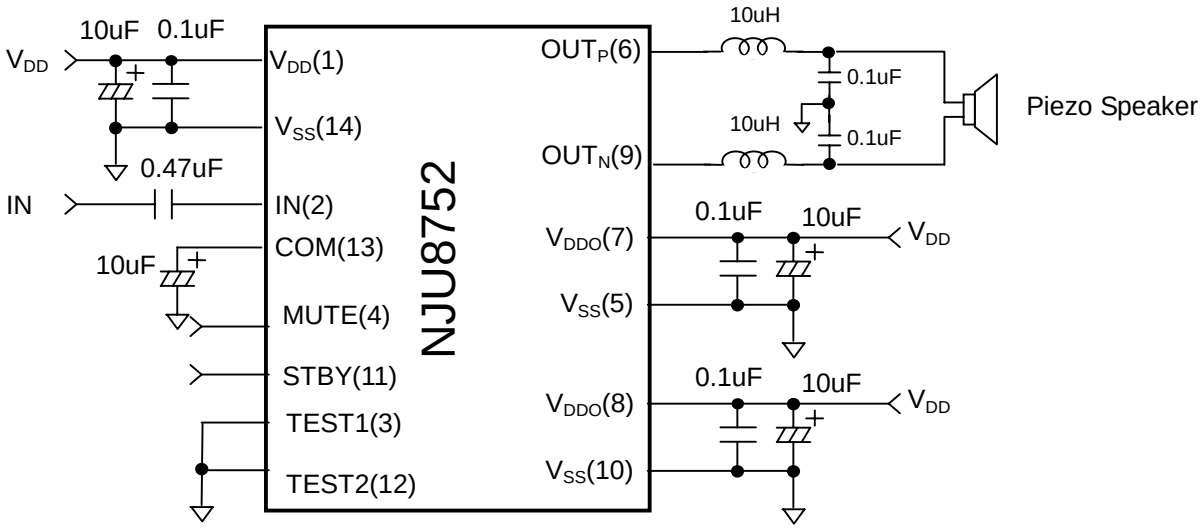


Figure 2. Application Circuit example

Note 5) De-coupling capacitors must be connected between each power supply pin and GND.
Note 6) A switching regulator with a high response against a voltage fluctuation is ideal for the V_{DDO} to obtain better T.H.D. performance.
Note 7) Testing actual samples in your system is highly recommended. The typical application circuit is one of examples.
Note 8) The transition time of MUTE and STBY signals must be less than 100us. Otherwise, a malfunction might occur.
Note 9) (1)-(14) indicates pin number.