National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMC555-X REV 2A1

Original Creation Date: 08/16/95
Last Update Date: 06/20/00
Last Major Revision Date: 06/15/00

CMOS, LOW VOLTAGE, PRECISION TIMER, SINGLE

General Description

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. It offers the same capability of generating accurate time delays and frequencies but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS(TM) process extends both the frequency range and low supply capability.

Industry Part Number

LMC555

NS Part Numbers

LMC555H/883
LMC555J/883

Prime Die

LMC555

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Less than 1 mW typical power dissipation at 5V supply.
- 3 MHz astable frequency capability.
- 1.5V supply operating voltage guaranteed.
- Output fully compatible with TTL and CMOS logic at 5V supply.
- Tested to -10 mA, +50 mA output current levels.
- Reduced supply current spikes during output transitions.
- Extremely low reset, trigger, and threshold currents.
- Excellent temperature stability.
- Pin-for-pin compatible with 555 series of timers.

CONTROLLING DOCUMENT:

LMC555H/883	5962-8950305GA
LMC555J/883	5962-8950305PA

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage, V8	15V
Input Voltages, V2,V4,V5,V6	-0.3V to Vs +0.3V
Output Voltages, V3,V7	15V
Output Current I3, I7	100mA
Operating Temperature Range	-55 C ≤Ta≤ +125 C
Storage Temperature Range	-65 C ≤Ta≤ +150 C
Maximum Junction Temperature	175 C
Maximum Power Dissipation (Note 2)	550mW
Thermal Resistance	
ThetaJA	
H-Pkg (Still Air)	180 C/W
J-Pkg (Still Air)	125 C/W
ThetaJC	30 C/W
ESD Tolerance (Note 3)	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The Maximum Power Dissipation must be derated at elevated temperatures, and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Rating, whichever is lower.

Note 3: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Idd	Power Supply Current	Vdd = 1.5V				200	uA	1, 2, 3
		Vdd = 5.0V				300	uA	1, 2, 3
		Vdd = 12.0V				400	uA	1, 2, 3
		Vdd = 15.0V				600	uA	1, 2, 3
Vtr	Trigger Voltage	Vdd = 1.5V			0.40	0.60	V	1, 2, 3
		Vdd = 5.0V			1.30	2.00	V	1, 2, 3
		Vdd = 12V			3.70	4.30	V	1, 2, 3
Itr	Trigger Current	Vdd = 1.5V				±50	nA	1, 2
		Vdd = 5.0V				±50	nA	1, 2
		Vdd = 12.0V				±50	nA	1, 2
Vth	Threshhold Voltage	Vdd = 1.5V			0.70	1.30	V	1, 2, 3
		Vdd = 5.0V			2.70	3.90	V	1, 2, 3
		Vdd = 12.0V			7.30	8.70	V	1, 2, 3
Ith	Threshhold Current	Vdd = 1.5V				±50	nA	1, 2
		Vdd = 5.0V				±50	nA	1, 2
		Vdd = 12.0V				±50	nA	1, 2
Voh	High Level Output Voltage	Vdd = 1.5V, Ioh = -0.25mA			1.00	1.50	V	1, 2, 3
		Vdd = 5.0V, Ioh = -1.0mA			4.20	5.00	V	1, 2, 3
		Vdd = 12.0V, Ioh = -10.0mA			10.25	12.00	V	1, 2, 3
		Vdd = 12.0V, Ioh = -5.0mA			10.70	12.00	V	1, 2, 3
		Vdd = 12.0V, Ioh = -1.0mA			11.00	12.00	V	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vol	Low Level Output Voltage	Vdd = 1.5V, Iol = 1.0mA				0.40	V	1, 2, 3
		Vdd = 5.0V, Iol = 8.0mA				0.60	V	1, 2, 3
		Vdd = 5.0V, Iol = 5.0mA				0.45	V	1, 2, 3
		Vdd = 5.0V, Iol = 3.2mA				0.40	V	1, 2, 3
		Vdd = 12.0V, Iol = 75mA				3.50	V	1, 2, 3
		Vdd = 12.0V, Iol = 50mA				2.25	V	1, 2, 3
		Vdd = 12.0V, Iol = 10mA				1.00	V	1, 2, 3
Icex	Discharge Transistor Leakage Current	Vdd = 1.5V				100	nA	1
						1000	nA	2
		Vdd = 5.0V				100	nA	1
						1000	nA	2
		Vdd = 12.0V				100	nA	1
						1000	nA	2
Ir	Reset Current	Vdd = 1.5V				±50	nA	1, 2
		Vdd = 5.0V				±50	nA	1, 2
		Vdd = 12.0V				±50	nA	1, 2
Vsat	Discharge Transistor Saturation Voltage	Vdd = 1.5V, Iol = 1.0mA				0.15	V	1, 2, 3
		Vdd = 5.0V, Iol = 10mA				0.30	V	1, 2, 3
		Vdd = 12.0V, Iol = 25mA				2.00	V	1, 2, 3

AC PARAMETERS

tMON	Monostable Timing Accuracy	1.5V ≤ Vdd ≤ 12.0V, Rt = 10K Ohm, Ct = 0.1uF			900	1250	uS	9, 10, 11
tAST	Astable Timing Accuracy	Vdd = 12.0V, Ct = 0.1uF, Rta = 1k Ohm, Rtb = 1k Ohm			178	250	uS	9, 10, 11

Graphics and Diagrams

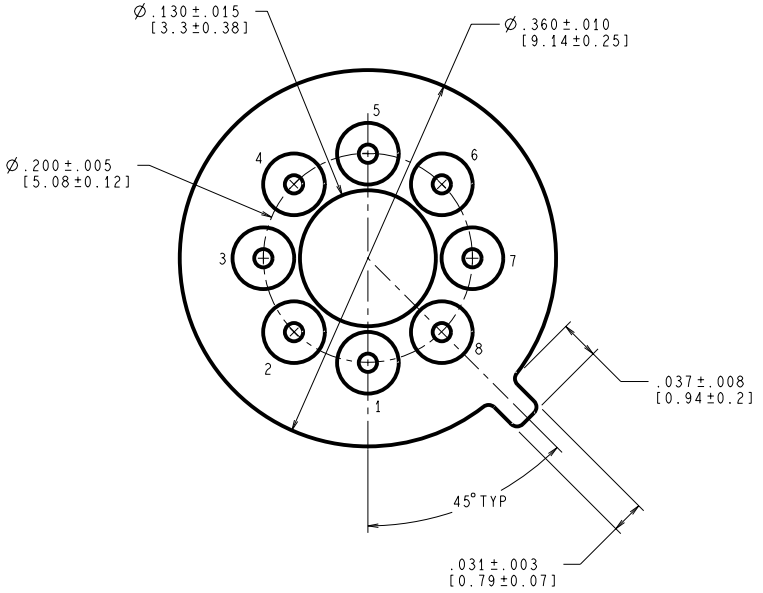
GRAPHICS#	DESCRIPTION
See attached graphics following this page.	

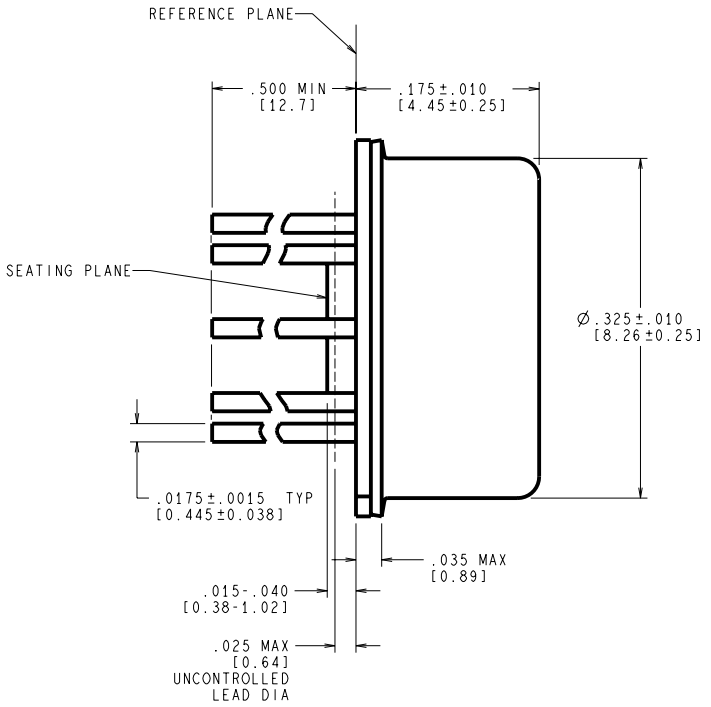
Graphics and Diagrams (Continued)

GRAPHICS#	DESCRIPTION
5798HRA2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
6150HRA1	CERDIP (J), 8 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000391A	METAL CAN (H), TO-99, 8LD .200 DIA P.C.(PIN OUT)
P000392A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

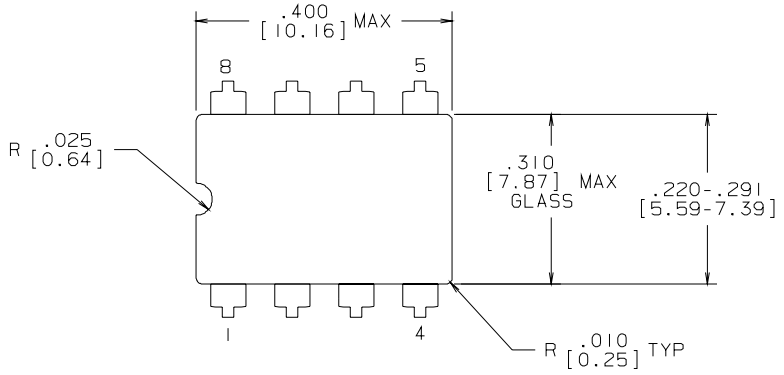
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

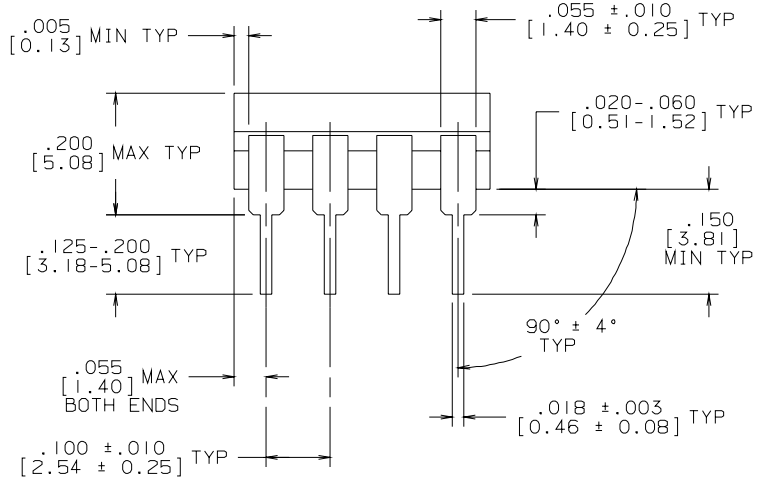
PROJECTION — INCH [MM]

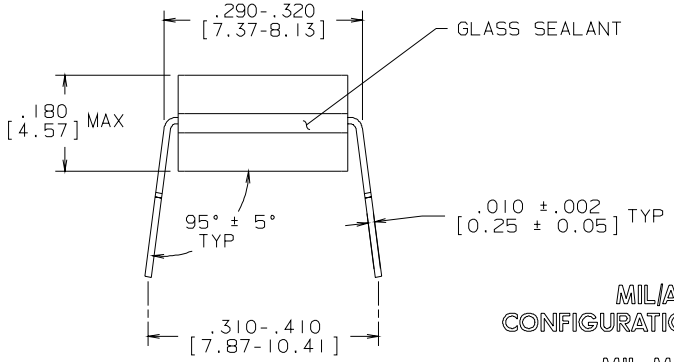
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

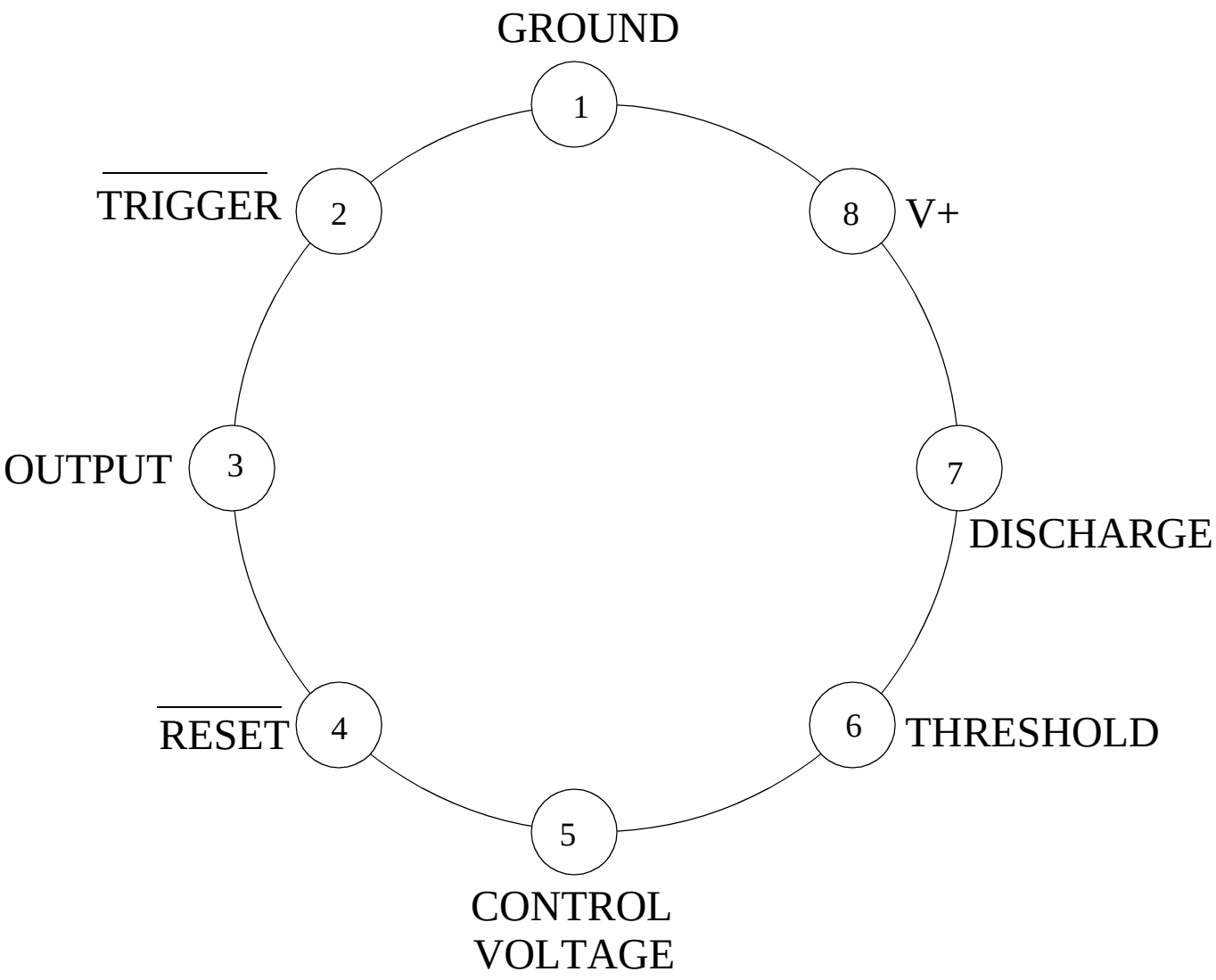
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

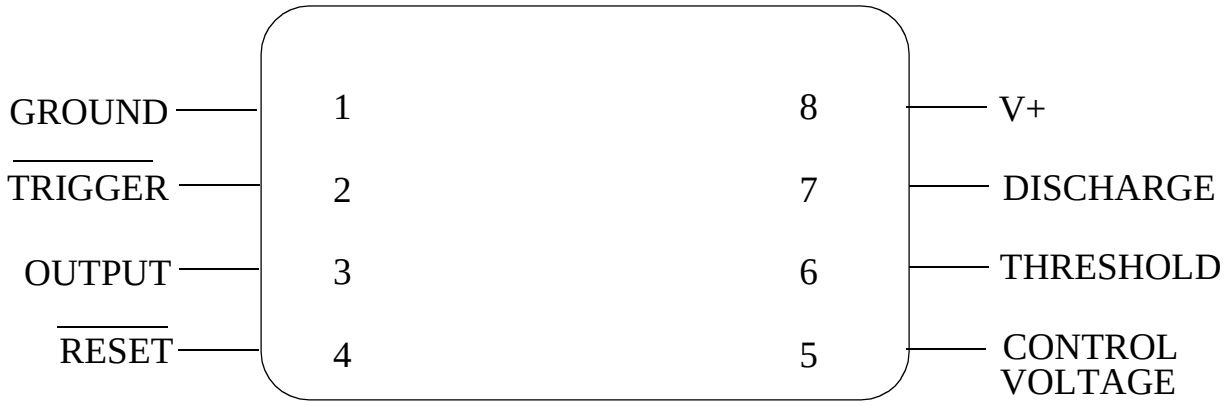
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMC555H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000391A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LMC555J

8 - LEAD CERDIP

CONNECTION DIAGRAM

TOP VIEW

P000392A

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Revision History

Rev	ECN #	Rel Date	Originator	Changes
1AL	M0002722	06/20/00	Barbara Lopez	Update MDS: MNLMC555-X Rev. 0AL to MNLMC555-X Rev. 1AL. Verifed NSID, Per DESC drawing, change limit for high temp from 300nA to 1000nA, added thermal data, updated operating temperature range, updated junction temperature range.
2A1	M0003726	06/20/00	Rose Malone	Update MDS: MNLMC555-X, Rev. 1AL to MNLMC555-X, Rev. 2A1 Fully Released MDS. Moved reference to Controlling Documents to Features Section. Changed Voh Min. limit for condition Vdd = 12.0V, Ioh = -10.0mA from 10.50V to 10.25V and Vol Max. limit for condition Vdd = 12.0V, Ioh = 50mA from 2.00V to 2.25V. Added Pin Out graphics to graphics section.