Z8060 FIFO

Buffer Unit and FIFO Expander

DISTINCTIVE CHARACTERISTICS

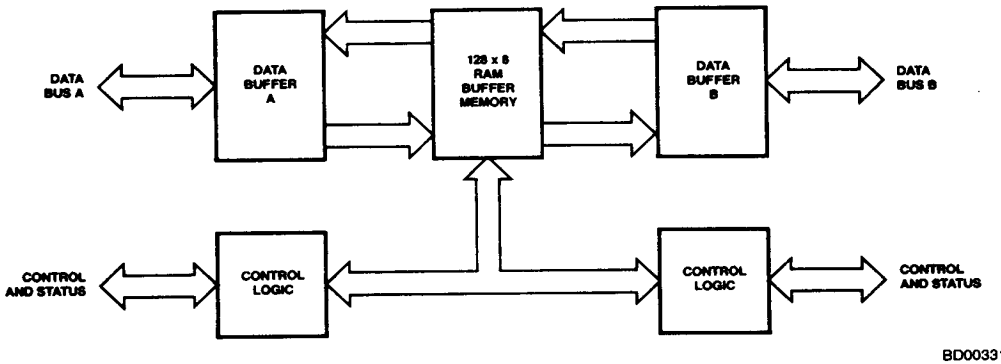
- Bidirectional, asynchronous data transfer capability
- Large 128-bit-by-8-bit buffer memory
- Two-wire, interlocked handshake protocol
- 3-state data outputs
- Wire-ORing of empty and full outputs for sensing of multiple-unit buffers
- Connects any number of FIFOs in series to form buffer of any desired length
- Connects any number of FIFOs in parallel to form buffer of any desired width

GENERAL DESCRIPTION

The Z8060* First-In, First-Out (FIFO) buffer unit consists of a 128-bit-by-8-bit memory, bidirectional data transfer and handshake logic. The structure of the FIFO unit is similar to that of other available buffer units. FIFO is a general-purpose unit; its handshake logic is compatible with that of other members of the Z8000 family.

FIFOs can be cascaded end-to-end without limit to form a parallel 8-bit buffer of any desired length (in 128-byte increments). Any number of single- or multiple-unit FIFO serial buffers can be connected in parallel to form buffers of any desired width (in 8-bit increments).

FIFO BLOCK DIAGRAM



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*Z8000 is a trademark of Zilog, Inc.

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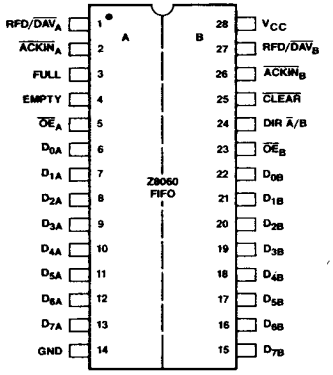
CONNECTION DIAGRAM
Top View
D-28, P-28



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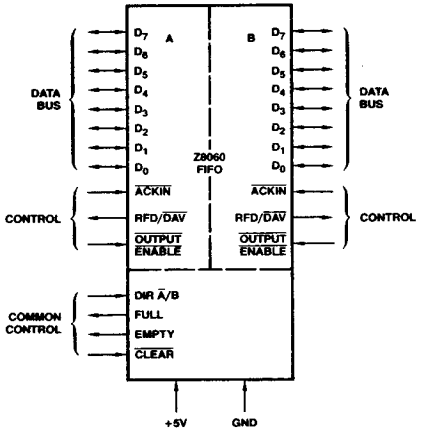
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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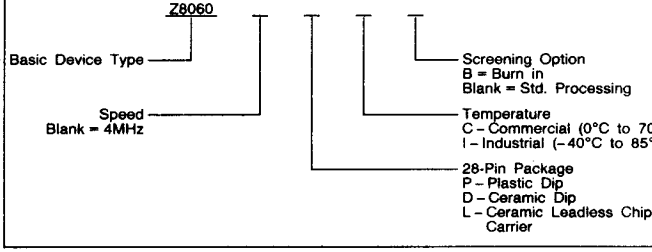
ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Z8060	DC, DCB DI, DIB

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
28	V_{CC}		+5V Power Supply.
14	GND		Ground.
2, 26	$\overline{ACKIN}$	I active LOW	Acknowledge Input. This line signals the FIFO that output data has been received by peripherals or that input data is valid.
25	$\overline{CLEAR}$	I active LOW	Clear Buffer. When set to LOW, this line causes all data to be cleared from the FIFO buffer.
6 – 13	D_0-D_7	I/O	Data Bus (bidirectional). These bidirectional lines are used by the FIFO to receive and to transmit data.
24	DIR $\overline{A}$/B	I	Direction Input $\overline{A}$/B (two control states). A HIGH on this line signals that input data is to be received at port B. A LOW on this line signals that input data is to be received at port A.
4	EMPTY	O active HIGH	Buffer Status (open-drain). A HIGH on this line indicates that the FIFO buffer is empty.
3	FULL	O active HIGH	Buffer Status (open-drain). A HIGH on this line indicates that the FIFO buffer is full.
5, 23	$\overline{OE}_A$, $\overline{OE}_B$	I active LOW	Output Enable A, Output Enable B. When LOW, $\overline{OE}_A$ enables the bus drivers for port A; when HIGH, $\overline{OE}_A$ causes the bus drivers to float to a high-impedance level. Input $\overline{OE}_B$ controls the bus drivers for port B in the same manner as $\overline{OE}_A$ controls those for port A.
1, 27	RFD/$\overline{DAV}$	O	Ready-for-Data/Data Available (outputs RFD, active HIGH, $\overline{DAV}$ active LOW). RFD, when HIGH, signals to the peripherals involved that the FIFO is ready to receive data. $\overline{DAV}$, when LOW, signals to the peripherals involved that FIFO has data available to send.

DETAILED DESCRIPTION

Interlocked 2-Wire Handshake

In interlocked 2-wire handshake operation, the action of FIFO must be acknowledged by the other half of the handshake before the next action can occur. In an Output Handshake mode, the FIFO indicates that new data is available only after the external device has indicated that it is ready for the data. In an Input Handshake mode, the FIFO does not indicate that it is ready for new data until the data source indicates that the previous byte of the data is no longer available, thereby acknowledging the acceptance of the last byte. This control feature allows the FIFO, with no external logic, to directly interface with the port of any CPU in the Z8 Family — a CIO, a UPC, an FIO, or another FIFO. The timing for the input and output handshake operations is shown in Figures 1 and 2, respectively.

Resetting or Clearing the FIFO

The $\overline{CLEAR}$ is used to initialize and clear the FIFO. A Low level on this input clears all data from the FIFO, allows the EMPTY output to go HIGH and forces both outputs RFD/$\overline{DAV}_A$ and RFD/$\overline{DAV}_B$ HIGH. A HIGH level on $\overline{CLEAR}$ allows the data to transfer through the FIFO.

Bidirectional Transfer Control

The FIFO has bidirectional data transfer capability under control of the DIR $\overline{A}$/B input. When DIR $\overline{A}$/B is set LOW, port A becomes input handshake and port B becomes output handshake; data transfers are then made from port A to port B. Setting DIR $\overline{A}$/B HIGH reverses the handshake assignments and the direction of transfer. This bidirectional control is illustrated in Table 1.

TABLE 1. BIDIRECTIONAL CONTROL FUNCTION TABLE

DIR $\overline{A}$/B	Port A Handshake	Port B Handshake	Transfer
0	Input	Output	A to B
1	Output	Input	B to A

The FIFO buffer must be empty before the direction of transfer is changed; otherwise, the results of the change will be unpredictable. If FIFO status is unknown when a transfer direction change is to be made, the recommended procedure is:

(1) Force and hold $\overline{CLEAR}$ LOW,
(2) Set DIR $\overline{A}$/B to the level required for the desired direction, and then
(3) Force $\overline{CLEAR}$ HIGH.

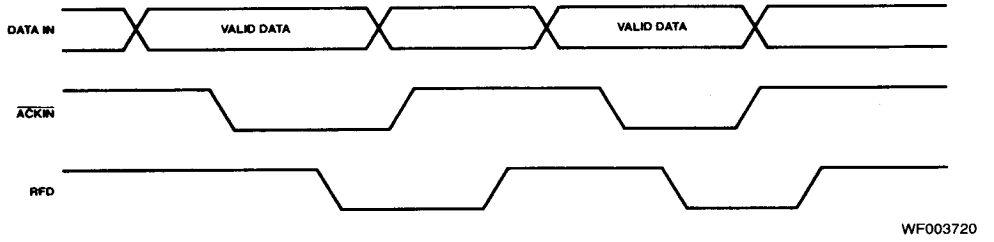

Figure 1. Two-Wire Interlocked Handshake Timing (Input)

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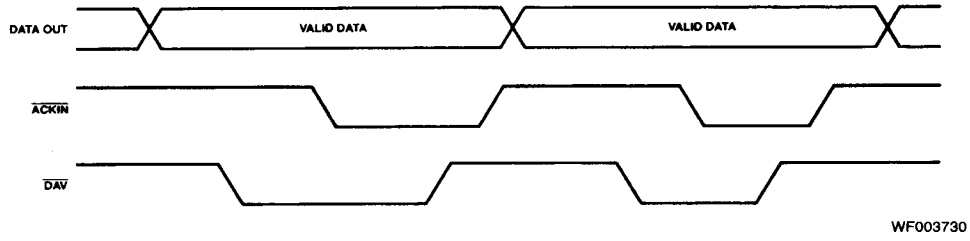


Figure 2. Two-Wire Interlocked Handshake Timing (Output)

EMPTY and FULL Operation

The EMPTY and FULL output lines can be wire-ORed with the EMPTY and FULL lines of other FIFOs and FIOs. This capability enables the user to determine the EMPTY/FULL status of a buffer consisting of multiple FIFOs, FIOs, or a combination of both. Table 2 shows the various states of EMPTY and FULL.

TABLE 2. SIGNALS EMPTY AND FULL OPERATION TABLE

Number of Bytes in FIFO	Empty	Full
0	HIGH	LOW
1-127	LOW	LOW
128	LOW	HIGH

Interconnection Example

A simplified block diagram showing the manner in which FIFOs can be interconnected to extend a FIO buffer is shown in Figure 3.

Output Enable Operation

The FIFO provides a separate Output Enable ($\overline{OE}$) signal for each port of the buffer. An $\overline{OE}$ output is valid only when its port is in the Output Handshake mode. The control of this output function is shown in Table 3. Signal $\overline{OE}$ operates with lines DIR $\overline{A}$/B. A HIGH on a valid $\overline{OE}$ line 3-states its port's data bus but does not affect the handshake operation. A LOW level on a valid $\overline{OE}$ enables the data bus outputs if its port is in the Output Handshake mode. Note that the handshake operation is unaffected by the Output Enable pin.

TABLE 3. OUTPUT CONTROL FUNCTION TABLE

DIR $\overline{A}$/B	$\overline{OE}_A$	$\overline{OE}_B$	Function
0	X	0	Disable Port A Output Enable Port B Output
0	X	1	Disable Port A Output Disable Port B Output
1	0	X	Enable Port A Output Disable Port B Output
1	1	X	Disable Port A Output Disable Port B Output

Note: X = Don't Care.

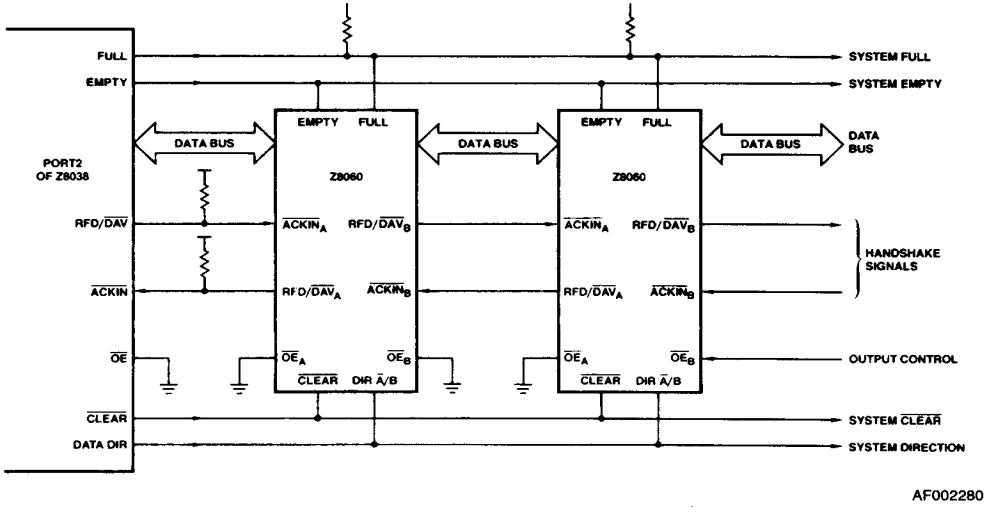


Figure 3. Typical Interconnection (Simplified Diagram)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage to any Pin Relative to V_{SS} ..... −0.5 to +7.0V
Power Dissipation 1.8W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

	Z8060
Commercial Operating Range T_A = 0 to +70°C V_{CC} = 5V ±5% V_{SS} = 0V	Z8060DC
Industrial Operating Range T_A = −40 to +85°C V_{CC} = 5V ±10% V_{SS} = 0V	Z8060DI

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 1)

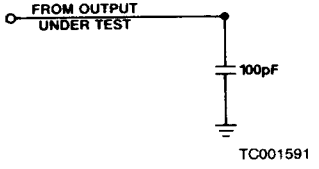
Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input LOW Voltage		−0.3		+0.8	Volts
V_{IH}	Input HIGH Voltage	Standard Temp	2.0		V_{CC} +0.3	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA			0.5	Volts
		I_{OL} = 2.0mA			0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = −250µA	2.4			Volts
I_{OZL}	Output Leakage Current	V_{OUT} = 0.4V			10	µA
I_{OZH}	Output Leakage Current	V_{OUT} = V_{CC}			10	µA
I_I	Input Leakage Current				±10	µA
C_{IN}	Input Capacitance	Unmeasured pins returned to ground. f = 1MHz over specified temperature range.			10	pF
$C_{I/O}$	I/O Capacitance				20	pF
C_{OUT}	Output Capacitance				15	pF
I_{CC}	Power Supply Current	V_{CC} = MAX			250	mA

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75V ≤ V_{CC} ≤ +5.25V
GND = 0V
0°C ≤ T_A ≤ +70°C

Test Load Conditions



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FIFO 2-WIRE HANDSHAKE TIMING

Timing for 2-wire interlock handshake operation is shown in Figure 1. The symbol, description and values for the numbered parameters (Figure 1) are given in Switching Characteristics.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Number	Parameters	Description	Min	Max	Units
1	TsDI(ACK)	Data Input to $\overline{ACKIN}\downarrow$ to Setup Time	50		ns
2	TdACKf(RFD)	$\overline{ACKIN}\downarrow$ to RFD↓ Delay	0	500	ns
3	TdRFDr(ACK)	RFD↑ to $\overline{ACKIN}\downarrow$ Delay	0		ns
4	TsDO(DAV)	Data Out to $\overline{DAV}\downarrow$ Setup Time	25		ns
5	TdDAVf(ACK)	DAV↓ to $\overline{ACKIN}\downarrow$ Delay	0		ns
6	ThDO(ACK)	Data Out to $\overline{ACKIN}\uparrow$ Hold Time	50		ns
7	TdACK(DAV)	$\overline{ACKIN}\downarrow$ to $\overline{DAV}\uparrow$ Delay	0	500	ns
8	ThDI(RFD)	Data input to RFD ↓ Hold Time	0		ns
9	TdRFDf(ACK)	RFD↓ to $\overline{ACKIN}\uparrow$ Delay	0		ns
10	TdACKr(RFD)	$\overline{ACKIN}$ ↑ to RFD ↑ Delay	0	400	ns
11	TdDAVr(ACK)	DAV ↑ to $\overline{ACKIN}$ ↑	0		ns
12	TdACKr(DAV)	$\overline{ACKIN}$ ↑ to $\overline{DAV}$ ↓	0	800	ns
13	TdACKINf(EMPTY)	(Input) $\overline{ACKIN}$ ↓ to EMPTY ↓ Delay		600	ns
		(Output) $\overline{ACKIN}$ ↓ to EMPTY ↑ Delay			
14	TdACKINf(FULL)	(Input) $\overline{ACKIN}$ ↓ to FULL ↑ Delay		600	ns
		(Output) $\overline{ACKIN}$ ↓ to FULL ↓ Delay			
15	ACKIN Clock Rate	(Input)		1.0	MHz
16	TdACKINf($\overline{DAV}$f)	(Bubble Time)		800	ns
17	TwCLR	Width of Clear to Reset FIFO	700		ns
18	TdOE(DO)	$\overline{OE}$ ↓ to Data Bus Driven	0	150	ns
19	TdOE(DRZ)	$\overline{OE}$ ↑ to Data Bus Float		100	ns

Note: All timing references assume 2.0V for a logic 1 and 0.8V for a logic 0.

SWITCHING WAVEFORMS

INPUT TIMING

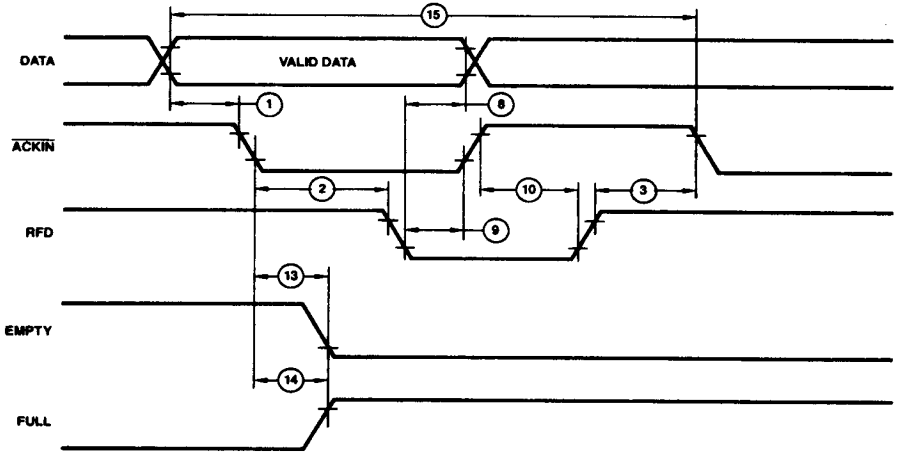
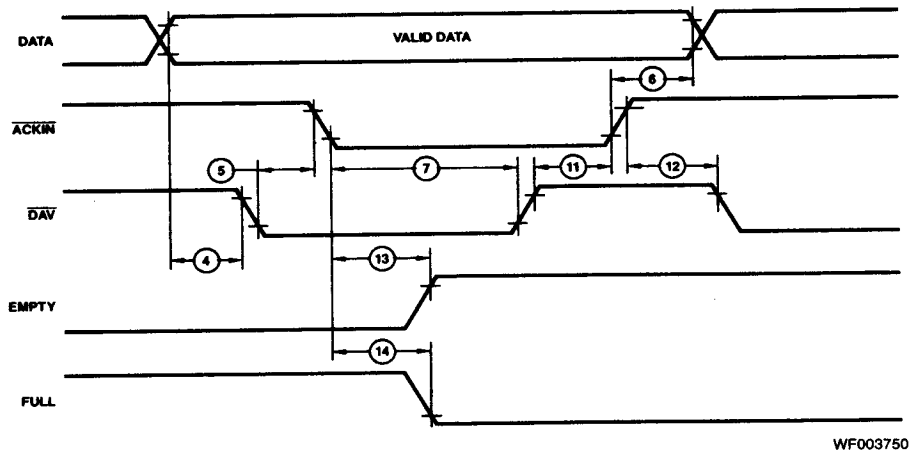


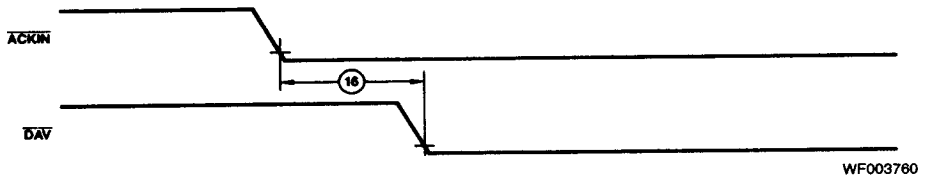
Figure 4. Timing Diagrams

SWITCHING WAVEFORMS (Cont.)

OUTPUT TIMING



ACKNOWLEDGE INPUT DATA TO DATA AVAILABLE TIME (BUBBLE TIME)



OUTPUT ENABLE AND CLEAR

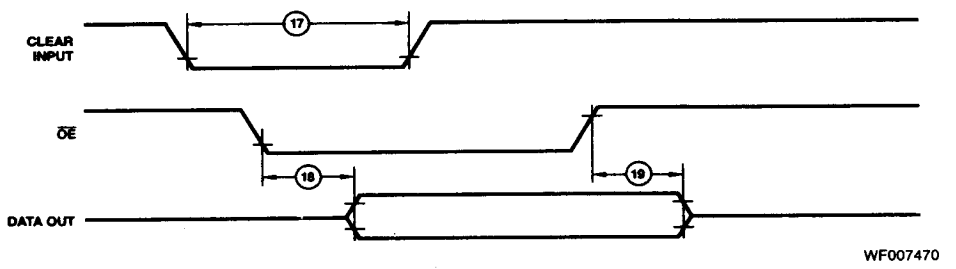


Figure 4. Timing Diagrams (Cont.)