14-Bit, 80 MSPS, A/D Converter

AD9444

FEATURES

80 MSPS guaranteed sampling rate
100 dB two-tone SFDR with 69.3 MHz and 70.3 MHz
73.1 dB SNR with 70 MHz input
97 dBc SFDR with 70 MHz input
Excellent linearity
DNL = ±0.4 LSB typical
INL = ±0.6 LSB typical
1.2 W power dissipation
3.3 V and 5 V supply operation
2.0 V p-p differential full-scale input
LVDS outputs (ANSI-644 compatible)
Data format select
Output clock available

APPLICATIONS

Multicarrier, multimode cellular receivers
Antenna array positioning
Power amplifier linearization
Broadband wireless
Radar, infared imaging
Communications instrumentation

GENERAL DESCRIPTION

The AD9444 is a 14-bit monolithic, sampling analog-to-digital converter (ADC) with an on-chip, track-and-hold circuit and is optimized for power, small size, and ease of use. The product operates at up to an 80 MSPS conversion rate and is optimized for multicarrier, multimode receivers, such as those found in cellular infrastructure equipment.

The ADC requires 3.3 V and 5.0 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are LVDS-compatible (ANSI-644) or CMOS-compatible and include the means to reduce the overall current needed for short trace distances.

FUNCTIONAL BLOCK DIAGRAM

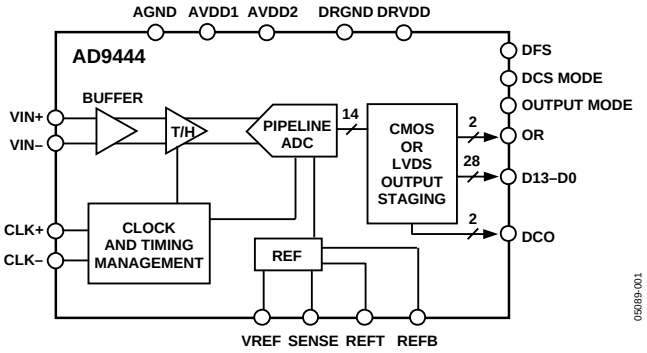

Figure 1.

Optional features allow users to implement various selectable operating conditions, including data format select and output data mode.

The AD9444 is available in a 100-lead surface-mount plastic package (100-lead TQFP/EP) specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High performance: Outstanding SFDR performance for multicarrier, multimode 3G and 4G cellular base station receivers.
2. Ease of use: On-chip reference and track-and-hold. An output clock simplifies data capture.
3. Packaged in a Pb-free, 100-lead TQFP/EP.
4. Clock DCS maintains overall ADC performance over a wide range of clock pulse widths.
5. OR (out-of-range) outputs indicate when the signal is beyond the selected input range.

Rev. 0

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AD9444* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9444: 14-Bit, 80 MSPS, A/D Converter Data Sheet

TOOLS AND SIMULATIONS

- Visual Analog
- AD9444 IBIS Models

REFERENCE MATERIALS

Technical Articles

- Correlating High-Speed ADC Performance to Multicarrier 3G Requirements
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9444 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9444 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

10/04—Revision 0: Initial Version

DC SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, LVDS mode, sample rate = 80 MSPS, 2 V p-p differential input, internal trimmed reference (1.0 V mode), A_{IN} = −0.5 dBFS, DCS on, unless otherwise noted.

Table 1.

			AD9444BSVZ-80			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	VI		14		Bits
ACCURACY						
No Missing Codes	Full	VI		Guaranteed		
Offset Error	Full	VI	6	±0.3	6	mV
Gain Error[1]	Full	VI	−3.0	±0.4	+3.0	% FSR
Differential Nonlinearity (DNL)[2]	Full	VI	−0.8	±0.4	+0.8	LSB
Integral Nonlinearity (INL)[2]	25°C	I	−1.3	±0.6	+1.3	LSB
	Full	VI	−1.7		+1.7	LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		12		µV/°C
Gain Error	Full	V		0.002		%FS/°C
VOLTAGE REFERENCE						
Output Voltage[1]	Full	VI	0.87	1.0	1.13	V
Load Regulation @ 1.0 mA	Full	V		±2		mV
Reference Input Current (External 1.0 V Reference)	Full	VI		80	125	µA
INPUT REFERRED NOISE	25°C	V		1.0		LSB rms
ANALOG INPUT						
Input Span	Full	V		2		V p-p
Input Common-Mode Voltage	Full	V		3.5		V
Input Resistance[3]	Full	V		1		kΩ
Input Capacitance[3]	Full	V		2.5		pF
POWER SUPPLIES						
Supply Voltage						
AVDD1	Full	IV	3.14	3.3	3.46	V
AVDD2	Full	IV	4.75	5.0	5.25	V
DRVDD—LVDS Outputs	Full	IV	3.0		3.6	V
DRVDD—CMOS Outputs	Full	IV	3.0	3.3	3.6	V
Supply Current						
AVDD1	Full	VI		217	240	mA
AVDD2[2]	Full	VI		71	80	mA
IDRVDD[2]—LVDS Outputs	Full	VI		55	62	mA
IDRVDD[2]—CMOS Outputs	Full	V		12		mA
PSRR						
Offset	Full	V		1		mV/V
Gain	Full	V		0.2		%/V
POWER CONSUMPTION						
DC Input—LVDS Outputs	Full	VI		1.21	1.4	W
DC Input—CMOS Outputs	Full	V		1.07		W
Sine Wave Input[2]—LVDS Outputs	Full	VI		1.25		W
Sine Wave Input[2]—CMOS Outputs	Full	V		1.11		W

[1] The internal voltage reference is trimmed at final test to minimize the gain error of the AD9444.
[2] Measured at the maximum clock rate, f_{IN} = 15 MHz, full-scale sine wave, with a 100 Ω differential termination on each pair of output bits for LVDS output mode and approximately 5 pF loading on each output bit for CMOS output mode.
[3] Input capacitance or resistance refers to the effective impedance between one differential input pin and AGND. Refer to Figure 6 for the equivalent analog input structure.

AC SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, LVDS mode, sample rate = 80 MSPS, 2 V p-p differential input, internal trimmed reference (1.0 V mode), A_{IN} = −0.5 dBFS, DCS on, unless otherwise noted.

Table 2.

			AD9444BSVZ-80			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)						
f_{IN} = 10 MHz	25°C	IV	73.0	74.0		dB
	Full	IV	72.7			dB
f_{IN} = 35 MHz	25°C	I	72.4	73.7		dB
	Full	IV	72.3			dB
f_{IN} = 70 MHz	25°C	IV	72.3	73.1		dB
	Full	IV	72.0			dB
f_{IN} = 100 MHz	25°C	V		72.3		dB
SIGNAL-TO-NOISE-AND DISTORTION (SINAD)						
f_{IN} = 10 MHz	25°C	IV	73.0	74.0		dB
	Full	IV	72.7			dB
f_{IN} = 35 MHz	25°C	I	72.4	73.7		dB
	Full	IV	72.2			dB
f_{IN} = 70 MHz	25°C	IV	72.2	73.1		dB
	Full	IV	72.0			dB
f_{IN} = 100 MHz	25°C	V		72.3		dB
EFFECTIVE NUMBER OF BITS (ENOB)						
f_{IN} = 10 MHz	25°C	V		12.1		Bits
f_{IN} = 35 MHz	25°C	V		12.0		Bits
f_{IN} = 70 MHz	25°C	V		11.9		Bits
f_{IN} = 100 MHz	25°C	V		11.8		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)						
f_{IN} = 10 MHz	25°C	IV	91	97		dBc
	Full	IV	87			dBc
f_{IN} = 35 MHz	25°C	I	91	97		dBc
	Full	IV	87			dBc
f_{IN} = 70 MHz	25°C	IV	90	97		dBc
	Full	IV	87			dBc
f_{IN} = 100 MHz	25°C	V		96		dBc
WORST HARMONIC, SECOND OR THIRD						
f_{IN} = 10 MHz	25°C	IV		−97	−91	dBc
	Full	IV			−87	dBc
f_{IN} = 35 MHz	25°C	I		−97	−91	dBc
	Full	IV			−87	dBc
f_{IN} = 70 MHz	25°C	IV		−97	−90	dBc
	Full	IV			−87	dBc
f_{IN} = 100 MHz	25°C	V		−96		dBc
WORST SPUR EXCLUDING SECOND OR HARMONICS						
f_{IN} = 10 MHz	25°C	IV		−102	−93	dBc
	Full	IV			−93	dBc
f_{IN} = 35 MHz	25°C	I		−103	−93	dBc
	Full	IV			−93	dBc
f_{IN} = 70 MHz	25°C	IV		−102	−93	dBc
	Full	IV			−93	dBc
f_{IN} = 100 MHz	25°C	V		−99		dBc
TWO-TONE SFDR						
f_{IN} = 10.8 MHz @ −7 dBFS, 9.8 MHz @ −7 dBFS	25°C	V		−102		dBFS
f_{IN} = 70.3 MHz @ −7 dBFS, 69.3 MHz @ −7 dBFS	25°C	V		−100		dBFS
ANALOG BANDWIDTH	Full	V		650		MHz

DIGITAL SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, $R_{LVDSBIAS}$ = 3.74 kΩ, unless otherwise noted.

Table 3.

			AD9444BSVZ-80			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
CMOS LOGIC INPUTS (DFS, DCS MODE, OUTPUT MODE)						
High Level Input Voltage	Full	IV	2.0			V
Low Level Input Voltage	Full	IV			0.8	V
High Level Input Current	Full	VI			+200	µA
Low Level Input Current	Full	VI	−10		+10	µA
Input Capacitance	Full	V		2		pF
DIGITAL OUTPUT BITS—CMOS Mode (D0 to D13, OTR)[1]						
DRVDD = 3.3 V						
High Level Output Voltage	Full	IV	3.25			V
Low Level Output Voltage	Full	IV			0.2	V
DIGITAL OUTPUT BITS LVDS Mode (D0 to D13, OTR)						
V_{OD} Differential Output Voltage[2]	Full	VI	247		545	mV
V_{OS} Output Offset Voltage	Full	VI	1.125		1.375	V
CLOCK INPUTS (CLK+, CLK−)						
Differential Input Voltage	Full	IV	0.2			V
Common-Mode Voltage	Full	VI	1.3	1.5	1.6	V
Differential Input Resistance	Full	V	8	10	12	kΩ
Differential Input Capacitance	Full	V		4		pF

[1] Output voltage levels measured with 5 pF load on each output.
[2] LVDS R_{TERM} = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	AD9444BSVZ-80			Unit
			Min	Typ	Max	
CLOCK INPUT PARAMETERS						
Maximum Conversion Rate	Full	VI	80			MSPS
Minimum Conversion Rate	Full	V			10	MSPS
CLK Period	Full	V	12.5			ns
CLK Pulse Width High[1] (t_{CLKH})	Full	V	4			ns
CLK Pulse Width Low[1] (t_{CLKL})	Full	V	4			ns
DATA OUTPUT PARAMETERS						
Output Propagation Delay—CMOS (t_{PD})[2] (DX, DCO+)	Full	IV	3	5.25	8	ns
Output Propagation Delay—LVDS (t_{PD})[3] (DX+, DCO+)	Full	VI	3	5	7.5	ns
Pipeline Delay (Latency)	Full	V		12		Cycles
Aperture Delay (t_A)	Full	V				ns
Aperture Uncertainty (Jitter, t_J)	Full	V		0.2		ps rms

[1] With duty cycle stabilizer (DCS) enabled.
[2] Output propagation delay is measured from clock 50% transition to data 50% transition, with 5 pF load.
[3] LVDS R_{TERM} = 100 Ω. Measured from the 50% point of the rising edge of CLK+ to the 50% point of the data transition.

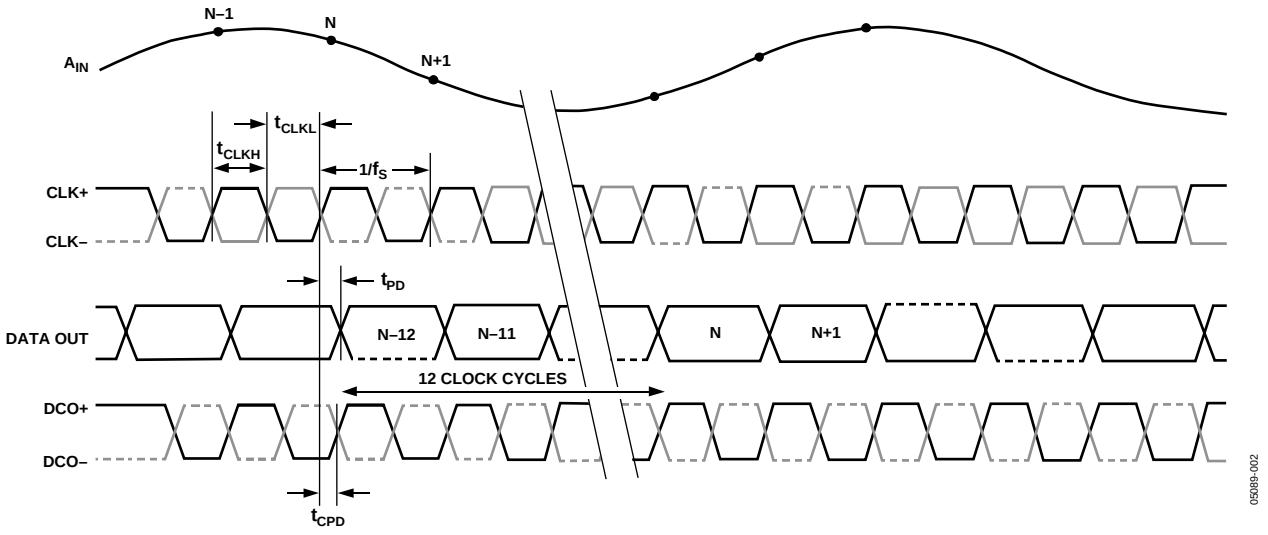


Figure 2. LVDS Mode Timing Diagram

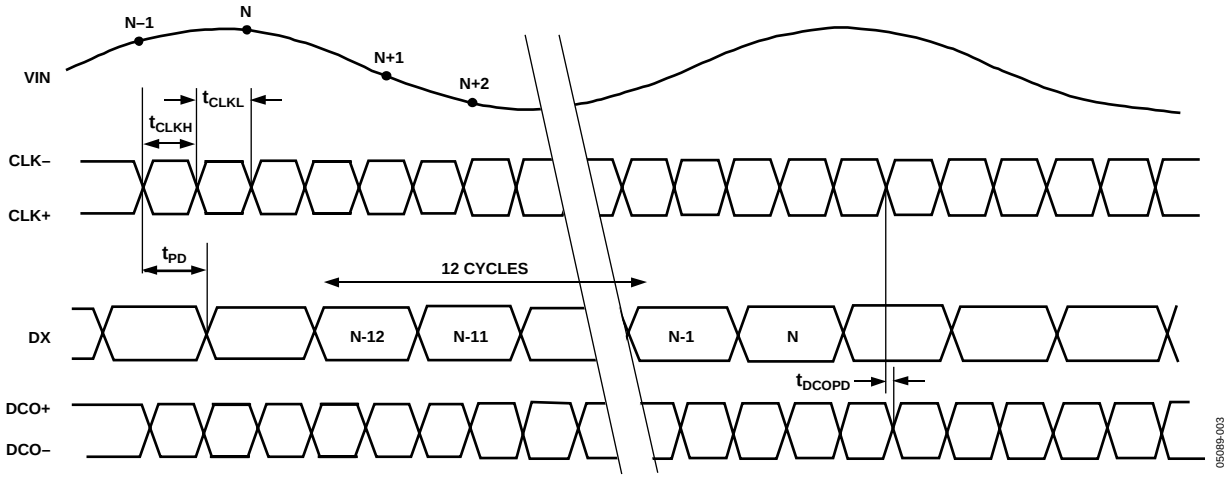


Figure 3. CMOS Timing Diagram

EXPLANATION OF TEST LEVELS

Test Level	Definitions
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD1	AGND	−0.3	+4	V
AVDD2	AGND	−0.3	+6	V
DRVDD	DGND	−0.3	+4	V
AGND	DGND	−0.3	+0.3	V
AVDD1	DRVDD	−4	+4	V
AVDD2	DRVDD	−4	+6	V
AVDD2	AVDD1	−4	+6	V
D0 to D13	DGND	−0.3	DRVDD + 0.3	V
CLK, MODE	AGND	−0.3	AVDD1 + 0.3	V
VIN+, VIN−	AGND	−0.3	AVDD2 + 0.3	V
VREF	AGND	−0.3	AVDD1 + 0.3	V
SENSE	AGND	−0.3	AVDD1 + 0.3	V
REFT, REFB	AGND	−0.3	AVDD1 + 0.3	V
ENVIRONMENTAL				
Storage Temperature		−65	+125	°C
Operating Temperature Range		−40	+85	°C
Lead Temperature Range (Soldering 10 sec)			300	°C
Junction Temperature			150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

The heat sink of the AD9444 package must be soldered to ground.

Table 6.

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
100-Lead TQFP/EP	19.8	8.3	2	°C/W

Typical θ_{JA} = 19.8°C/W (heat-sink soldered) for multilayer board in still air.

Typical θ_{JB} = 8.3°C/W (heat-sink soldered) for multilayer board in still air.

Typical θ_{JC} = 2°C/W (junction to exposed heat sink) represents the thermal resistance through heat-sink path.

Airflow increases heat dissipation effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads, from metal traces, through holes, ground, and power planes, reduces the θ_{JA}. It is required that the exposed heat sink be soldered to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth (Full Power Bandwidth)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter, t_J)
The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes must be present over all operating ranges.

Effective Number of Bits (ENOB)
The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur at an analog value 1 ½ LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Integral Nonlinearity (INL)
The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1 ½ LSBs beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Offset Error
The major carry transition should occur for an analog value ½ LSB below VIN+ = VIN−. Offset error is defined as the deviation of the actual transition from that point.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Output Propagation Delay (t_{PD})
The delay between the clock rising edge and the time when all bits are within valid logic levels.

Power-Supply Rejection Ratio
The change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Total Harmonic Distortion (THD)
The ratio of the rms input signal amplitude to the rms value of the sum of the first six harmonic components.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

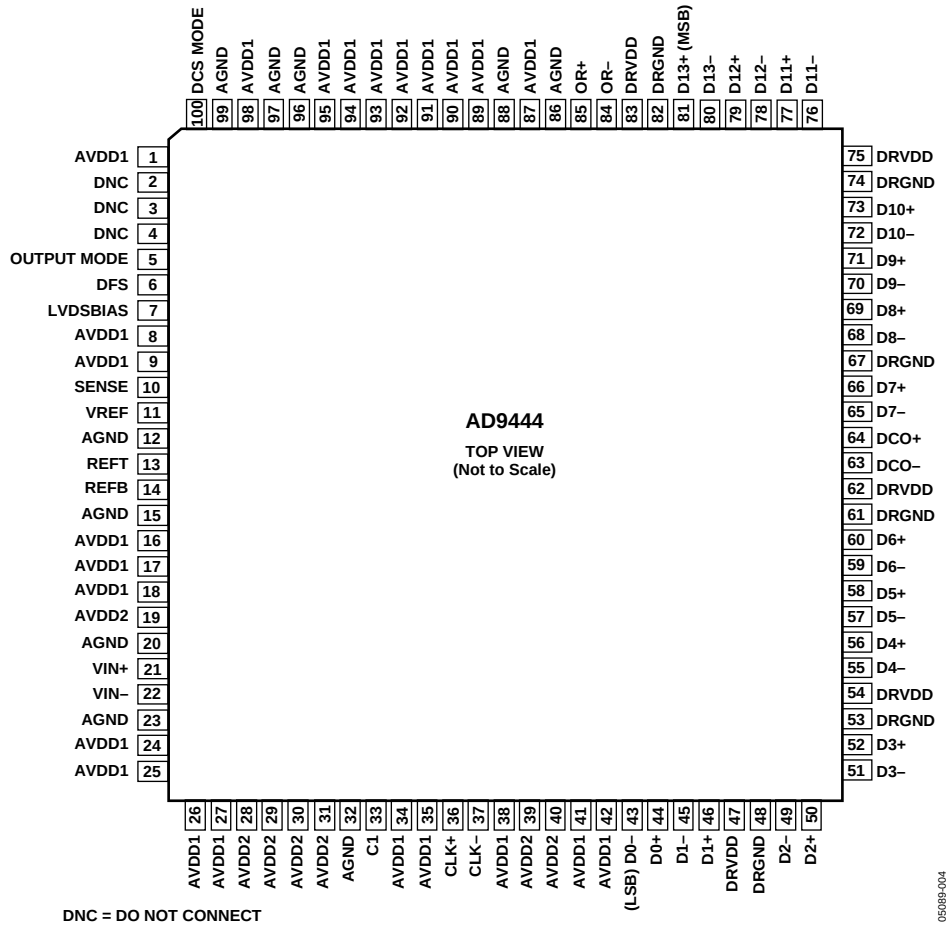


Figure 4. 100-Lead TQFP/EP Pin Configuration in LVDS Mode

Table 7. Pin Function Descriptions—100-Lead TQFP/EP in LVDS Mode

Pin No.	Mnemonic	Description
1, 8 to 9, 16 to 18, 24 to 27, 34 to 35, 38, 41 to 42, 87, 89 to 95, 98	AVDD1	3.3 V (±5%) Analog Supply.
2 to 4	DNC	Do Not Connect. These pins should float.
5	OUTPUT MODE	CMOS Compatible Output Logic Mode Control Pin. OUTPUT MODE = 0 for CMOS mode, and OUTPUT MODE = 1 (AVDD1) for LVDS outputs.
6	DFS	Data Format Select Pin. CMOS control pin that determines the format of the output data. DFS = high (AVDD1) for twos complement, DFS = low (ground) for offset binary format.
7	LVDSBIAS	Set Pin for LVDS Output Current. Place 3.7 kΩ resistor terminated to DRGND.
10	SENSE	Reference Mode Selection. Connect to AGND for internal 1 V reference, and connect to AVDD2 for external reference.
11	VREF	1.0 V Reference I/O—Function Dependent on SENSE. Decouple to ground with 0.1 µF and 10 µF capacitors.
12, 15, 20, 23, 32, 86, 88, 96 to 97, 99, Exposed Heat Sink	AGND	Analog Ground. The exposed heat sink on the bottom of the package must be connected to AGND.
13	REFT	Differential Reference Output. Decoupled to ground with 0.1 µF capacitor and to REFB (Pin 14) with 0.1 µF and 10 µF capacitors.
14	REFB	Differential Reference Output. Decoupled to ground with a 0.1 µF capacitor and to REFT (Pin 13) with 0.1 µF and 10 µF capacitors.
19, 28 to 31, 39 to 40	AVDD2	5.0 V Analog Supply (±5%).
21	VIN+	Analog Input—True.
22	VIN−	Analog Input—Complement.
33	C1	Internal Bypass Node. Connect a 0.1 µF capacitor from this pin to AGND.
36	CLK+	Clock Input—True.
37	CLK−	Clock Input—Complement.
43	D0− (LSB)	D0 Complement Output Bit (LVDS Levels).
44	D0+	D0 True Output Bit.
45	D1−	D1 Complement Output Bit.
46	D1+	D1 True Output Bit.
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V).
48, 53, 61, 67, 74, 82	DRGND	Digital Ground.
49	D2−	D2 Complement Output Bit.
50	D2+	D2 True Output Bit.
51	D3−	D3 Complement Output Bit.
52	D3+	D3 True Output Bit.
55	D4−	D4 Complement Output Bit.
56	D4+	D4 True Output Bit.
57	D5−	D5 Complement Output Bit.
58	D5+	D5 True Output Bit.
59	D6−	D6 Complement Output Bit.
60	D6+	D6 True Output Bit.
63	DCO−	Data Clock Output—Complement.
64	DCO+	Data Clock Output—True.
65	D7−	D7 Complement Output Bit.
66	D7+	D7 True Output Bit.
68	D8−	D8 Complement Output Bit.
69	D8+	D8 True Output Bit.
70	D9−	D9 Complement Output Bit.
71	D9+	D9 True Output Bit.
72	D10−	D10 Complement Output Bit.
73	D10+	D10 True Output Bit.
76	D11−	D11 Complement Output Bit.
77	D11+	D11 True Output Bit.
78	D12−	D12 Complement Output Bit.
79	D12+	D12 True Output Bit.
80	D13−	D13 Complement Output.
81	D13+ (MSB)	D13 True Output Bit.
84	OR−	Out-of-Range Complement Output Bit.
85	OR+	Out-of-Range True Output Bit.
100	DCS MODE	Clock Duty Cycle Stabilizer (DCS) Control Pin, CMOS-Compatible. DCS = low (AGND) to enable DCS (recommended). DCS = high (AVDD1) to disable DCS.

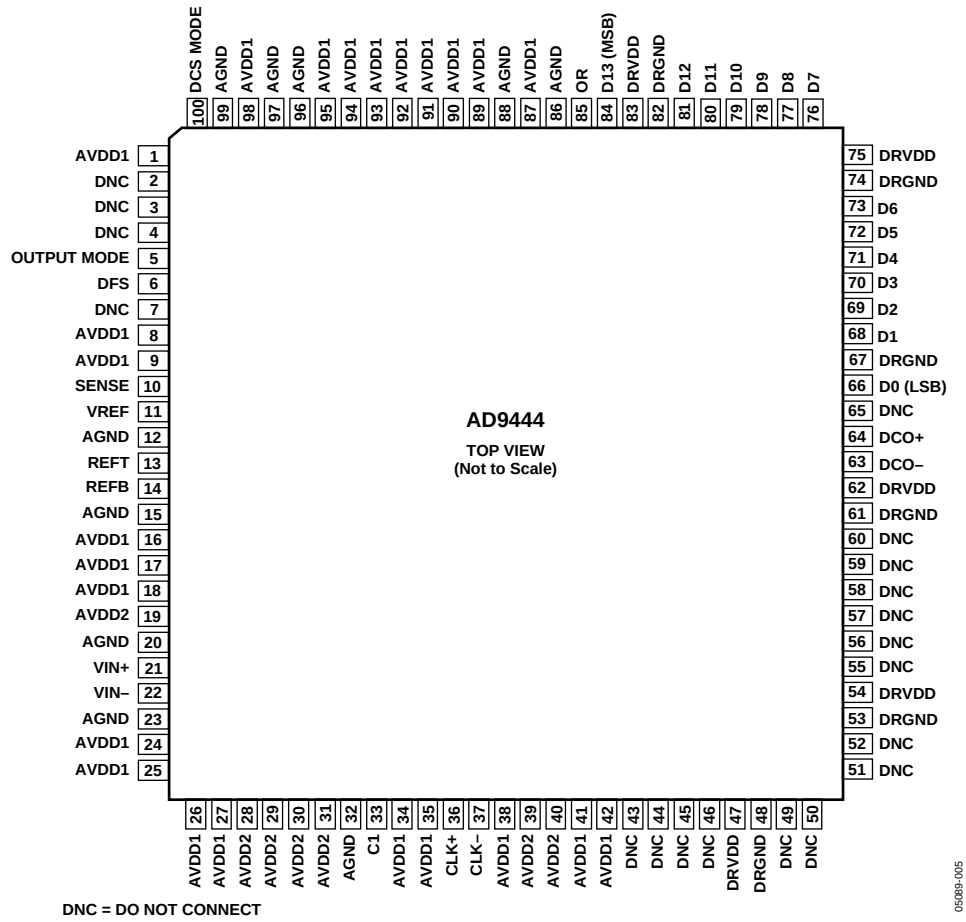


Figure 5. 100-Lead TQFP/EP Pin Configuration in CMOS Mode

Table 8. Pin Function Descriptions—100-Lead TQFP/EP in CMOS Mode

Pin No.	Mnemonic	Description
1, 8 to 9, 16 to 18, 24 to 27, 34 to 35, 38, 41 to 42, 87, 89 to 95, 98	AVDD1	3.3 V (±5%) Analog Supply.
2 to 4, 7, 43 to 46, 49 to 52, 55 to 60, 65	DNC	Do Not Connect. These pins should float.
5	OUTPUT MODE	CMOS Compatible Output Logic Mode Control Pin. OUTPUT MODE = 0 for CMOS mode, and OUTPUT MODE = 1 (AVDD1) for LVDS outputs.
6	DFS	Data Format Select Pin. CMOS control pin that determines the format of the output data. DFS = high (AVDD1) for twos complement, DFS = low (ground) for offset binary format.
10	SENSE	Reference Mode Selection. Connect to AGND for internal 1 V reference, and connect to AVDD2 for external reference.
11	VREF	1.0 V Reference I/O—Function Dependent on SENSE. Decouple to ground with 0.1 µF and 10 µF capacitors.
12, 15, 20, 23, 32, 86, 88, 96 to 97, 99, Exposed Heat Sink	AGND	Analog Ground. The exposed heat sink on the bottom of the package must be connected to AGND.
13	REFT	Differential Reference Output. Decoupled to ground with 0.1 µF capacitor and to REFB (Pin 14) with 0.1 µF and 10 µF capacitors.
14	REFB	Differential Reference Output. Decoupled to ground with a 0.1 µF capacitor and to REFT (Pin 13) with 0.1 µF and 10 µF capacitors.
19, 28 to 31, 39 to 40	AVDD2	5.0 V Analog Supply (±5%).
21	VIN+	Analog Input—True.
22	VIN−	Analog Input—Complement.
33	C1	Internal Bypass Node. Connect a 0.1 µF capacitor from this pin to AGND.
36	CLK+	Clock Input—True.
37	CLK−	Clock Input—Complement.
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (2.5V to 3.6 V).
48, 53, 61, 67, 74, 82	DRGND	Digital Ground.
63	DCO−	Data Clock Output—Complement (CMOS Levels).
64	DCO+	Data Clock Output—True.
66	D0 (LSB)	D0 Output Bit (LSB) (CMOS Levels).
68	D1	D1 Output Bit.
69	D2	D2 Output Bit.
70	D3	D3 Output Bit.
71	D4	D4 Output Bit.
72	D5	D5 Output Bit.
73	D6	D6 Output Bit.
76	D7	D7 Output Bit.
77	D8	D8 Output Bit.
78	D9	D9 Output Bit.
79	D10	D10 Output Bit.
80	D11	D11 Output Bit.
81	D12	D12 Output Bit.
84	D13 (MSB)	D13 Output Bit.
85	OR	Out-of-Range Output.
100	DCS MODE	Clock Duty Cycle Stabilizer (DCS) Control Pin, CMOS-Compatible. DCS = low (AGND) to enable DCS (recommended). DCS = high (AVDD1) to disable DCS.

EQUIVALENT CIRCUITS

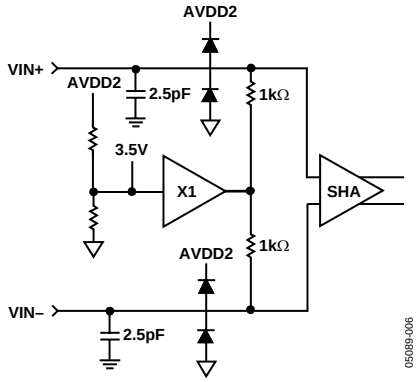


Figure 6. Equivalent Analog Input Circuit

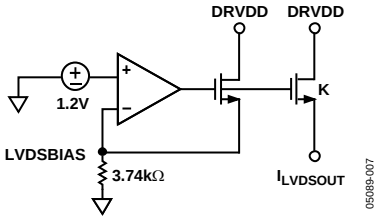


Figure 7. Equivalent LVDS BIAS Circuit

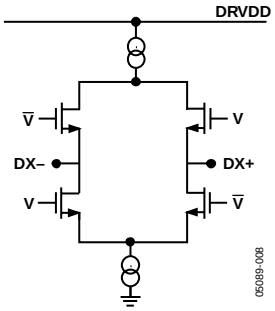


Figure 8. Equivalent LVDS Digital Output Circuit

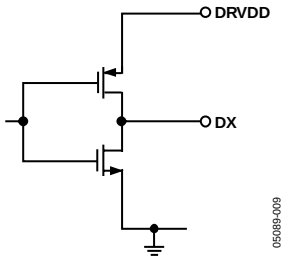


Figure 9. Equivalent CMOS Digital Output Circuit

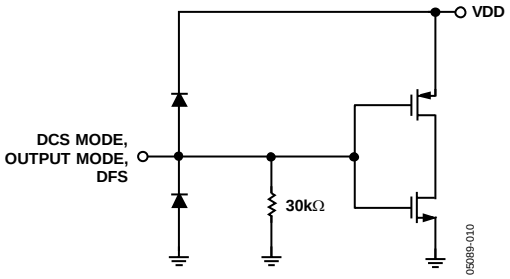


Figure 10. Equivalent Digital Input Circuit, DFS, DCS MODE, OUTPUT MODE

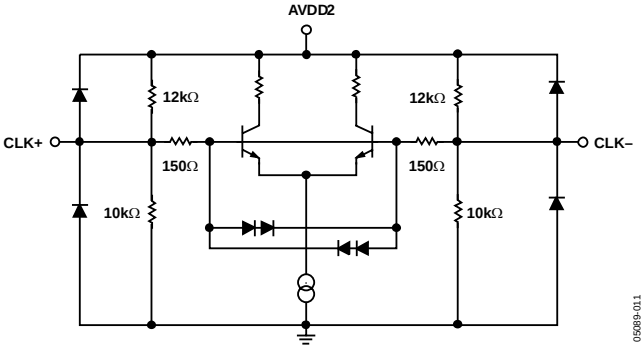


Figure 11. Equivalent Sample Clock Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 3.3 V, AVDD2 = 5.0 V, DRVDD = 3.3 V, sample rate = 80 MSPS, LVDS mode, DCS enabled, T_A = 25°C, 2 V p-p differential input, AIN = −0.5 dBFS, internal trimmed reference (nominal VREF = 1.0 V), unless otherwise noted.

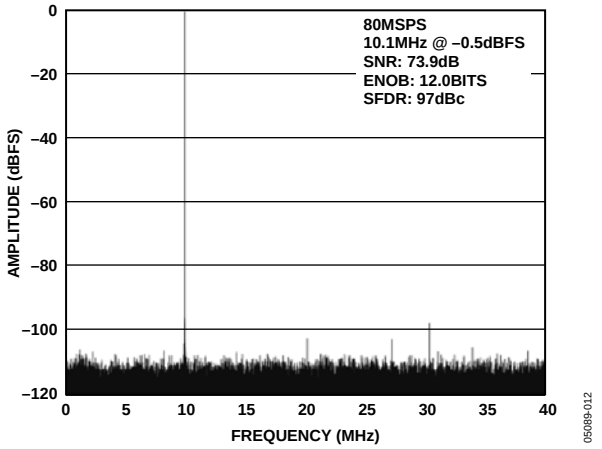


Figure 12. 64K Point Single-Tone FFT/80 MSPS/10.1 MHz

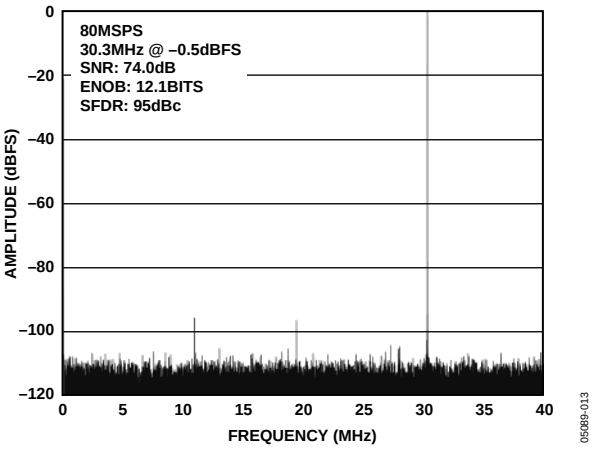


Figure 13. 64K Point Single-Tone FFT/80 MSPS/30.3 MHz

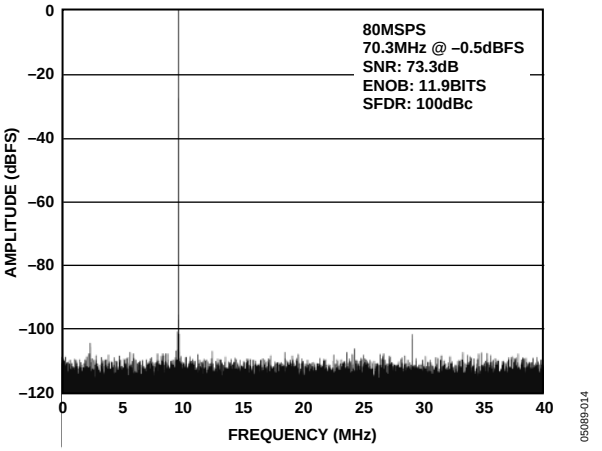


Figure 14. 64K Point Single-Tone FFT/80 MSPS/70 MHz

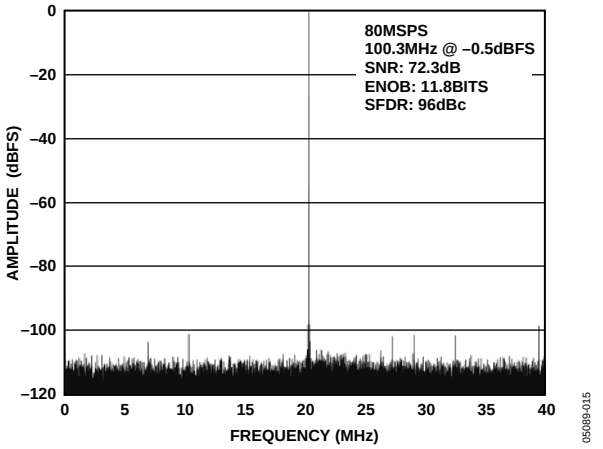


Figure 15. 64K Point Single-Tone FFT/80 MSPS/100 MHz

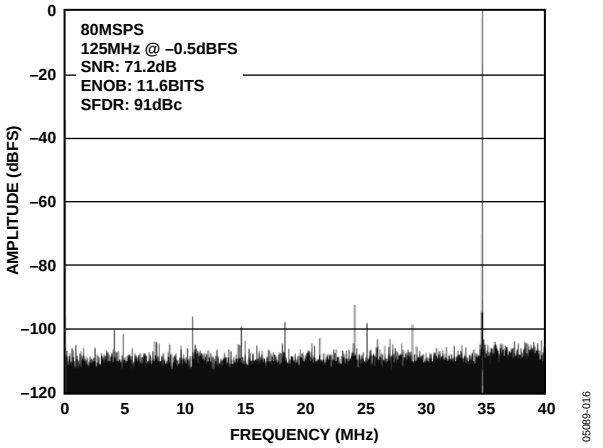


Figure 16. 64K Point Single-Tone FFT/80 MSPS/125 MHz

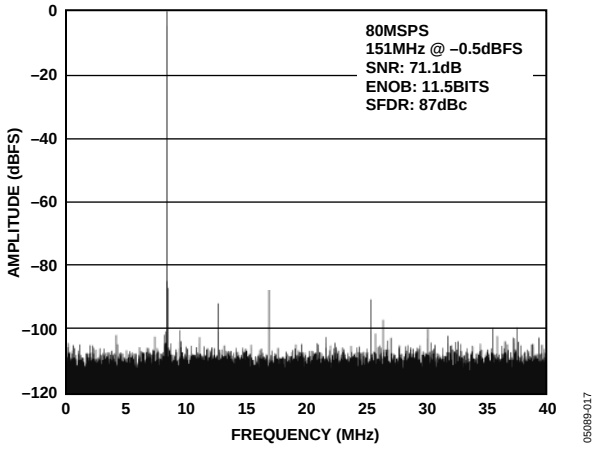


Figure 17. 64K Point Single-Tone FFT/80 MSPS/151 MHz

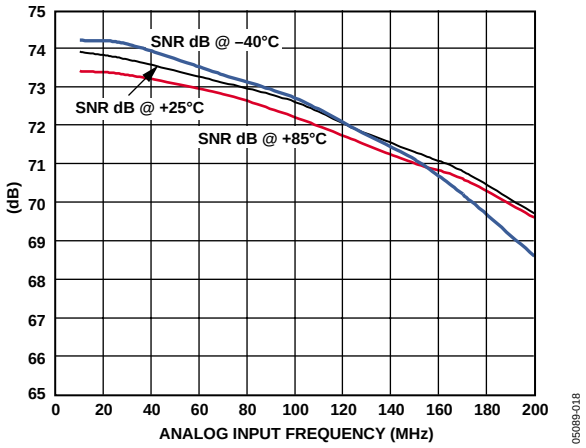


Figure 18. SNR vs. Analog Input Frequency, 80 MSPS/LVDS Mode

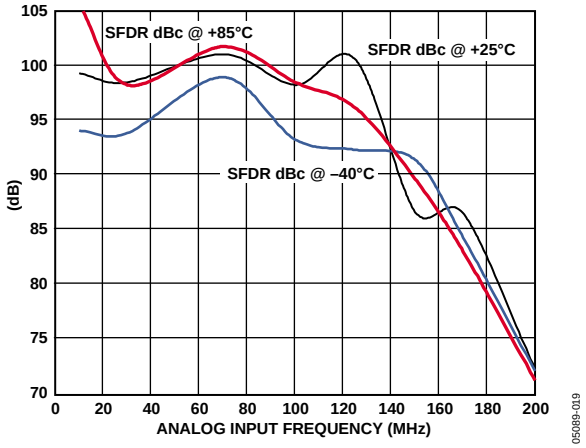


Figure 19. SFDR vs. Analog Input Frequency, 80 MSPS/LVDS Mode

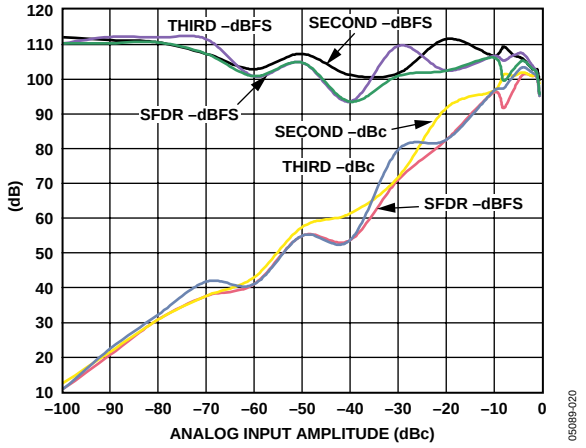


Figure 20. Single-Tone SFDR/Second/Third vs. Analog Input Level, 80 MSPS, A_{IN} = 30.3 MHz

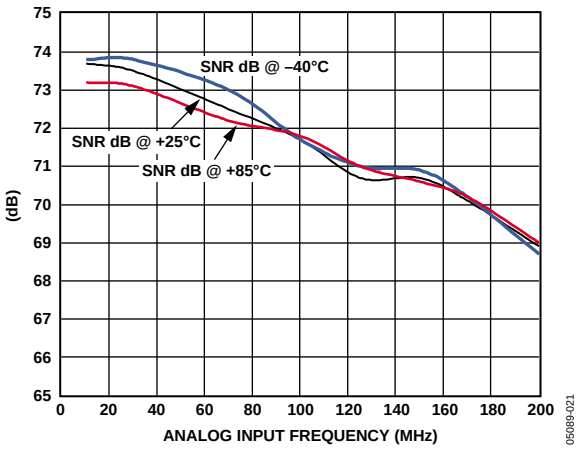


Figure 21. SNR vs. Analog Input Frequency, 80 MSPS/CMOS Mode

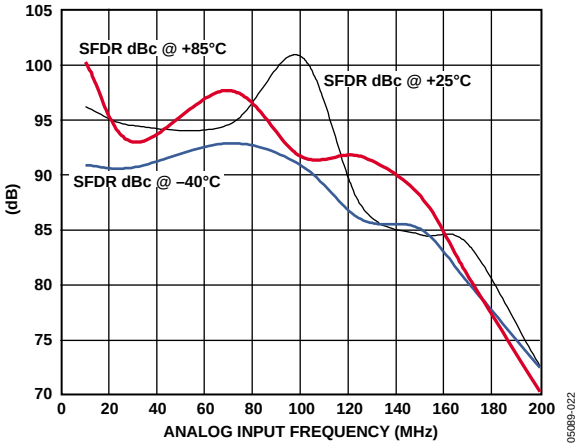


Figure 22. SFDR vs. Analog Input Frequency, 80 MSPS/CMOS Mode

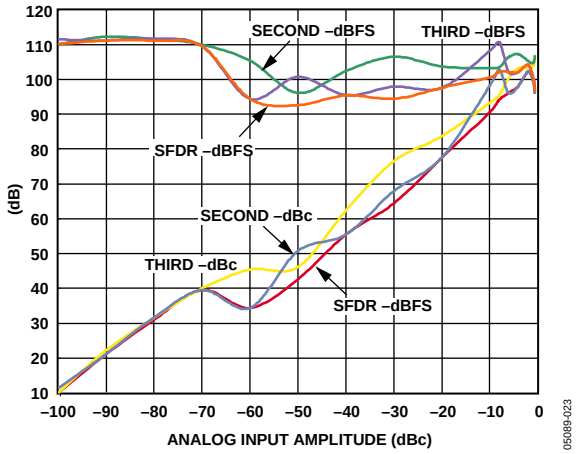


Figure 23. Single-Tone SFDR/Second/Third vs. Analog Input Level 80 MSPS, A_{IN} = 70.30 MHz

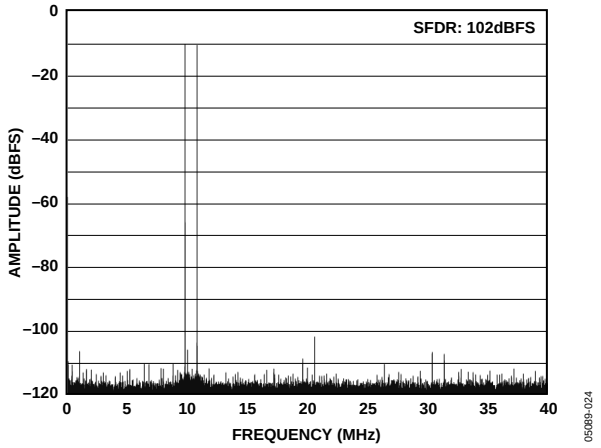


Figure 24. 32K Point Two-Tone FFT 80 MSPS/9.8 MHz/10.8 MHz

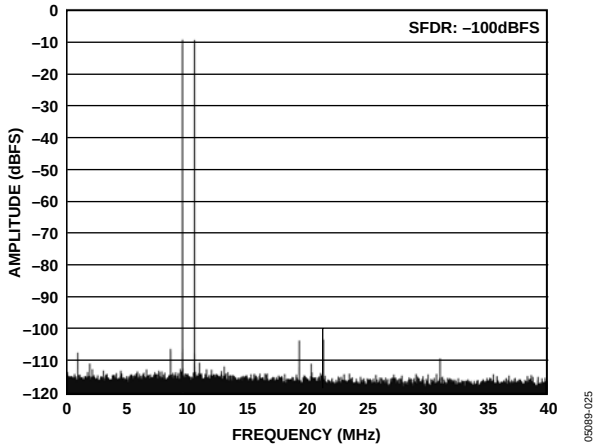


Figure 25. 32K Point Two-Tone FFT 80 MSPS/69.3 MHz/70.3 MHz

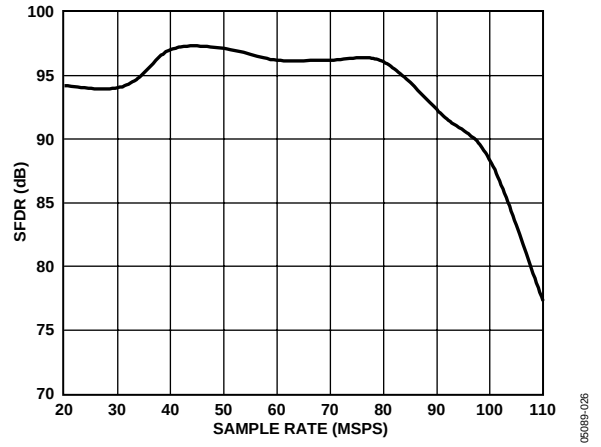


Figure 26. SFDR vs. Sample Rate, V_{IN} = 10.3 MHz @ –0.5 dBFS

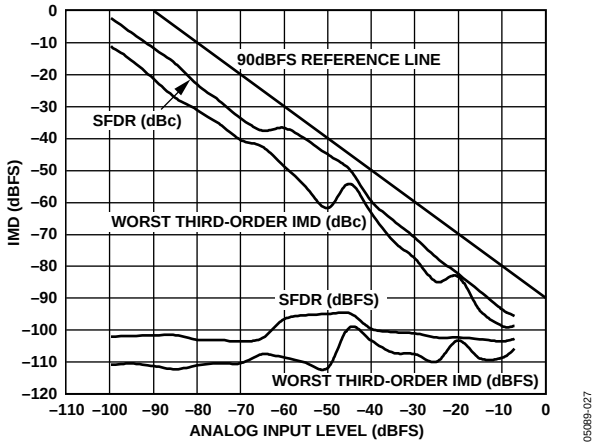


Figure 27. Two-Tone SFDR vs. Analog Input Level, A_{IN} = 9.8 MHz/10.8 MHz

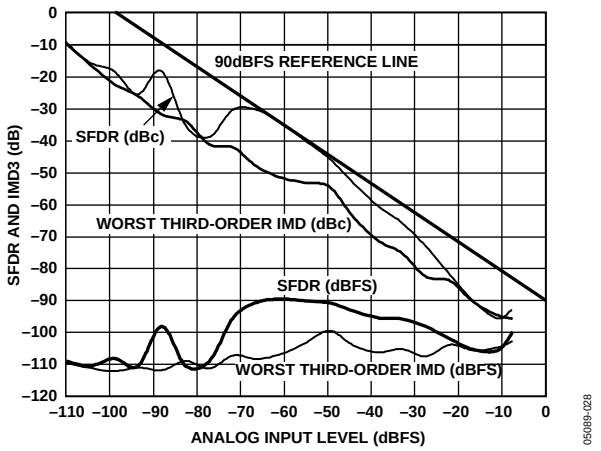


Figure 28. Two-Tone SFDR vs. Analog Input Level, A_{IN} = 69.3 MHz/70.3 MHz

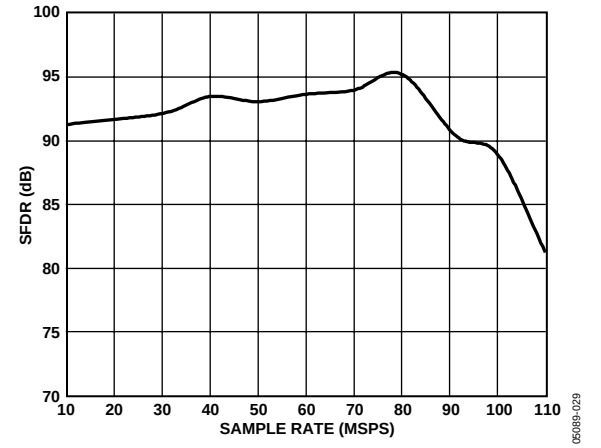


Figure 29. SFDR vs. Sample Rate, V_{IN} = 70.3 MHz @ –0.5 dBFS

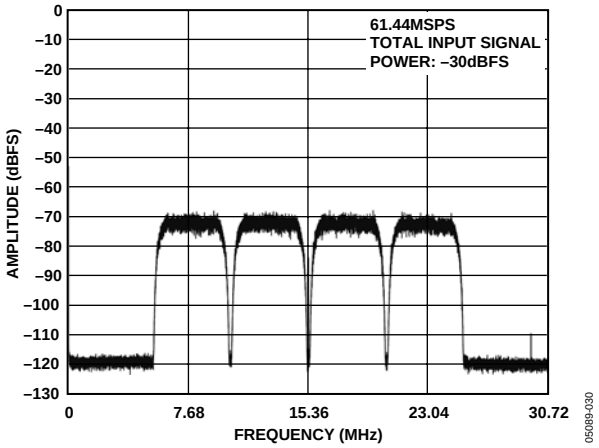


Figure 30. 64K FFT, 61.44 MSPS, 4 @ WCDMA, IF = 46.08 MHz

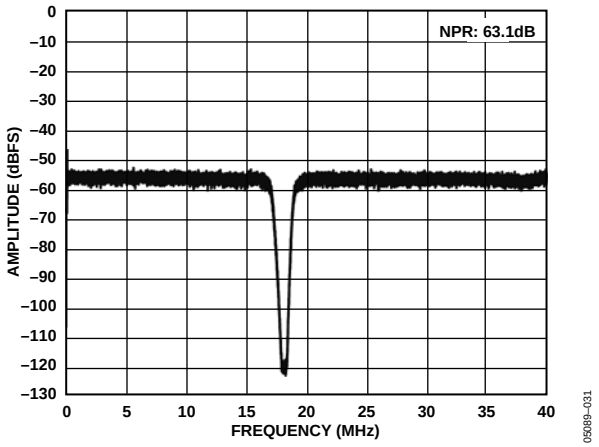


Figure 31. NPR, 80 MSPS/18 MHz Notch

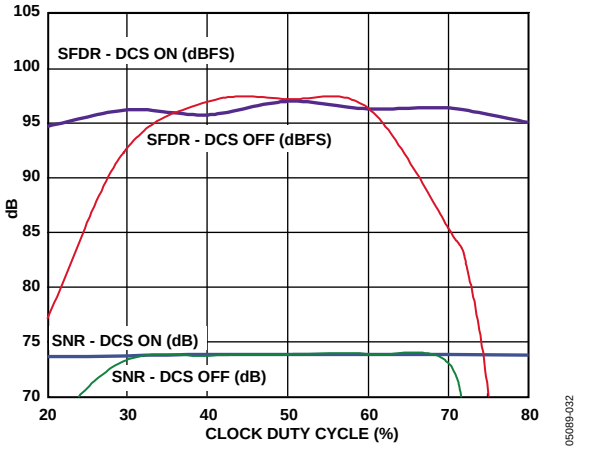


Figure 32. Single-Tone SNR/SFDR vs. Clock Duty Cycle, F_{SAMPLE} = 80 MSPS, 10.3 MHz @ –0.5 dBFS

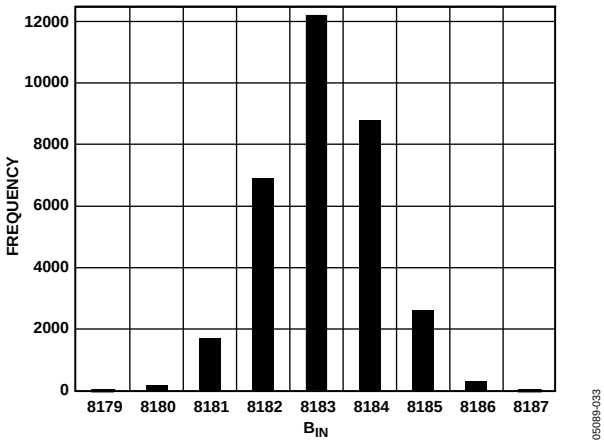


Figure 33. Ground Input Histogram
80 MSPS, VIN+ = VIN–, 32K Samples

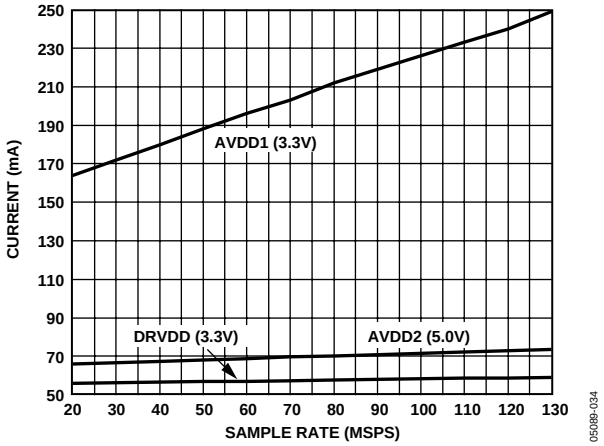


Figure 34. I_{SUPPLY} vs. Sample Rate, A_{IN} = 10.3 MHz @ –0.5 dBFS

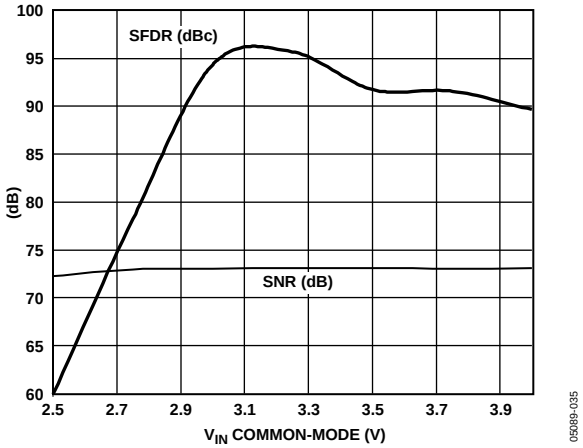


Figure 35. Single-Tone SNR/SFDR vs.
V_{IN} Common-Mode Voltage 80 MSPS/10.3 MHz

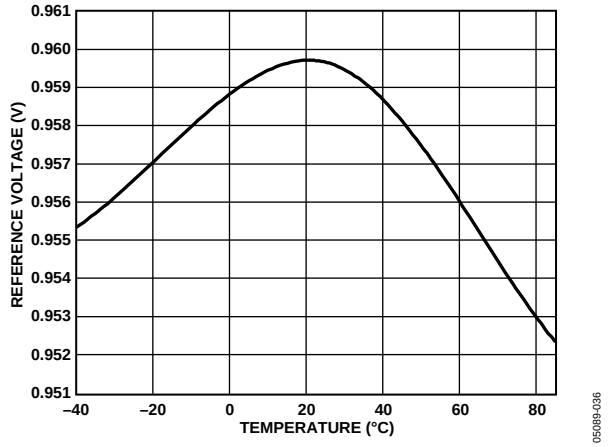


Figure 36. VREF vs. Temperature

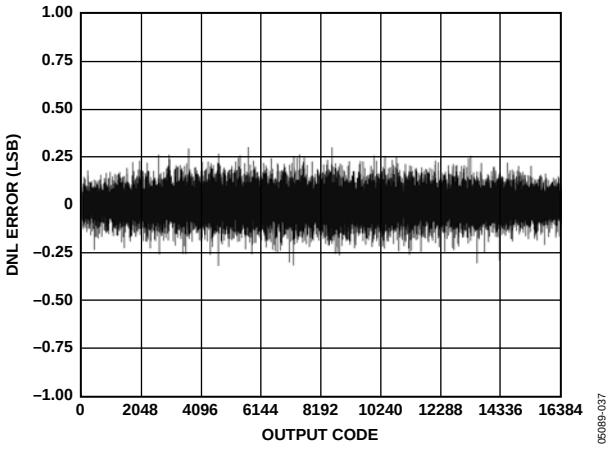


Figure 37. DNL Error vs. Output Code, 80 MSPS, A_{IN} = 15 MHz

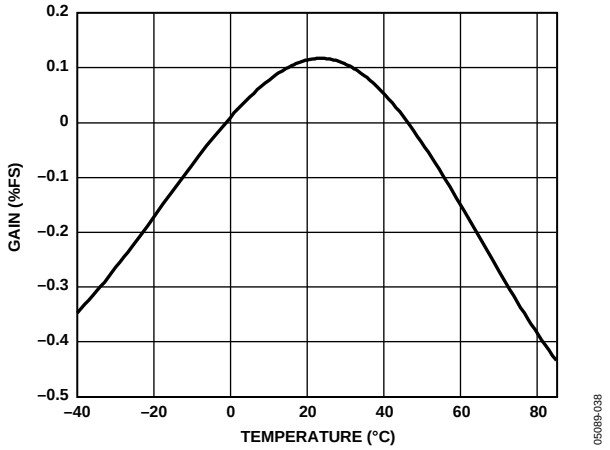


Figure 38. Gain vs. Temperature

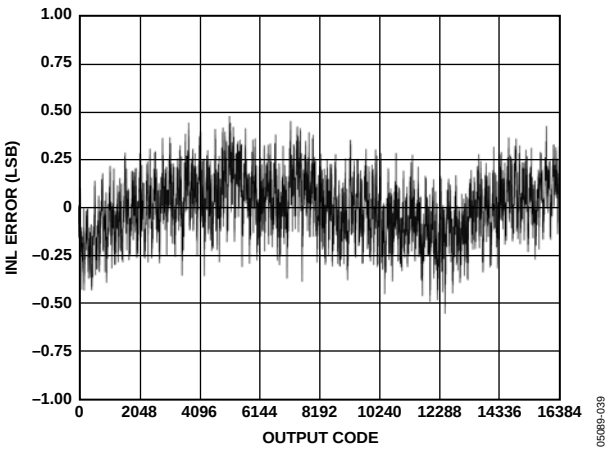


Figure 39. INL Error vs. Output Code, 80 MSPS, A_{IN} = 15 MHz

THEORY OF OPERATION

The AD9444 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated, high bandwidth, track-and-hold circuit that samples the signal prior to quantization by the 14-bit pipeline ADC core. The device includes an on-board reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output logic levels are user selectable as standard 3 V CMOS or LVDS (ANSI-644 compatible) via the OUTPUT MODE pin.

ANALOG INPUT AND REFERENCE OVERVIEW

A stable and accurate 0.5 V voltage reference is built into the AD9444. The input range can be adjusted by varying the reference voltage applied to the AD9444, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are described in the next few sections.

Internal Reference Connection

A comparator within the AD9444 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 40), setting VREF to ~1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a ~0.5 V reference output. If a resistor divider is connected, as shown in Figure 41, the switch again sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

Internal Reference Trim

The internal reference voltage is trimmed during the production test to adjust the gain (analog input voltage range) of the AD9444. Therefore, there is little advantage to the user supplying an external voltage reference to the AD9444. The gain trim is performed with the AD9444's input range set to 2 V p-p nominal (SENSE connected to AGND). Because of this trim, and because the 2 V p-p analog input range provides maximum ac performance, there is little benefit to using analog input ranges < 2 V p-p. Users are cautioned that the differential nonlinearity of the ADC varies with the reference voltage. Configurations that use < 2 V p-p may exhibit missing codes and, therefore, degraded noise and distortion performance.

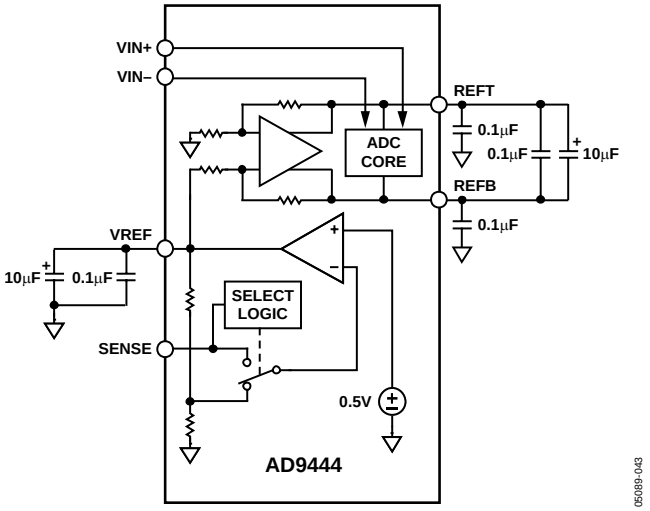


Figure 40. Internal Reference Configuration

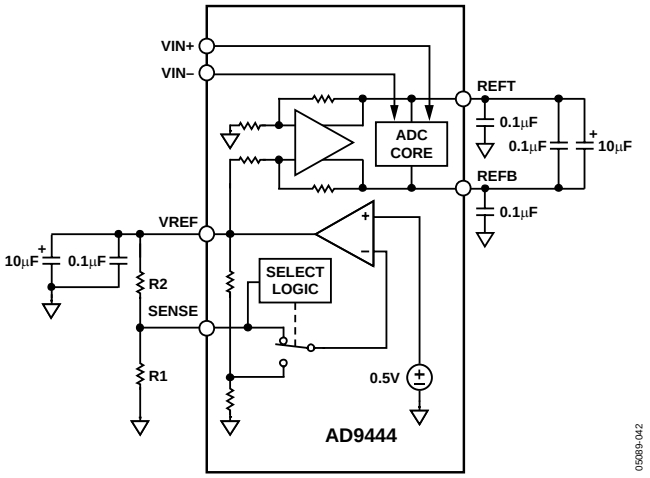


Figure 41. Programmable Reference Configuration

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	$0.5 \times \left(1 + \frac{R2}{R1}\right)$ (See Figure 41)	2 × VREF
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

External Reference Operation

The AD9444's internal reference is trimmed to enhance the gain accuracy of the ADC. An external reference may be more stable over temperature, but the gain of the ADC is not likely to be improved. Figure 36 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

Analog Inputs

As with most new high speed, high dynamic range ADCs, the analog input to the AD9444 is differential. Differential inputs improve on-chip performance as signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even-order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection of stray signals, such as ground and power noise. Second, they provide good rejection of common-mode signals, such as local oscillator feedthrough. The specified noise and distortion of the AD9444 cannot be realized with a single-ended analog input, so such configurations are discouraged. Contact ADI for recommendations of other 14-bit ADCs that support single-ended analog input configurations.

With the 1 V reference (nominal value, see the Internal Reference Trim section), the differential input range of the AD9444's analog input is nominally 2 V p-p or 1 V p-p on each input (VIN+ or VIN−).

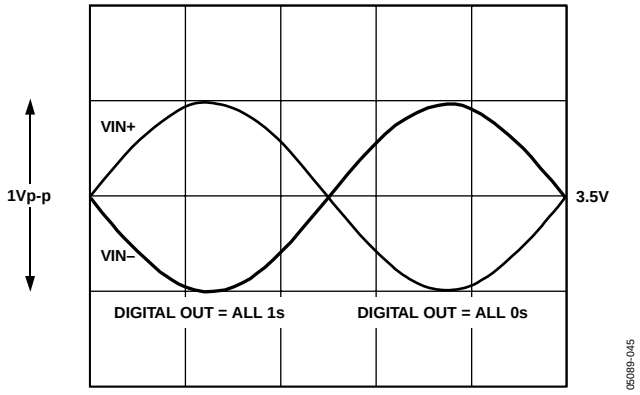


Figure 42. Differential Analog Input Range for VREF = 1 V

The AD9444 analog input voltage range is offset from ground by 3.5 V. Each analog input connects through a 1 kΩ resistor to the 3.5 V bias voltage and to the input of a differential buffer. The internal bias network on the input properly biases the buffer for maximum linearity and range (see the Equivalent Circuits section). Therefore, the analog source driving the AD9444 should be ac-coupled to the input pins. The recommended method for driving the analog input of the AD9444 is to use an RF transformer to convert single-ended signals to differential (see Figure 44). Series resistors between the output of the transformer and the AD9444 analog inputs help isolate the analog input source from switching transients caused by the internal sample-and-hold circuit. The series resistors, along with the 1 kΩ resisters connected to the internal 3.5 V bias, must be considered in impedance matching the transformers input. For example, if R_T were set to 51 Ω and R_S were set to 33 Ω, along with a 1:1 impedance ratio transformer, the input would match a 50 Ω source with a full-scale drive of 10.0 dBm. The 50 Ω impedance matching can also be incorporated on the secondary side of the transformer, as shown in the evaluation board schematic (see Figure 47 and Figure 59).

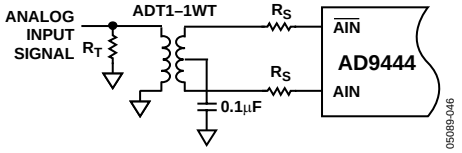


Figure 43. Transformer-Coupled Analog Input Circuit

CLOCK INPUT CONSIDERATIONS

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. For that reason, considerable care was taken in the design of the clock inputs of the AD9444, and the user is advised to give careful thought to the clock source.

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to the clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9444 contains a clock duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. As shown in Figure 32, noise and distortion performance are nearly flat for a 30% to 70% duty cycle with the DCS enabled. The DCS circuit locks to the rising edge of CLK+ and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 30 MHz nominally. The loop has a time constant associated with it that needs to be considered in applications where the clock rate can change dynamically, which requires a wait time of 1.5 µs to 5 µs after a dynamic clock frequency increase (or decrease) before the DCS loop is relocked to the input signal. During the time period the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependant on the duty cycle of the input clock signal. In such an application, it may appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

The DCS circuit is controlled by the DCS MODE pin; a CMOS logic low (AGND) on DCS MODE enables the duty cycle stabilizer, and logic high (AVDD1 = 3.3 V) disables the controller.

The AD9444 input sample clock signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on the encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 70 MHz analog input signals when using a high jitter clock source. (See AN-501, Aperture Uncertainty and ADC System Performance, for complete details.) For optimum performance, the AD9444 must be clocked differentially. The sample clock inputs are internally biased to ~2.2 V, and the input signal is usually ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. Figure 44 shows one preferred method for clocking the AD9444. The clock source (low jitter) is converted from single-ended-to-differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9444 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9444 and limits the noise presented to the sample clock inputs.

If a low jitter clock is available, another option is to ac couple a differential ECL/PECL signal to the encode input pins, as shown in Figure 46.

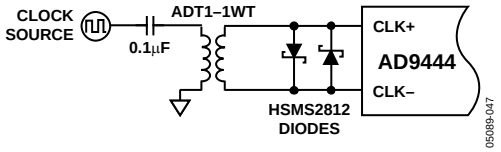


Figure 44. Crystal Clock Oscillator, Differential Encode

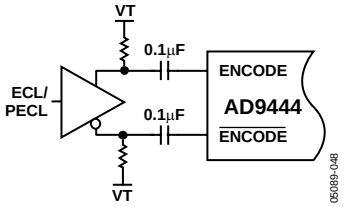


Figure 45. Differential ECL for Encode

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) and rms amplitude due only to aperture jitter (t_J) can be calculated using the following equation.

$$SNR = 20 \log[2\pi f_{INPUT} \times t_J]$$

In the equation, the rms aperture jitter represents the root-mean square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, see Figure 46.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9444. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

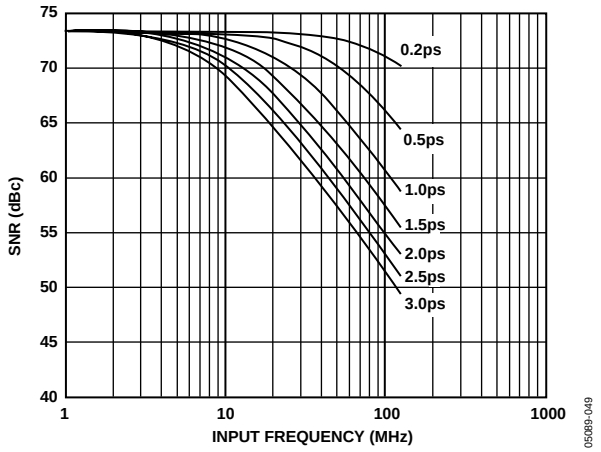


Figure 46. SNR vs. Input Frequency and Jitter

POWER CONSIDERATIONS

Care should be taken when selecting a power source. The use of linear dc supplies is highly recommended. Switching supplies tend to have radiated components that may be received by the AD9444. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD9444 has separate digital and analog power supply pins. The analog supplies are denoted AVDD1 (3.3 V) and AVDD2 (5 V) and the digital supply pins are denoted DRVDD. Although the AVDD1 and DRVDD supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that both AVDD1 and AVDD2 must be held within 5% of the specified voltage.

The DRVDD supply of the AD9444 is a dedicated supply for the digital outputs, in either LVDS or CMOS output modes. When in LVDS mode, the DRVDD should be set to 3.3 V. In CMOS mode, the DRVDD supply may be connected from 2.5 V to 3.6 V to be compatible with the receiving logic.

DIGITAL OUTPUTS

LVDS Mode

The off-chip drivers on the chip can be configured to provide LVDS-compatible output levels via Pin 5 (OUTPUT MODE). LVDS outputs are available when OUTPUT MODE is CMOS logic high (or AVDD1 for convenience) and a 3.74 kΩ R_{SET} resistor is placed at Pin 7 (LVDSBIAS) to ground. Dynamic performance, including both SFDR and SNR, is maximized when the AD9444 is used in LVDS mode, and designers are encouraged to take advantage of this mode. The AD9444 outputs include complimentary LVDS outputs for each data bit (DX+/DX−), the overrange output (OR+/OR−), and the output data clock output (DCO+/DCO−). The R_{SET} resistor current is ratioed on-chip, setting the output current at each output equal to a nominal 3.5 mA ($11 \times I_{R_{SET}}$). A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. LVDS mode facilitates interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor as close to the receiver as possible. It is recommended to keep the trace length less than 1 inch to 2 inches and to keep differential output trace lengths as equal as possible.

CMOS Mode

In applications that can tolerate a slight degradation in dynamic performance, the AD9444 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. CMOS outputs are available when OUTPUT MODE is CMOS logic low (or AGND for convenience). In this mode, the output data bits are single-ended CMOS, DX, as is the overrange output, OR. The output clock is provided as a differential CMOS signal, DCO+/DCO−. Lower supply voltages are recommended to avoid coupling switching transients back to the sensitive analog sections of the ADC. The capacitive load to the CMOS outputs should be minimized, and each output should be connected to a single gate through a series resistor (220 Ω) to minimize switching transients caused by the capacitive loading.

TIMING

The AD9444 provides latched data outputs with a pipeline delay of 12 clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of CLK+. Refer to Figure 2 and Figure 3 for detailed timing diagrams.

OPERATIONAL MODE SELECTION

Data Format Select

The data format select (DFS) pin of the AD9444 determines the coding format of the output data. This pin is 3.3 V CMOS compatible, with logic high (or AVDD1, 3.3 V) selecting twos complement, and DFS logic low (AGND) selecting offset binary format. Table 10 summarizes the output coding.

Output Mode Select

The OUPUT MODE pin controls the logic compatibility, as well as the pinout of the digital outputs. This pin is a CMOS compatible input. With OUTPUT MODE = 0 (AGND), the AD9444 outputs are CMOS-compatible and the pin assignment for the device is defined in Table 8. With OUTPUT MODE = 1 (AVDD1, 3.3 V), the AD9444 outputs are LVDS-compatible and the pin assignment for the device is defined in Table 7.

Duty Cycle Stabilizer

The DCS circuit is controlled by the DCS MODE pin; a CMOS logic low (AGND) on DCS MODE enables the DCS, and logic high (AVDD1, 3.3 V) disables the controller.

Table 10. Digital Output Coding

Code	VIN+ − VIN− Input Span = 2 V p-p (V)	VIN+ − VIN− Input Span = 1 V p-p (V)	Digital Output Offset Binary (D9•••••D0)	Digital Output Twos Complement (D9•••••D0)
16383	1.000	0.500	11 1111 1111 1111	01 1111 1111 1111
8192	0	0	10 0000 0000 0000	00 0000 0000 0000
8191	−0.000122	−0.000061	01 1111 1111 1111	11 1111 1111 1111
0	−1.00	−0.5000	00 0000 0000 0000	10 0000 0000 0000

EVALUATION BOARD

Evaluation boards are offered to configure the AD9444 in either CMOS or LVDS mode. Each represents a recommended configuration for using the device over a wide range of sample rates and analog input frequencies. These evaluation boards provide all the support circuitry required to operate the ADC in its various modes and configurations. Complete schematics and layout plots follow and demonstrate the proper routing and grounding techniques that should be applied at the system level.

It is critical that signal sources with very low phase noise (< 1 ps rms jitter) be used to realize the ultimate performance of the converter. Proper filtering of the input signal, to remove harmonics and lower the integrated noise at the input, is also necessary to achieve the specified noise performance.

The evaluation boards are shipped with an ac to 6 V dc power supply. The evaluation boards include low dropout regulators to generate the various dc supplies required by the AD9444 and its support circuitry. Separate power supplies are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (see Figure 47 to Figure 50 and Figure 59 to Figure 61).

Both the LVDS and CMOS versions of the evaluation board are compatible with the high speed ADC FIFO evaluation kit (part number HSC-ADC-EVALA-SC). The kit includes a high speed data capture board that provides a hardware solution for capturing up to 32Ksamples of high speed ADC output data in a FIFO memory chip (user upgradeable to 256K samples). Software is provided to enable the user to download the captured data to a PC via the USB port. This software also includes a behavioral model of the AD9444 and many other high speed ADCs.

Behavioral modeling of the AD9444 is also available at www.analog.com/ADIsimADC. The ADIsimADC™ software supports virtual ADC evaluation using ADI proprietary behavioral modeling technology. This allows rapid comparison between the AD9444 and other high speed ADCs, with or without hardware evaluation boards.

The AD9444 LVDS evaluation board includes an on-board, LVDS-to-CMOS translator, but the user may choose to remove the translator and terminations to access the LVDS outputs directly.

The CMOS evaluation board includes a buffer for the output data and the DCO output clock of the AD9444.

LVDS EVALUATION BOARD SCHEMATICS

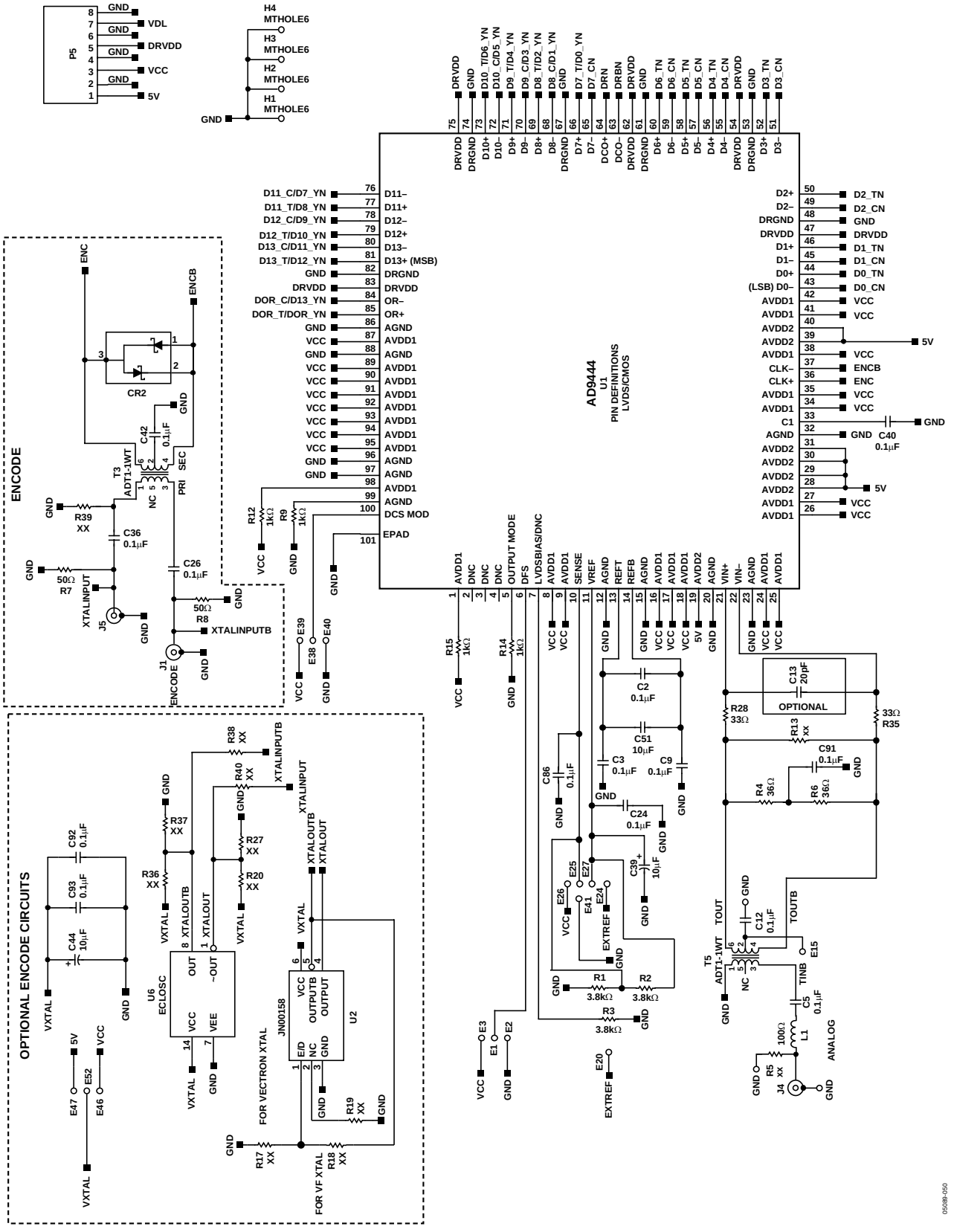


Figure 47. LVDS Mode Evaluation Board Schematic

POWER OPTIONS

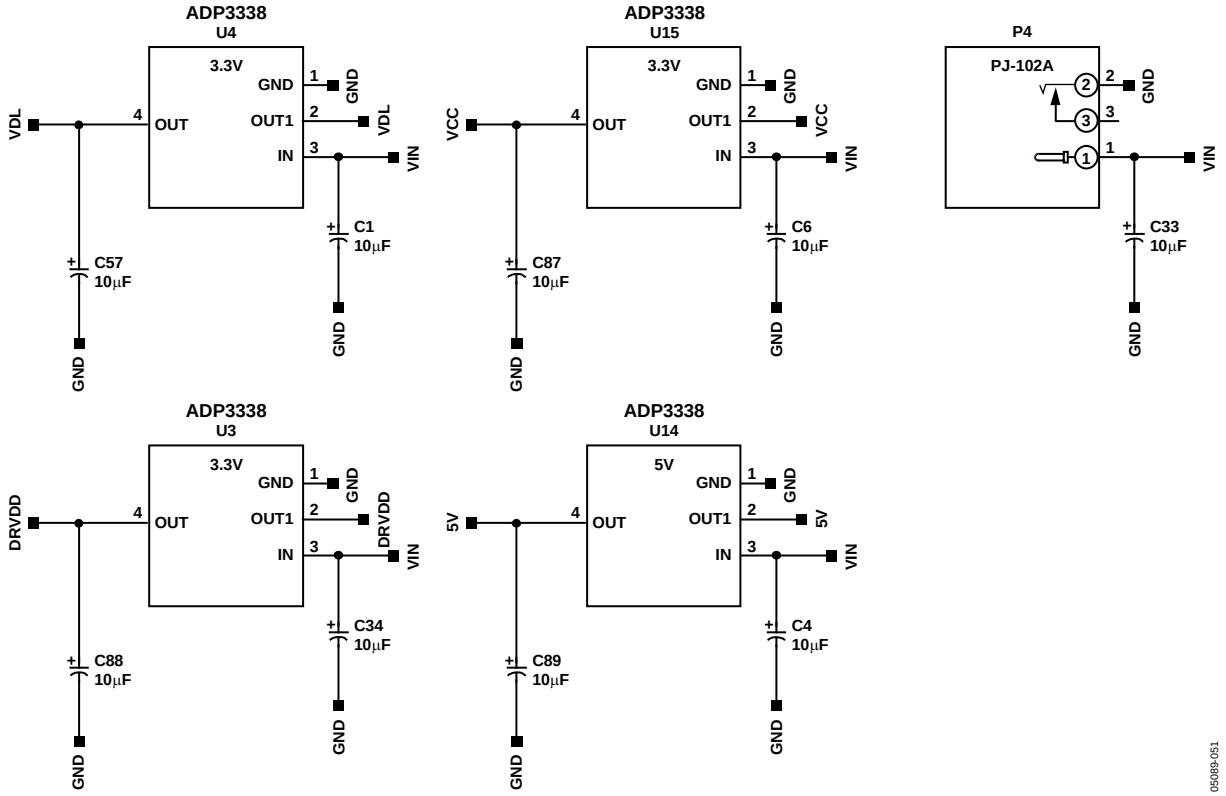


Figure 48. LVDS Mode Evaluation Board Schematic (Continued)

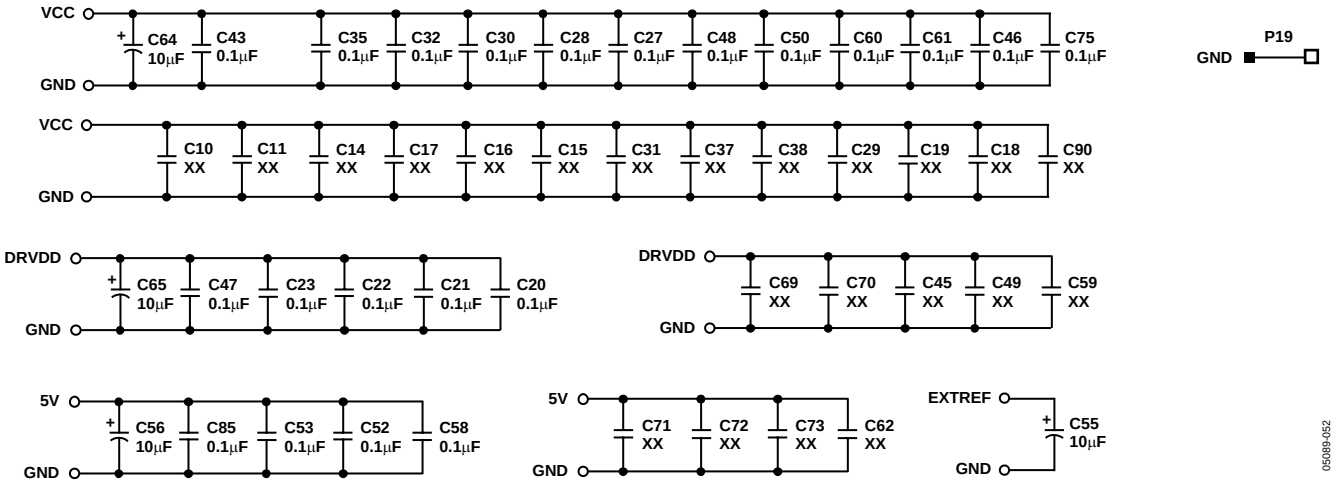


Figure 49. LVDS Mode Evaluation Board Schematic (Continued)

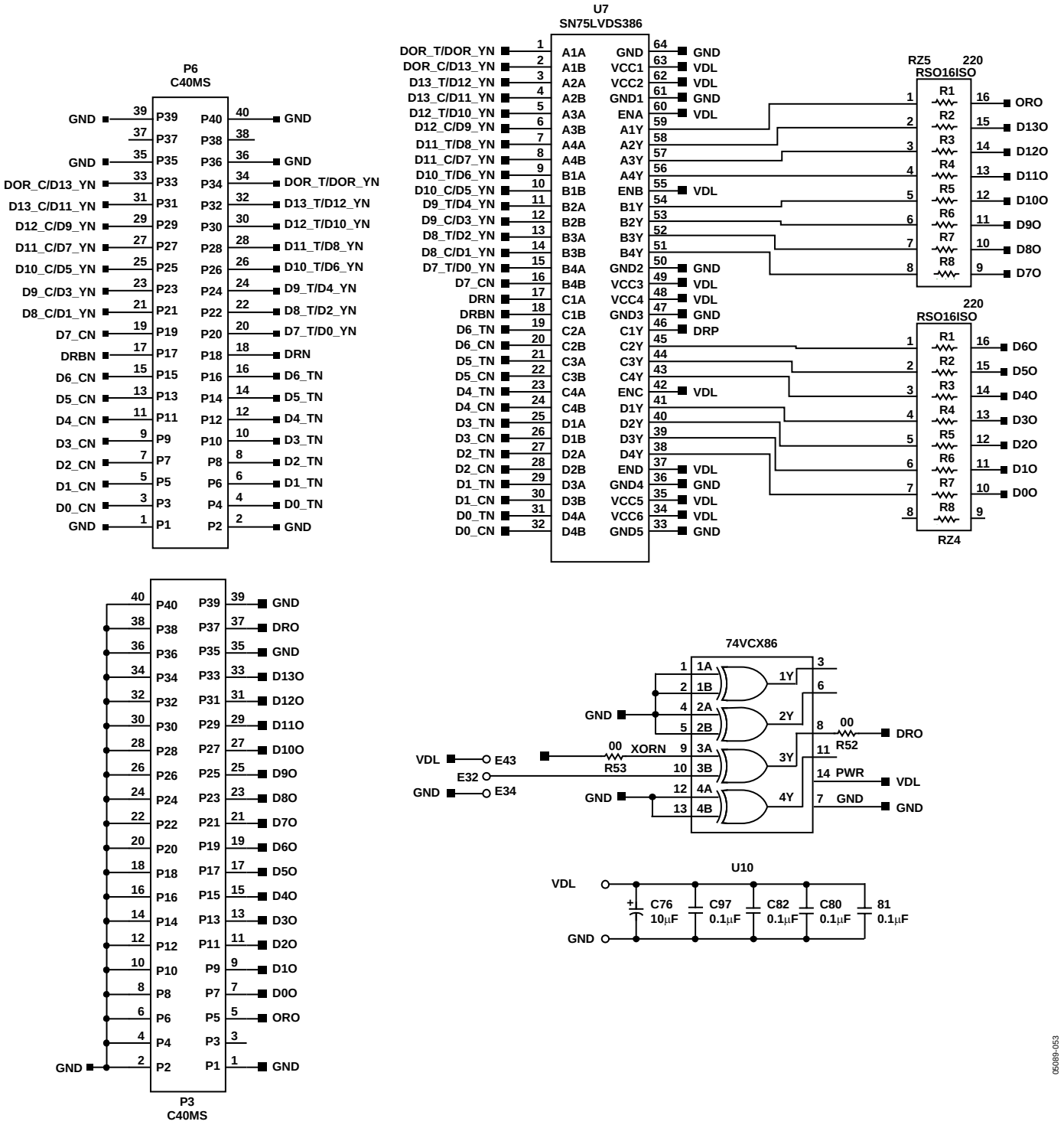


Figure 50. LVDS Mode Evaluation Board Schematic (Continued)

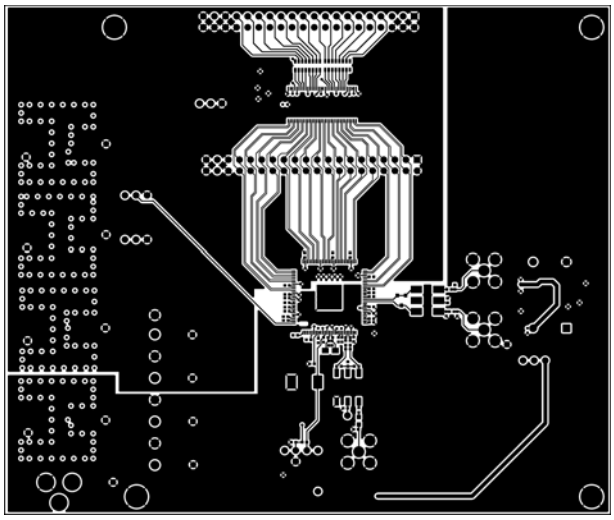


Figure 51. LVDS Mode Evaluation Board Layout, Primary Side

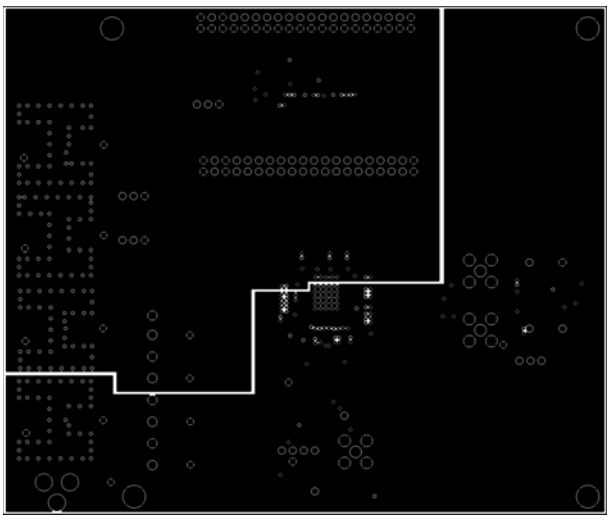


Figure 54. LVDS Mode Evaluation Board Layout, Ground Plane 2

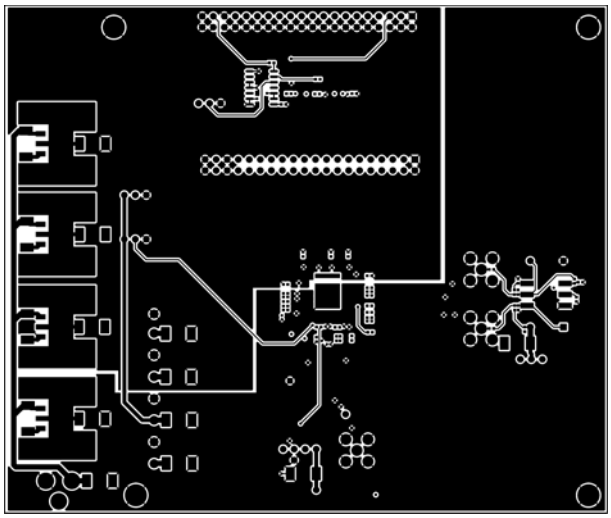


Figure 52. LVDS Mode Evaluation Board Layout, Secondary Side

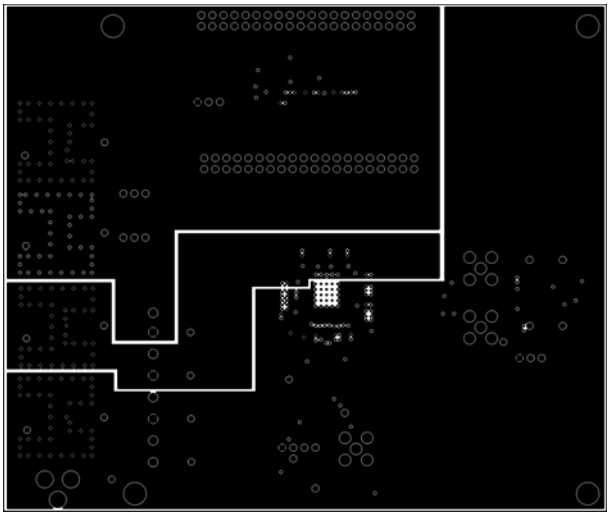


Figure 55. LVDS Mode Evaluation Board Layout, Power Plane 1

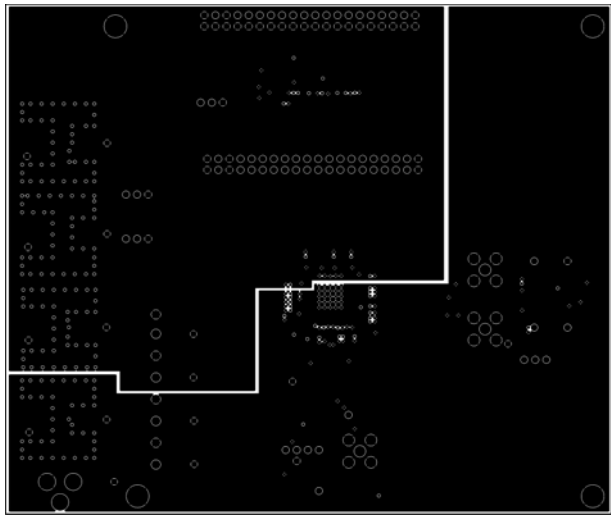


Figure 53. LVDS Mode Evaluation Board Layout, Ground Plane 1

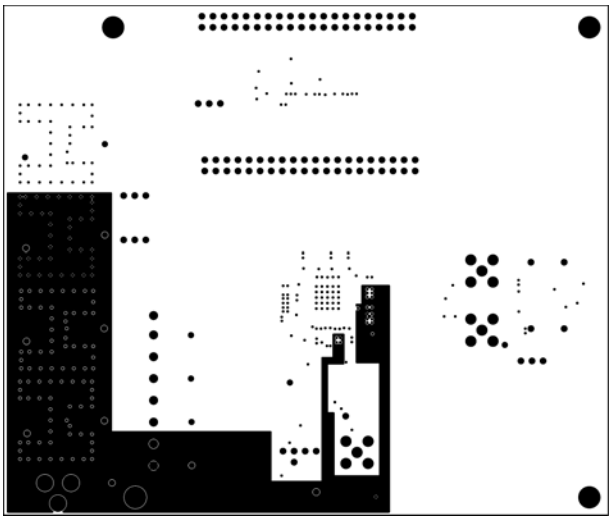


Figure 56. LVDS Mode Evaluation Board Layout, Power Plane 2

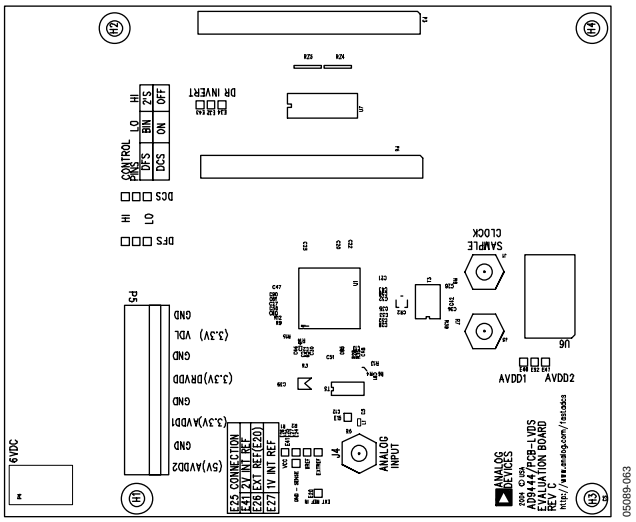


Figure 57. LVDS Mode Evaluation Board Layout, Primary Silkscreen

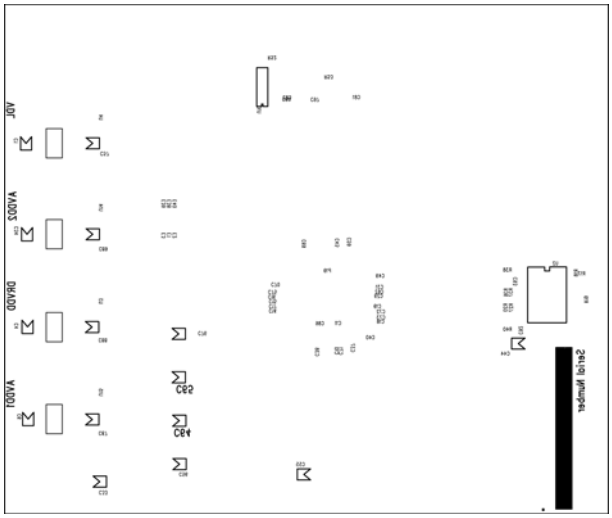


Figure 58. LVDS Mode Evaluation Board Layout, Secondary Silkscreen

LVDS MODE EVALUATION BOARD BILL OF MATERIALS (BOM)

Table 11.

Item	Qty.	REFDES	Description	Manufacturer	MFG_PART_NO
1	1	AD9444PCB	PCB, AD9444 LVDS Engineering Evaluation Board	PCSM	AD9444LVDSCUSTREVC
2	16	C1, C4, C6, C33, C34, C39, C44, C55 to C57, C64, C65, C76, C87 to C89	Capacitors, Tantalum, SMT BCAPTAJC, 10 µF, 16 V, 10%	KEMET	T491C106K016AS
3	38	C2, C3, C5, C9, C12, C20 to C24, C26 to C28, C30, C32, C35, C40, C42, C43, C46 to C48, C50, C52, C53, C58, C60, C61, C75, C80 to C82, C85, C86, C91 to C93, C97	Capacitors, 0.1 µF 10 V Ceramic X5R 0402	Panasonic	ECJ-0EB1A104K
4	1	C51	Capacitor, Ceramic 10 µF 6.3 V X5R 0805	KEMET	C0805C106K9PACTU
5	1	CR2	Diode, Dual Schottky HSMS2812, SOT-23, 30 V, 20 mA	Panasonic	MA716-(TX)
6	17	E1 to E3, E24, to E27, E32, E34, E38, E39, E40, E41, E43, E46, E47, E52	40-Pin Breakable Header	3M	2340-611TN
7	2	J1, J4	Connector, Gold, Male, Coaxial, SMA, Vertical	Johnston Comp.	142-0701-201
8	1	L1	10 nH Inductor	Coilcraft	0603CJ-10NXGBU
9	1	P3	Header, 40-Pin, Male, 40-Pin Right Angle	Samtec	TSW-120-08-T-D-RA
10	1	P4	Power Jack	Swithcraft	RAPC722
11	1	R3	Resistor, 3.6 kΩ 1/16 W 1% 0402 SMD	Panasonic	ERJ-2GEJ362X
12	2	R4, R6	Resistor, 36 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GEJ360X
13	1	R8	Resistor, 49.9 Ω 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF49R9X
14	4	R9, R12, R14, R15	Resistor, 1.00 kΩ 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF1001X
15	2	R28, R35	Resistor, 33 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GEJ330X
16	3	R39, R52, R53	Resistor, 0 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GE0R00X
17	2	RZ4, RZ5	22 Ω Resistor Array, 16 Term	CTS Corp.	742163220JTR
18	2	T3, T5	Transformer, ADT1-1WT, CD542, ADT1-1WT	Mini-Circuits	ADT1-1WT
19	1	U1	14-Bit, 80 MSPS ADC	ADI	AD9444BSVZ-80
20	3	U3, U4, U15	3.3 V Voltage Regulator	ADI	ADP3338-3.3 V
21	1	U14	5 V Voltage Regulator	ADI	ADP3338-5.0 V
22	1	U6	Clock Oscillator, 80 MHz	CTS Reeves	MX045-80
23	1	U7	LVDS-to-CMOS Translator with 100 Term	Texas Instruments	SN75LVDT386DGG
24	1	U10	2 Input XOR Gate	Fairchild	74VCX86M
25	4	U6	Pin Sockets, Closed End	AMP	5-330808-3

Item	Qty.	REFDES	Description	Manufacturer	MFG_PART_NO
26	24	C10, C11, C13, to C19, C29, C31, C36 to C38, C45, C49, C59, C62, C69, C70 to C73, C90[1]	Capacitors, Select 10 V Ceramic X5R 0402	Panasonic	
27	1	J5[1]	Connector, Gold, Male, Coaxial, SMA, Vertical	Johnston Comp.	142-0701-201
28	2	P5, P6[1]	Power Connectors	Weiland	
29	1	R1, R2, R5, R7, R13[1]	Resistors, Select 1/16 W 1% 0402 SMD	Panasonic	
30	1	R17 to R20, R27, R36 to R38, R40[1]	Resistors, Select 1/16 W 1% 0402 SMD	Panasonic	
31	5	U2[1]	XO Select	Vectron	

[1] Parts not placed.

CMOS EVALUATION BOARD SCHEMATICS

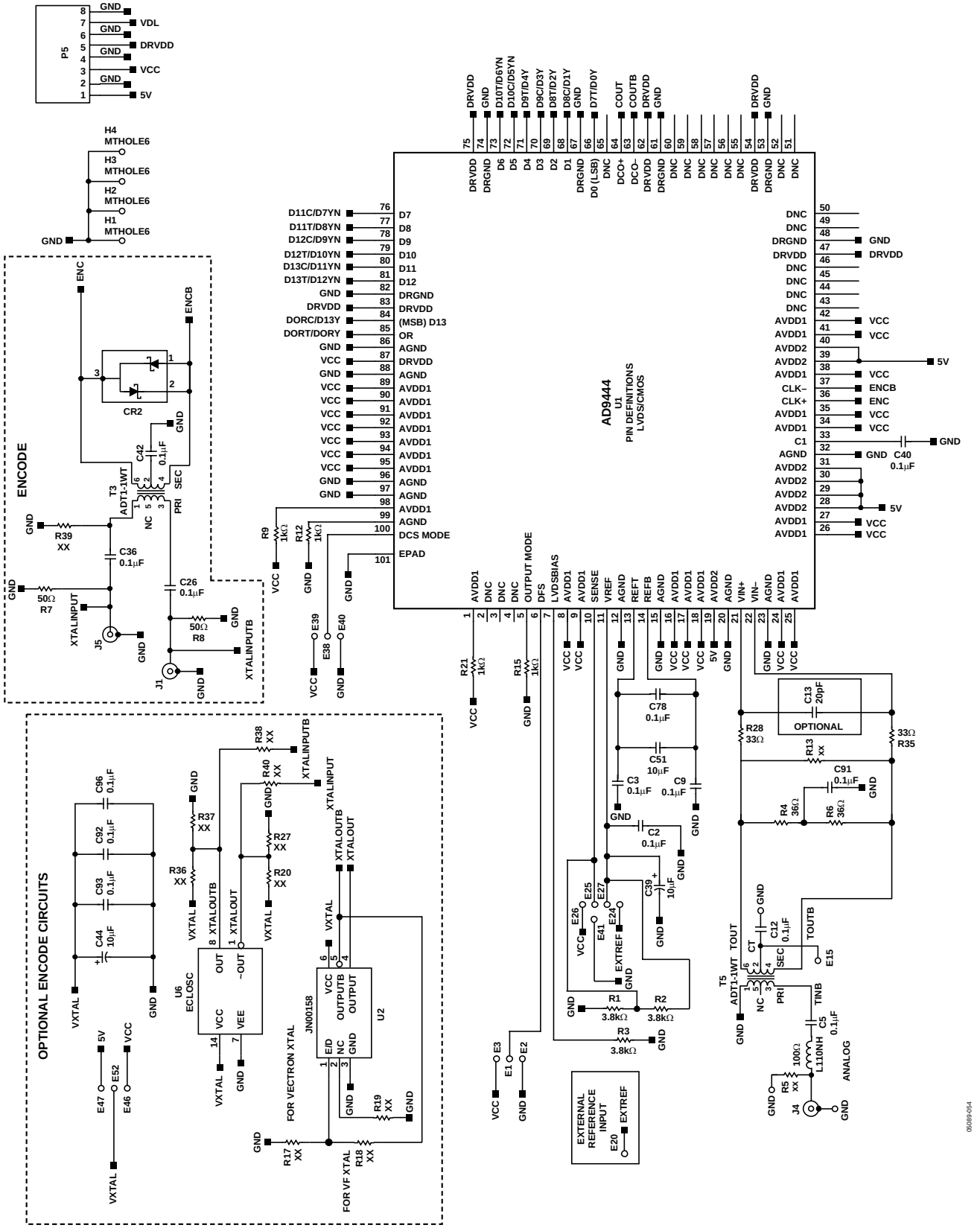


Figure 59. CMOS Mode Evaluation Board Schematic

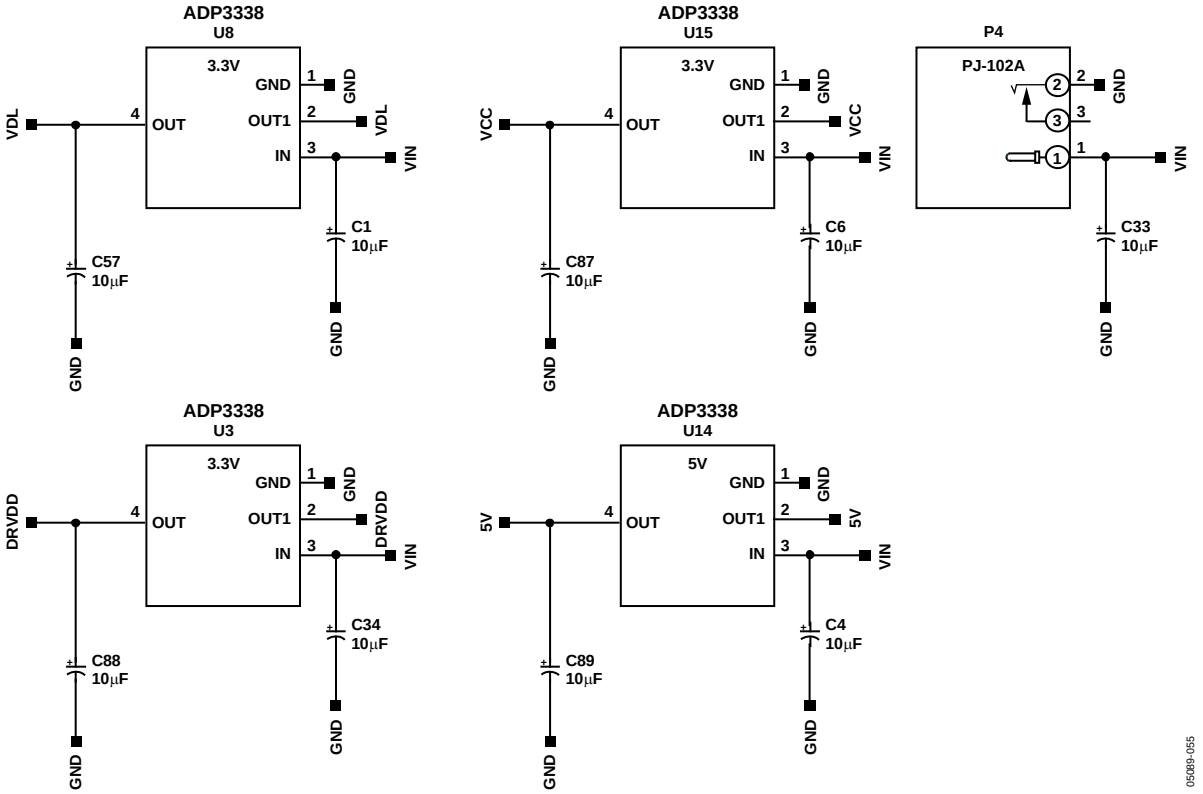


Figure 60. CMOS Mode Evaluation Board Schematic (Continued)

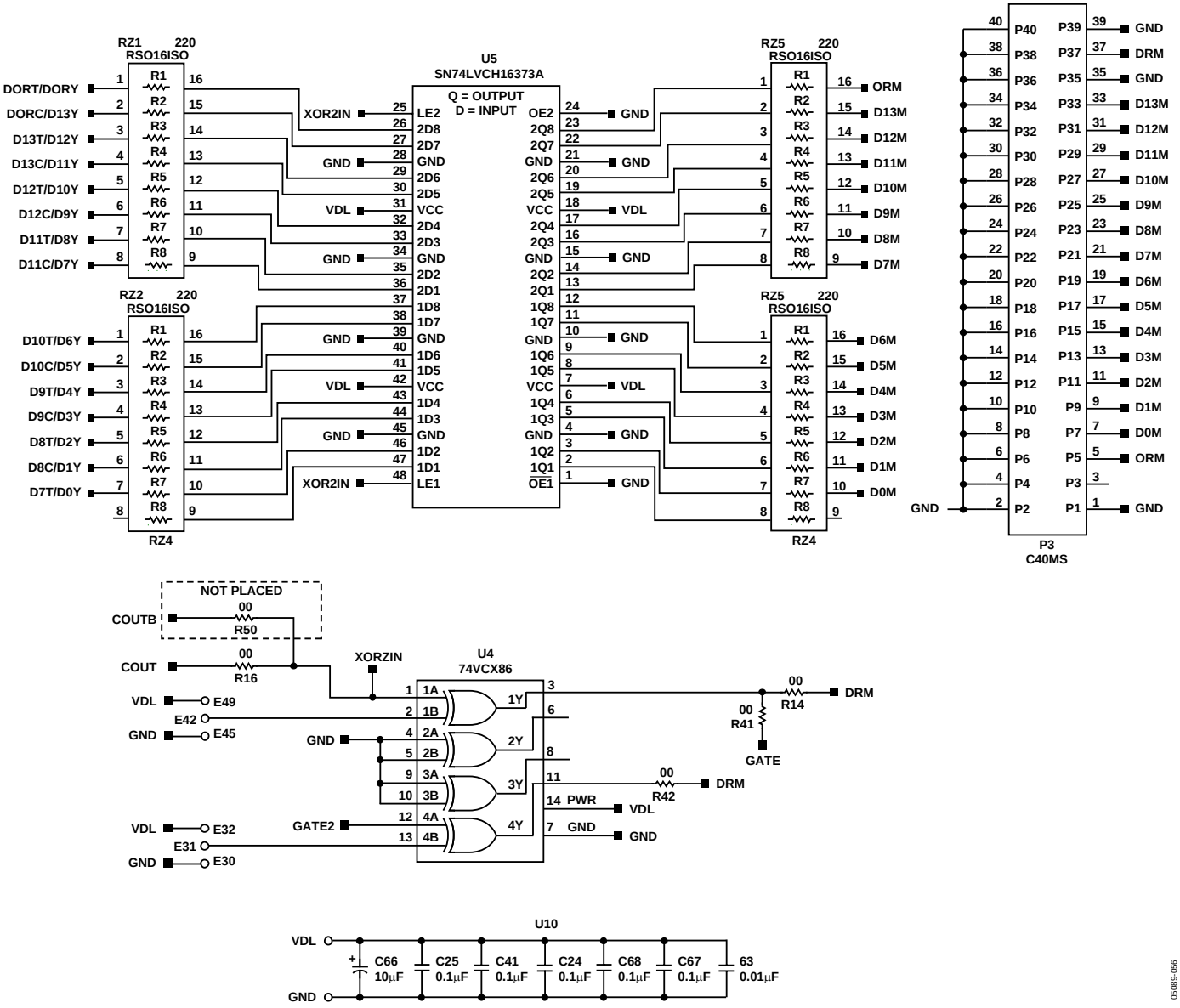


Figure 61. CMOS Mode Evaluation Board Schematic (Continued)

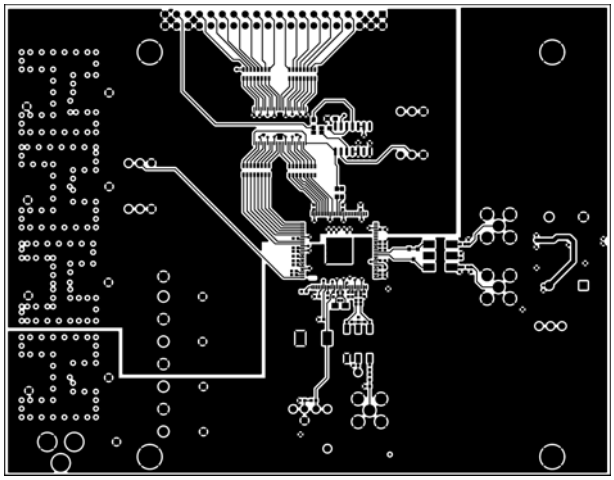


Figure 62. CMOS Mode Evaluation Board Layout, Primary Side

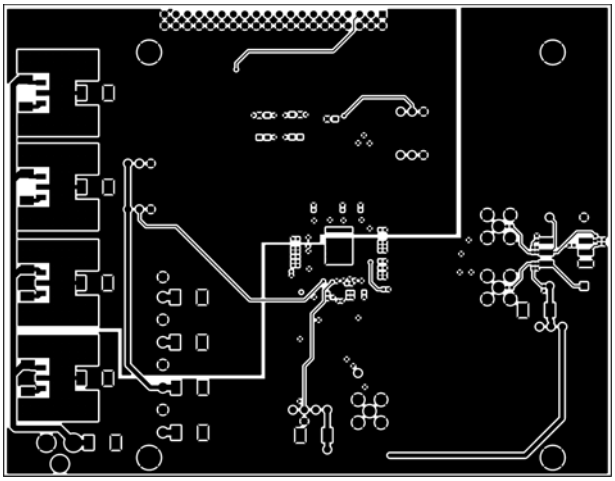


Figure 63. CMOS Mode Evaluation Board Layout, Secondary Side

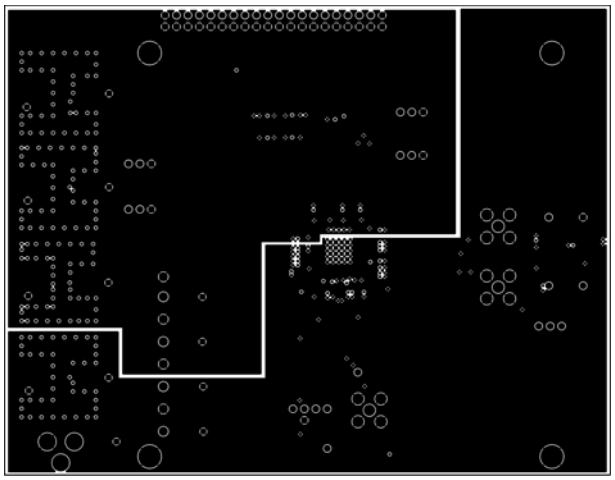


Figure 64. CMOS Mode Evaluation Board Layout, Ground Plane 1

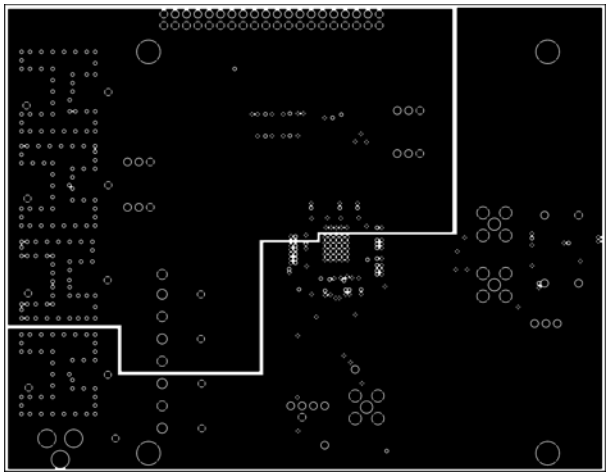


Figure 65. CMOS Mode Evaluation Board Layout, Ground Plane 2

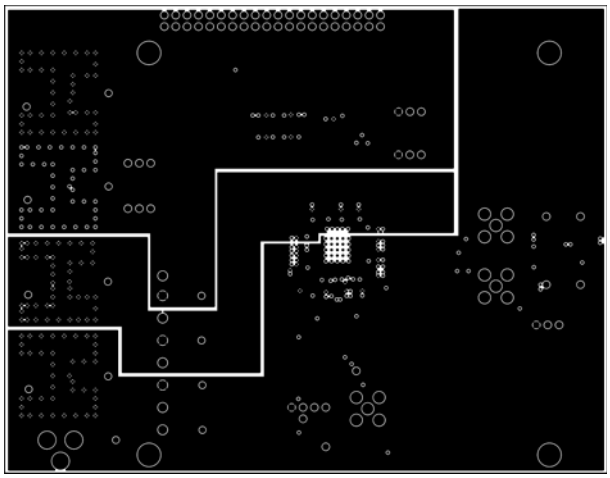


Figure 66. CMOS Mode Evaluation Board Layout, Power Plane 1

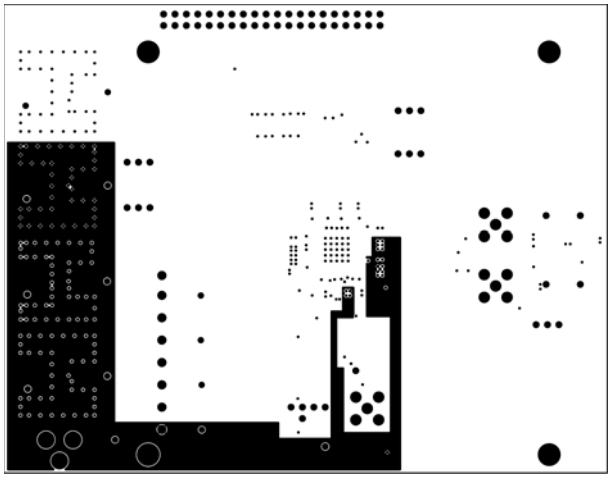


Figure 67. CMOS Mode Evaluation Board Layout, Power Plane 2

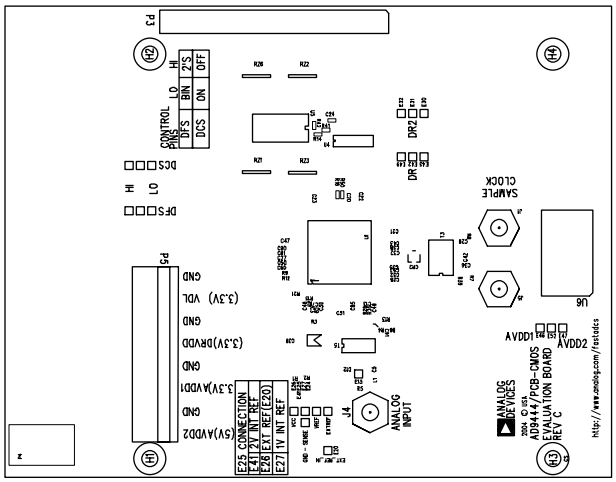


Figure 68. CMOS Mode Evaluation Board Layout, Primary Silkscreen

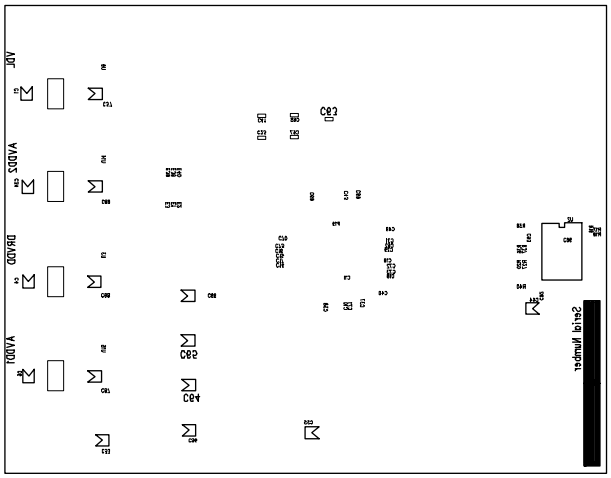


Figure 69. CMOS Mode Evaluation Board Layout, Secondary Silkscreen

CMOS MODE EVALUATION BOARD BILL OF MATERIALS (BOM)

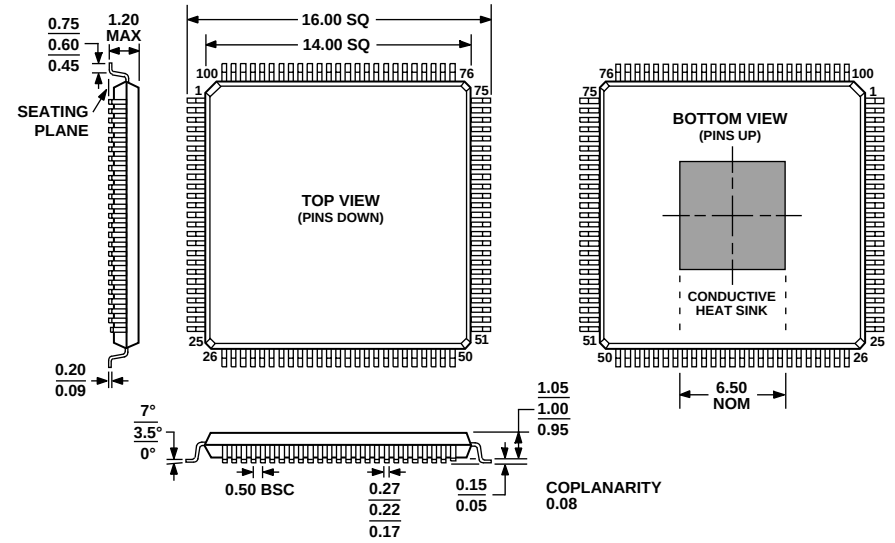
Table 12.

Item	Qty.	REFDES	Description	Manufacturer	MFG_PART_NO
1	1	AD9444PCB	PCB, AD9444 LVDS Evaluation Board	PCSM	AD9444LVDSCUSTREVC
2	16	C1, C4, C6, C33, C34, C39, C44, C55 to C57, C64 to C66, C87 to C89	Capacitors, Tantalum, SMT BCAPTAJC, 10 µF, 16 V, 10%	KEMET	T491C106K016AS
3	32	C2, C3, C5, C9, C12, C20 to C23, C26 to C28, C30, C32, C35, C40, C42, C43, C46 to C48, C50, C52, C53, C58, C60, C61, C75, C78, C85, C91, C92	Capacitors, 0.1 µF 10 V Ceramic X5R 0402	Panasonic	ECJ-0EB1A104K
4	5	C24, C25, C41, C67, C68	Capacitors, 0.1 µF 16 V Ceramic X7R 0603	Panasonic	ECJ-1VB1C104K
5	1	C51	Capacitor, Ceramic 10 µF 6.3 V X5R 0805	KEMET	C0805C106K9PACTU
6	1	CR2	Diode, Dual Schottky HSMS2812, SOT-23, 30 V, 20 mA	Panasonic	MA716-(TX)
7	20	E1 to E3, E24 to E27, E30 to E32, E38 to E42, E45 to E47, E49, E52	40-Pin Breakable Header	3M	2340-611TN
8	2	J1, J4	Connector, Gold, Male, Coaxial, SMA, Vertical	Johnston Comp.	142-0701-201
9	1	L1	10 nH O402 Inductor	Coilcraft	0402CS-10NX_B_
10	1	P3	Header, 40-Pin, Male, 40-Pin Right Angle	Samtec	TSW-120-08-T-D-RA
11	1	P4	Power Jack	Swithcraft	RAPC722
12	1	R3	Resistor, 3.6 kΩ 1/16 W 1% 0402 SMD	Panasonic	ERJ-2GEJ362X
13	2	R4, R6	Resistors, 36 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GEJ360X
14	1	R8	Resistor, 49.9 Ω 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF49R9X
15	4	R9, R12, R15, R21	Resistors, 1.00 kΩ 1/16 W 1% 0402 SMD	Panasonic	ERJ-2RKF1001X
16	2	R14, R50	Resistors, 0 Ω 1/10 W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
17	2	R28, R35	Resistors, 33 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GEJ330X
18	1	R39	Resistor, 0 Ω 1/16 W 5% 0402 SMD	Panasonic	ERJ-2GE0R00X
19	4	RZ1 to RZ3, RZ6	220 Ω Resistor Array, 16 Term	CTS Corp.	742163221JTR
20	2	T3, T5	Transformer, ADT1-1WT, CD542, ADT1-1WT	Mini-Circuits	ADT1-1WT
21	1	U1	14-Bit, 80 MSPS ADC	ADI	AD9444BSVZ-80
22	4	U3, U8, U15	3.3 V Voltage Regulator	ADI	ADP3338-3.3 V
23	1	U14	5 V Voltage Regulator	ADI	ADP3338-5.0 V
24	1	U5	16-Bit Flip Flop	Fairchild	74LVTH162374
25	4	U6	Pin Sockets, Closed End	AMP	5-330808-3

Item	Qty.	REFDES	Description	Manufacturer	MFG_PART_NO
26	26	C10, C11, C13, C14 to C19, C29, C31, C36 to C37, C38, C45, C49, C59, C62,C69, C70 to C73, C90, C93, C96[1]	Capacitors, Select 10 V Ceramic X5R 0402	Panasonic	
27	1	J5[1]	Connector, Gold, Male, Coaxial, SMA, Vertical	Johnston Comp.	142-0701-201
28	15	R1,R2,R5,R7, R13, R17 to R20, R27, R36 to R40[1]	Resistors, Select 1/16 W 1% 0402 SMD	Panasonic	
29	3	R16, R41, R42[1]	Resistors, Select 1/16 W 5% 0603 SMD	Panasonic	
30	1	C63[1]	Capacitor, Select 10 V Ceramic X5R 0603	Panasonic	
31	1	U4[1]	XOR 74VCX86D	Fairchild	74VCX86D
32	2	P5, P6[1]	Power Connectors	Weiland	

[1] Parts not placed.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026AED-HD

NOTES
1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE PACKAGE HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.
3. THE EXPOSED HEAT SINK SOLDERED TO THE GROUND PLANE IS REQUIRED FOR THE 100-LEAD TQFP/EP.

Figure 70. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline
AD9444BSVZ-80[1]	−40°C to +85°C	100-Lead TQFP_EP	SV-100-1
AD9444-CMOS/PCB		CMOS Mode Evaluation Board	
AD9444-LVDS/PCB		LVDS Mode Evaluation Board	

[1] Z = Pb-free part.

NOTES

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