

Evaluation Board for Dual, High Speed Operational Amplifiers (8-Lead SOIC and Exposed Paddle)

FEATURES

- Enables quick breadboarding/prototyping**
- User-defined circuit configuration**
- Edge-mounted SMA connector provisions**
- Easy connection to test equipment and other circuits**
- Two independent op amp configurations**
- Instrumentation amplifier configuration capable**

GENERAL DESCRIPTION

The EB-O8RE-2Z is designed to aid in the evaluation of dual, high speed operational amplifiers. The EB-O8RE-2Z is a bare board (that is, there are no components soldered to the board) that enables users to quickly prototype a variety of operational amplifier circuits, which minimizes risk and reduces time to market. The EB-O8RE-2Z evaluation board supports any of the Analog Devices, Inc., dual, high speed operational amplifiers in an 8-lead SOIC package with an exposed paddle.

Figure 1 shows the component side of the evaluation board, and Figure 2 shows the circuit side of the evaluation board. Figure 3 shows the evaluation board schematic.

The 4-layer evaluation board accepts edge-mounted SMA connectors on both inputs and outputs, which allows efficient and quick connection to test equipment or other circuitry.

The board ground plane, component placement, and power supply bypassing are optimized for maximum circuit flexibility and performance. The evaluation board uses a variety of SMT component case sizes: 0402, 0508, 0603, and 7343.

Figure 4 and Figure 6 show the evaluation board assembly drawings. Figure 5 and Figure 7 show the metal layout pattern for connecting the board to the op amp and to the supporting circuitry.

EVALUATION BOARD COMPONENT AND CIRCUIT SIDE DIAGRAMS

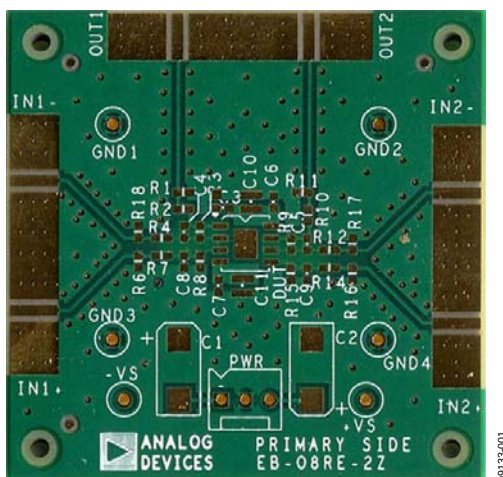


Figure 1. EB-O8RE-2Z Component Side of Evaluation Board

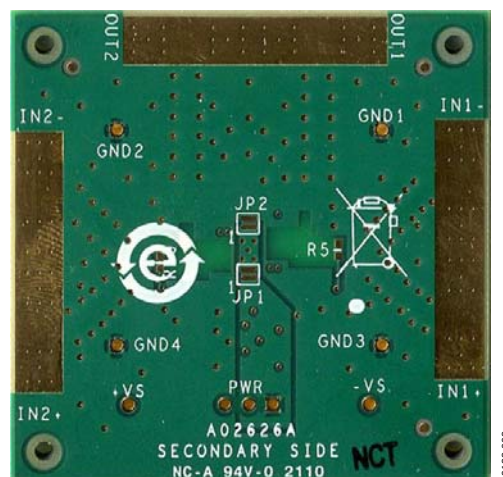


Figure 2. EB-O8RE-2Z Circuit Side of Evaluation Board

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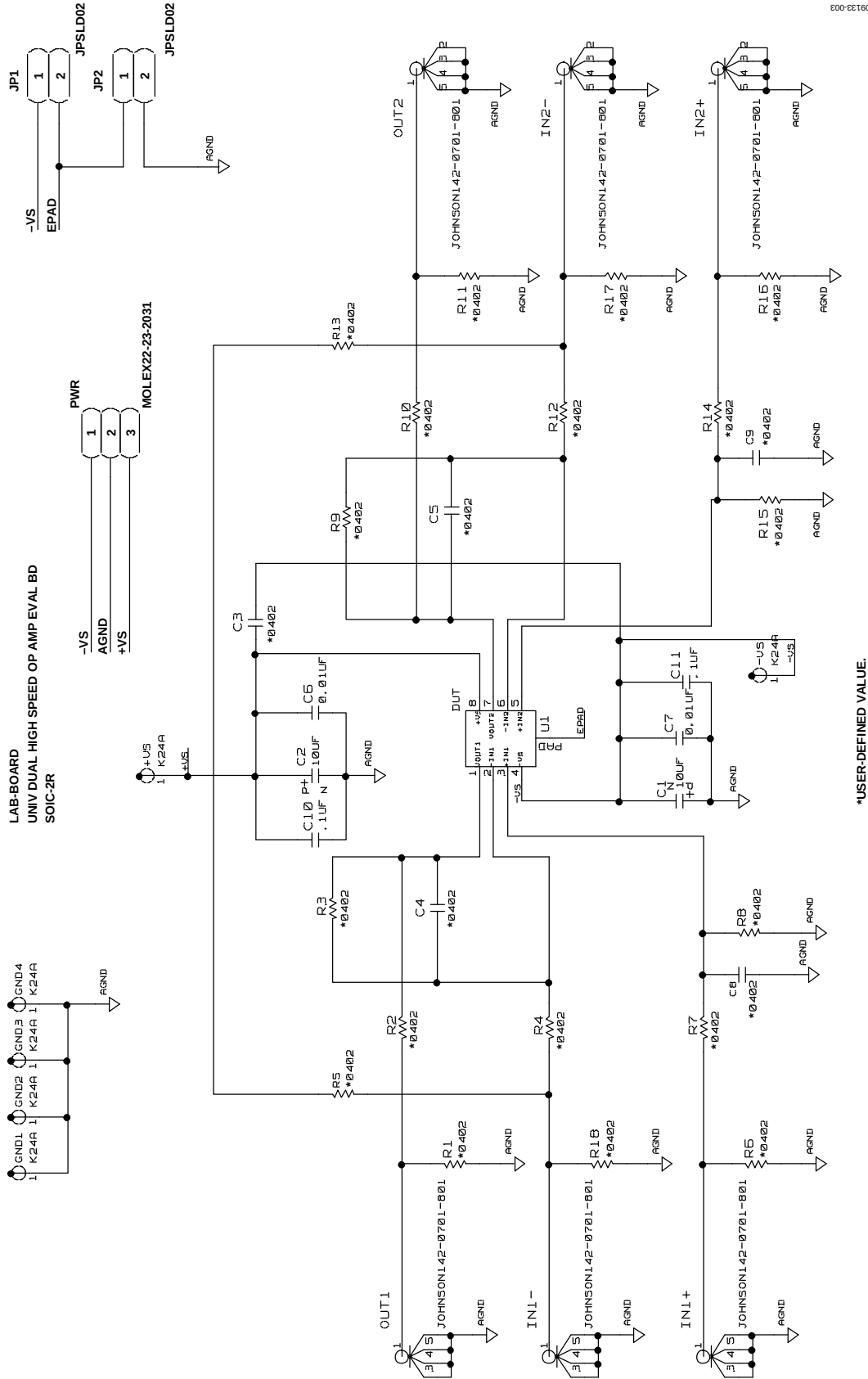
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REVISION HISTORY

5/10—Revision 0: Initial Version

EVALUATION BOARD SCHEMATIC, ASSEMBLY DRAWINGS, AND BOARD LAYOUTS

800-32160



*USER-DEFINED VALUE.

Figure 3. EB-O8RE-2Z Universal Evaluation Board Schematic

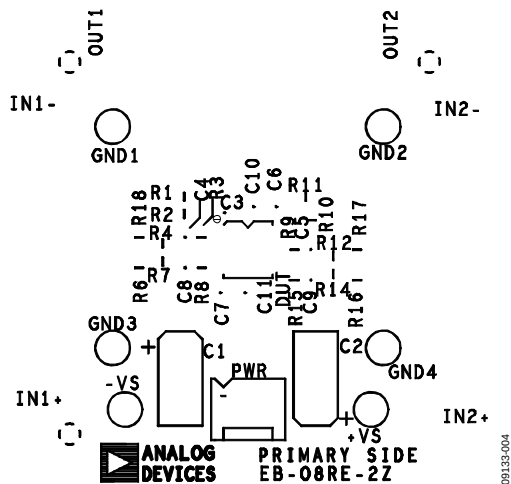


Figure 4. Board Assembly Drawing, Component Side

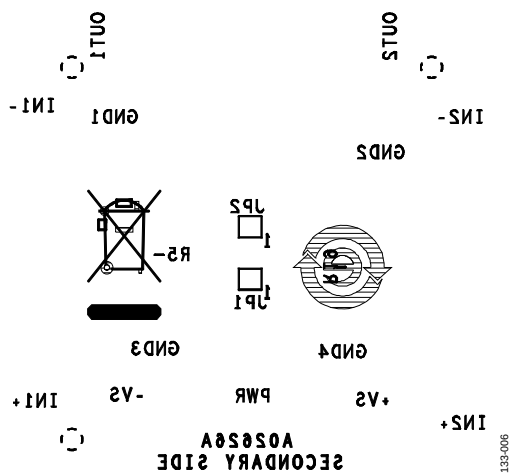


Figure 6. Board Assembly Drawing, Circuit Side

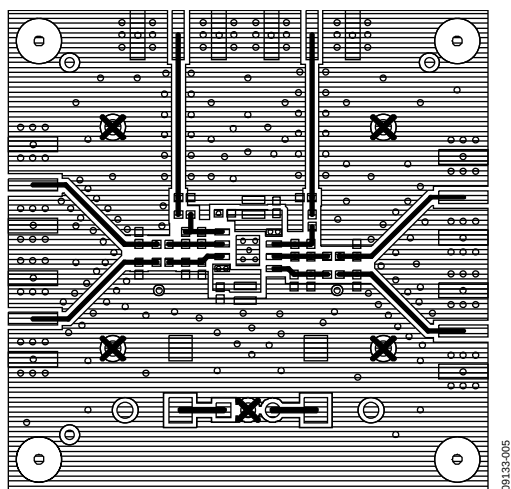


Figure 5. Board Layout Pattern, Component Side

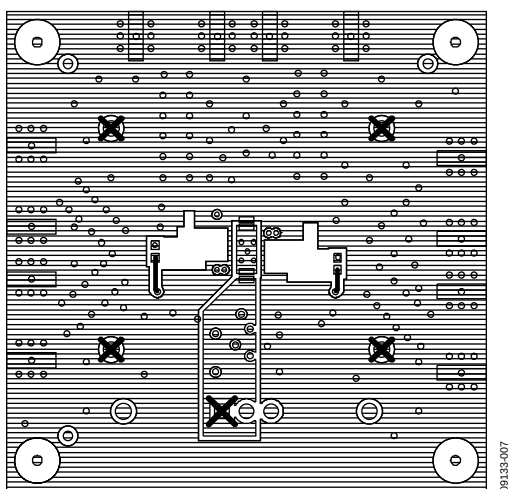


Figure 7. Board Layout Pattern, Circuit Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Package
6	IN1+, IN1–, OUT1, IN2+, IN2–, OUT2	SMA/SMT	SMA/SMT
5	C3, C4, C5, C8, C9	User-defined capacitor	C0402
2	C6, C7	0.01 μ F capacitor	C0402
2	C10, C11	0.1 μ F capacitor	C0508
2	C1, C2	10 μ F capacitor	C6032
18	R1 to R18	User-defined resistor	R0402
6	GND1, GND2, GND3, GND4, +VS, –VS	Test point	TP
1	PWR	Header 3 POS	Molex 22-23-2031
2	JP1, JP2	User-defined jumper	Solder jumper
1	U1	Amplifier	8-lead SOIC

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**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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