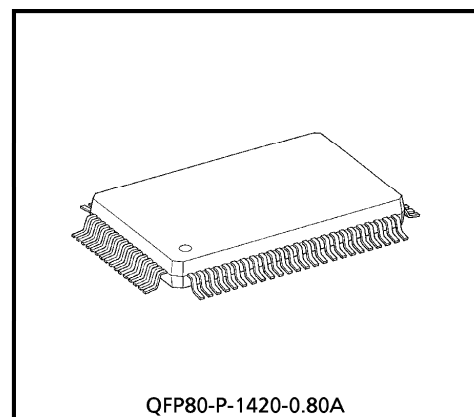


TC9284BF

CD SINGLE CHIP PROCESSOR WITH BUILT-IN 1BIT DA CONVERTER

The TC9284BF is a single chip processor for sync separation protection/synchronization, EFM demodulation, error correction/interpolation, microcomputer interface, CLV servo a focus tracking servo in CD player system. And, built-in 1bit DA converter. In combination with the TA8190F/TA8191F/TA2031F/TA2035F/TA2065F/TA2077F, which are focus tracking servo LSI, a CD player system can be composed very simply.



Weight : 1.57g (Typ.)

FEATURES

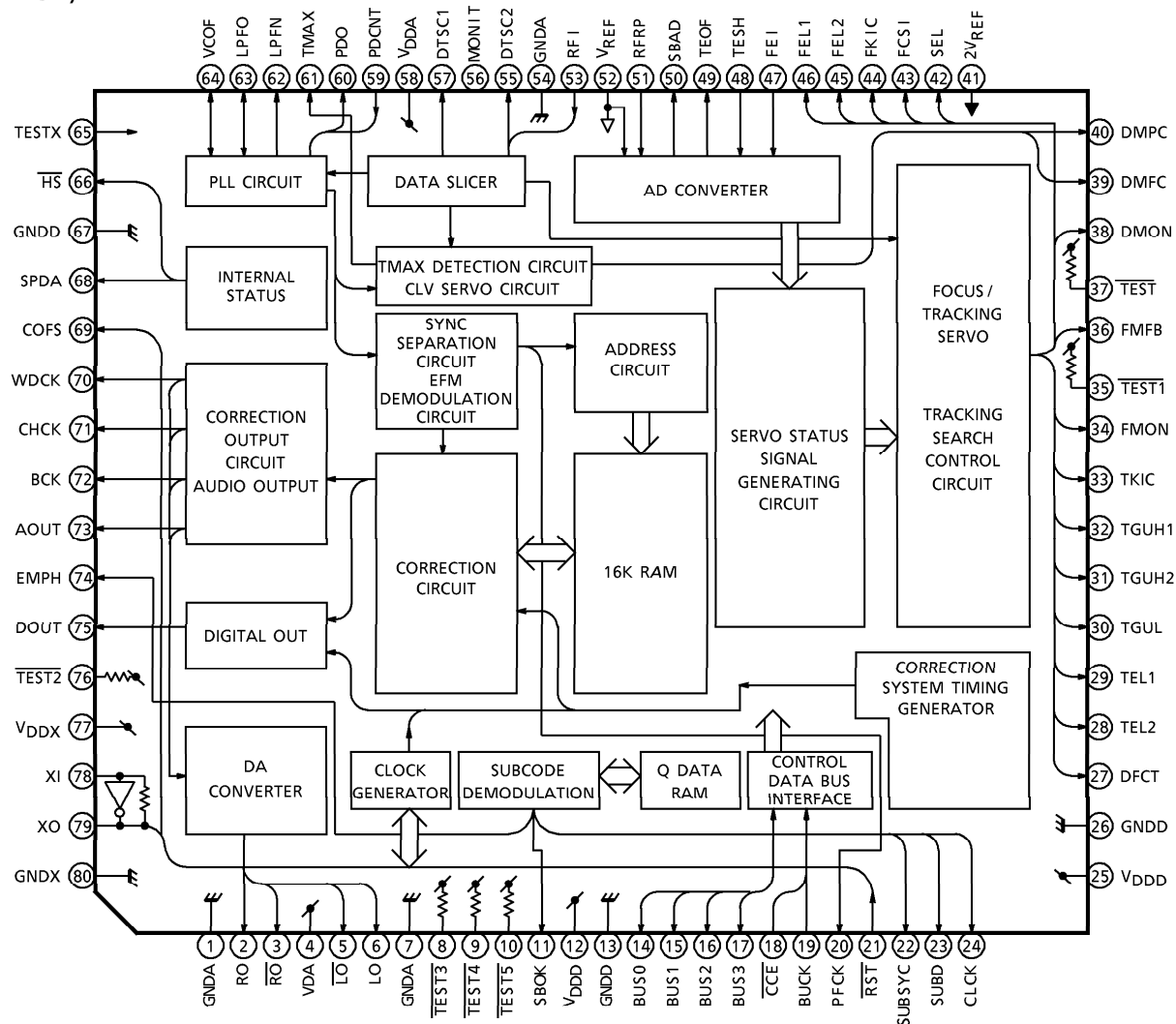
- Positive sync pattern detection, sync signal protection and synchronization.
- Built-in EFM demodulation and subcode demodulation circuit.
- Has the correction capacity of single and double corrections for C1 and C2 correcting units, respectively, using CIRC correction theoretical format.
- Jitter absorbing capacity of ± 5 frames.
- Built-in 16K RAM.
- Built-in digital out circuit.
- Smooth muting through zero cross detection.
- Read timing free subcode Q data.
- Built-in data slicer and analog PLL (free-adjustment VCO adopted) circuit.
- Focus/tracking loop gain auto adjusting function incorporated.
- Built-in AFC and APC circuits for disc motor CLV servo.
- Built-in focus tracking servo control circuit.
- Tracking search control capable of coping with all modes.
- Built-in 1bit DA converter.
Function of DA converter.
 - (1) Built-in 8-time oversampling digital filter.
 - (2) Built-in soft mute function.
- Built-in microcomputer interface circuit.
- Double speed play is possible.
- In CMOS structure, high speed and low power dissipation.
- 80 pin flat package.

980508EBA2

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

PIN CONNECTION / BLOCK DIAGRAM

(Top view)



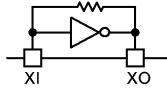
PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTIONAL DESCRIPTION	REMARKS
1	GNDA	—	Analog grand terminal for DA converter (R channel)	—
2	RO	O	R channel data forward output terminal.	—
3	$\overline{RO}$	O	R channel data reverse output terminal.	—
4	V _{DA}	—	Analog power supply terminal for DA converter.	—
5	$\overline{LO}$	O	L channel data reverse output terminal.	—
6	LO	O	L channel data forward output terminal.	—
7	GNDA	—	Analog grand terminal for DA converter (L channel)	—
8	$\overline{TEST3}$	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor
9	$\overline{TEST4}$	I	Test terminal. Normally, keep at "H" level or open.	
10	$\overline{TEST5}$	I	Test terminal. Normally, keep at "H" level or open.	
11	SBOK	O	Subcode Q data CRC check adjusting result output terminal. The adjusting result is OK at "H" level.	—
12	V _{DD}	—	Digital supply voltage terminal. (+5V)	—
13	GNDD	—	Digital ground terminal.	—
14 & 17	BUS0 & BUS3	I / O	Command and data sending / receiving input / output terminals.	Schmitt input Open drain output With pull-up resistor
18	$\overline{CCE}$	I	Command and data sending / receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmitt input
19	BUCK	I	Command and data sending / receiving clock input terminal.	
20	PFCK	O	Regeneration system frame periodic signal output terminal. 7.35kHz	—
21	$\overline{RST}$	I	Reset input terminal. The internal system is reset at "L" level.	With pull-up resistor
22	SUBSYC	O	Subcode sync signal output terminal.	—
23	SUBD	O	Subcode P~W output terminals.	—
24	CLCK	I	Subcode P~W data readout clock input terminal.	—
25	V _{DD}	—	Digital supply voltage terminal.	—
26	GNDD	—	Digital ground terminal.	—
27	DFCT	O	Defect detection signal output terminal. V _{REF} when defect is detected. Normally, HiZ.	—
28 29	TEL2 TEL1	O	Tracking gain adjusting analog switch output terminals V _{REF} or HiZ.	—
30	TGUL	O	Tracking servo loop low frequency phase compensator change-over analog switch output terminal. HiZ (gain up) when detecting shock. Normally, V _{REF} .	—

PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS																
31	TGUH2	O	Tracking servo loop middle / high frequency phase compensator change-over analog switch output terminals.	—																
32	TGUH1		HiZ (gain up) when detecting shock. Normally, VREF. TGUH1 is used at normal regeneration and TGUH2 is used at double speed regeneration.																	
33	TKIC	O	Tracking actuator kick signal output terminal. Kicks in the outer circumferential direction at "H" level and in the inner circumferential direction at "L" level.	3-state output																
34	FMON	O	Feed servo ON / OFF analog switch output terminals. Servo on at "HiZ". Servo off at "VREF".	—																
35	TEST1	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor																
36	FMFB	O	Feed motor FWD / BWD feeding control signal output terminal. Feed in the outer circumferential direction at "H" level and in the inner circumferential direction at "L" level.	3-state output																
37	TEST	I	Test terminal. Normally, keep at "H" level or open.	With pull-up resistor																
38	DMON	O	Disc motor driving circuit gain change-over analog switch output terminal.	—																
39	DMFC	O	Disc motor CLV servo AFC signal output terminal. <table border="1"><thead><tr><th>COMMAND</th><th>DMFC OUTPUT</th><th>OPERATION</th></tr></thead><tbody><tr><td>DMFK</td><td>H</td><td>Motor acceleration</td></tr><tr><td>DMSV</td><td>PWM</td><td>CLV servo ON</td></tr><tr><td>DMBK</td><td>L</td><td>Motor deceleration</td></tr><tr><td>DMOFF</td><td>VREF</td><td>CLV servo OFF</td></tr></tbody></table>	COMMAND	DMFC OUTPUT	OPERATION	DMFK	H	Motor acceleration	DMSV	PWM	CLV servo ON	DMBK	L	Motor deceleration	DMOFF	VREF	CLV servo OFF	3-state output	
COMMAND	DMFC OUTPUT	OPERATION																		
DMFK	H	Motor acceleration																		
DMSV	PWM	CLV servo ON																		
DMBK	L	Motor deceleration																		
DMOFF	VREF	CLV servo OFF																		
40	DMPC	O	Disc motor CLV servo APC signal output terminal.	3-state output																
41	2VREF	I	Double times reference voltage input terminal. (VREF×2)	—																
42	SEL	O	Servo mode indicating signal output terminal. <table border="1"><thead><tr><th>SEL</th><th>LD ON / OFF</th><th>FOCUS SERVO</th><th>OPERATION</th></tr></thead><tbody><tr><td>L</td><td>OFF</td><td>OFF</td><td>LD OFF</td></tr><tr><td>HiZ</td><td>ON</td><td>OFF</td><td>Focus Search</td></tr><tr><td>H</td><td>ON</td><td>ON</td><td>Normal play, etc. Focus Servo ON : FOK)</td></tr></tbody></table>	SEL	LD ON / OFF	FOCUS SERVO	OPERATION	L	OFF	OFF	LD OFF	HiZ	ON	OFF	Focus Search	H	ON	ON	Normal play, etc. Focus Servo ON : FOK)	3-state output
SEL	LD ON / OFF	FOCUS SERVO	OPERATION																	
L	OFF	OFF	LD OFF																	
HiZ	ON	OFF	Focus Search																	
H	ON	ON	Normal play, etc. Focus Servo ON : FOK)																	

PIN No.	SYMBOL	I/O	FUNCTION DESCRIPTION	REMARKS		
43	FCSI	O	Focus actuator driving signal output terminal in the focus search mode.	3-state output		
			COMMAND		FCSI OUTPUT	OPERATION
			FORST		H	Lens gets for away from disc
			FOSET		L	Lens gets near disc
			Others		HiZ	Other than focus search
44	FKIC	O	Focus actuator driving signal output terminal in the focus gain adjusting mode.	3-state output		
			COMMAND		FKIC OUTPUT	OPERATION
			FGASR		H	Lens gets for away from disc
			FGASS		L	Lens gets near disc
			Others		HiZ	Other than focus adjustment
45	FEL2	O	Fucus again adjusting analog switch output terminals.	—		
46	FEL1					
47	FEI	I	Focus error signal input terminal.	Analog output		
48	TESH	I	Tracking error signal input sample holding analog switch input terminal.	—		
49	TEOF	O	Tracking servo operation ON/OFF analog switch output terminal. VREF when the tracking servo is OFF.	—		
50	SBAD	I	Sub beam adding signal input terminal.	Analog input		
51	RFRP	I	RF ripple signal input terminal.			
52	VREF	I	Reference voltage input terminal. (+ 2.1V)	—		
53	RFI	I	RF signal input terminal.	Analog input		
54	GNDA	—	Analog ground terminal.	—		
55	DTSC2	O	Data slice control EFM signal passive output terminal.	—		
56	MONIT	O	Internal signal (EFMO, PLCK, LOCK and MBOV) output terminal. Selected by command.	—		
57	DTSC1	O	Data slice control EFM signal negative output terminal.	—		
58	VDDA	—	Analog supply voltage terminal. (+ 5V)	—		
59	PDCNT	I	PDO output control terminal. At “L” level, PDO output is made to HiZ by force.	—		
60	PDO	O	Phase error signal output terminal between EFM signal and PLCK.	3-state output		

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS	
61	TMAX	O	TMAX signal output terminal. Hiz at time of system clock.	3-state output	
			TMAX PERIOD		TMAX OUTPUT
			Longer than specified period		L
			Shorter than specified period		H (2VREF)
			Specified period		HiZ
62	LPFN	I	LPF amplifier inverting input terminal for PLL.	—	
63	LPFO	O	LPF amplifier output terminal for PLL.	—	
64	VCOF	I	VCO filter terminal.	—	
65	TESTX	I	Test terminal.	—	
66	HS	O	Double speed monitor output terminal. Double speed operation at “L” level.	—	
67	GNDD	—	Digital ground terminal.	—	
68	SPDA	O	Processor status signal output terminal. Correction process judging result, memory buffer capacity, etc.	—	
69	COFS	O	Correction system frame periodic signal output terminal. 7.35kHz.	—	
70	WDCK	O	Word clock output terminal. Normally, 88.2kHz.	—	
71	CHCK	O	Channel clock output terminal. Normally, 44.1kHz.	—	
72	BCK	O	Bit clock output terminal. Normally, 1.4112MHz.	—	
73	AOUT	O	Audio data output terminal.	—	
74	EMPH	O	Emphasis ON/OFF indication signal output terminal. Emphasis ON at “H” level.	—	
75	DOUT	O	Digital out output terminal.	—	
76	TEST2	I	Test terminal. Normally, keep at “H” level or open.	With pull-up resistor	
77	VDDX	O	Oscillator supply voltage terminal.	—	
78	XI	I	Crystal oscillator connecting terminal.		
79	XO	O			
80	GNDX	O	Oscillator grand terminal.	—	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{DD}	-0.3~6.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Power Dissipation	P _D	1250	mW
Operating Temperature	T _{opr}	-35~85	°C
Storage Temperature	T _{stg}	-55~150	°C

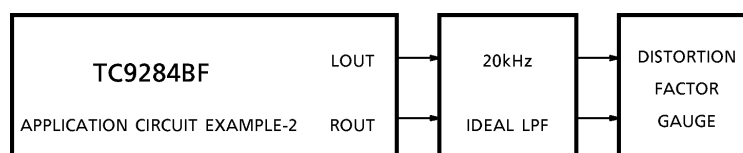
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{DD} = 5V, 2V_{REF} = 4.2V, V_{REF} = 2.1V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V _{DD}	—	Ta = -35~85°C	4.5	5.0	5.5	V
Operating Supply Current		I _{DD}	—	XI = 16.9344MHz In normal mode	—	40	70	mA
Input Voltage	"H" Level	V _{IH} (1)	—	Whole input terminals except BUS0~3, BUCK and CCE	3.5	—	V _{DD} + 0.3	V
	"L" Level	V _{IL} (1)	—		0	—	1.5	
	"H" Level	V _{IH} (2)	—	BUS0~3, BUCK, CCE (Schmitt input)	4.0	—	V _{DD} + 0.3	
	"L" Level	V _{IL} (2)	—		0	—	1.0	
Input Current	"H" Level	I _{IH}	—	V _{IH} = 5V CMOS input terminals except analog input terminal	—	—	1.0	μA
	"L" Level	I _{IL}	—		-1.0	—	—	
Try State Leak Current	"H" Level	I _{TLH}	—	V _{IH} = 5V	—	—	1.0	μA
	"L" Level	I _{TLL}	—	V _{IL} = 0V	-1.0	—	—	
Output Current	"H" Level	I _{OH} (1)	—	V _{OH} = 4.6V WDCK, CHCK, BCK, AOUT, DOUT, XO V _{OUT} = V _{DD}	—	—	-2.0	mA
	"L" Level	I _{OL} (1)	—	V _{OL} = 0.4V	2.0	—	—	
	"H" Level	I _{OH} (2)	—	V _{OH} = 4.6V SBOK, PFCK, SUBSYN, SUBD, CLCK, SEL, HS, FCSI, FKIC, PDCNT, MONIT, COFS, SPDA V _{OUT} = V _{DD}	—	—	-0.5	
	"L" Level	I _{OL} (2)	—	V _{OL} = 0.4V	1.0	—	—	
	"H" Level	I _{OH} (3)	—	V _{OH} = 3.8V TKIC, FMFB, DMFC, DMPC, TMAX V _{OUT} = 2V _{REF}	—	—	-0.4	
	"L" Level	I _{OL} (3)	—	V _{OL} = 0.4V	1.0	—	—	
	"H" Level	I _{OH} (4)	—	V _{OH} = 3.8V PDO V _{OUT} = 2V _{REF}	—	—	-1.0	
	"L" Level	I _{OL} (4)	—	V _{OL} = 0.4V	1.0	—	—	
Analog Switch OFF Current	"H" Level	I _{OFH}	—	V _{IH} = 5V	—	—	1.0	μA
	"L" Level	I _{OFL}	—	V _{IL} = 0V	-1.0	—	—	

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Switch ON Resistance	R _{ON} (1)	—	FEL1/2, TEL1/2, FMON, TGUL, TGUH1/2, DFCT, TEOF, DMON	—	—	0.3	kΩ
	R _{ON} (2)		TESH	—	—	0.6	
Pull-up Resistance	R _{UP} (1)	—	RST	—	50	—	kΩ
	R _{UP} (2)		TEST, TEST1~5	—	30	—	
	R _{UP} (3)		BUS3~0	8	—	—	
Oscillation Amplifier Feedback Resistance	R _N	—	XI XO between	2	4	6	kΩ
Operating Frequency Ratio	f _{op}	—	XI	6	—	28	MHz
Total Harmonic Distortion + Noise	THD + N	1	1kHz sine wave Full-scale input	—	− 85	− 80	dB
S / N Ratio	S / N	1		90	98	—	dB
Dynamic Range	DR	1	1kHz sine wave − 60dB input conversion	90	95	—	dB
Cross-talk	CT	1	1kHz sine wave Full-scale input	—	− 95	− 85	dB

TEST CIRCUIT 1 : Application circuit example-2 is used.



LPF : SHIBASOKU 725C BUILT-IN FILTER
 DISTORTION FACTOR GAUGE : SHIBASOKU 725C OR EQUIVALENT

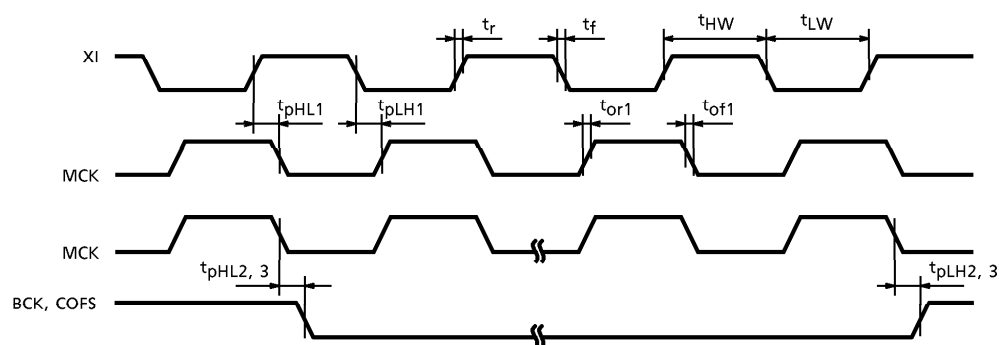
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S / N, DR	ON

A WEIGHT : IEC-A OR EQUIVALENT

AC CHARACTERISTICS

(1) Clock system timing

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	—	XI input	18	—	—	ns
	"L" Level	t_{LW}			18	—	—	
Input Rising Time		t_r			—	—	10	
Input Falling Time		t_f			—	—	10	
Transfer Time (1)	"H" Level	t_{pHL1}	—	XI→MCK	—	—	60	ns
	"L" Level	t_{pLH1}			—	—	60	
Transfer Time (2)	"H" Level	t_{pHL2}	—	MCK→BCK	—	—	60	
	"L" Level	t_{pLH2}			—	—	60	
Transfer Time (3)	"H" Level	t_{pHL3}	—	MCK→COFS	—	—	100	
	"L" Level	t_{pLH3}			—	—	100	
Output Rising Time (1)		t_{or1}	—	MCK, BCK	—	—	15	ns
Output Falling Time (1)		t_{of1}			—	—	15	
Output Rising Time (2)		t_{or2}	—	COFS	—	—	40	ns
Output Falling Time (2)		t_{of2}			—	—	40	

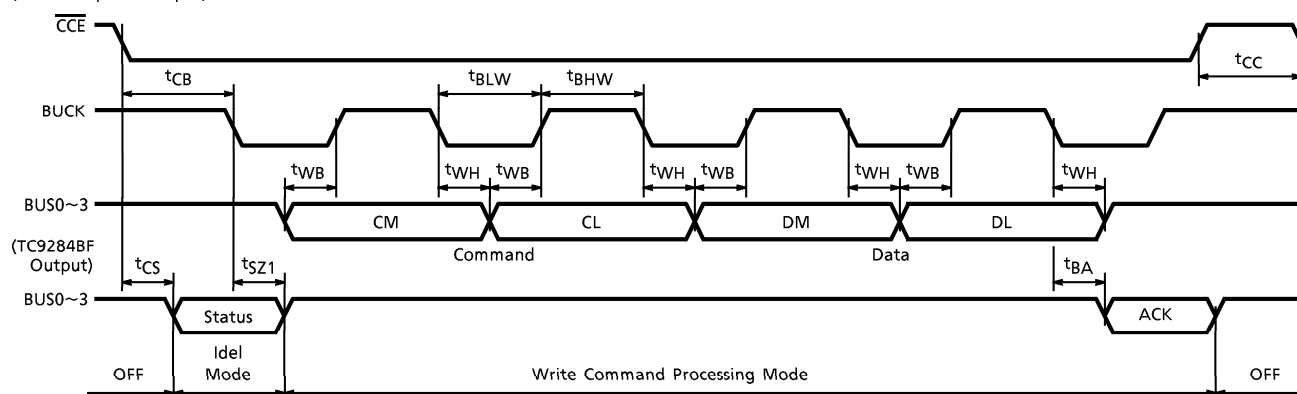


(2) Microcomputer interface timing

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width (1)	"H" Level	t_{BHW}	BUCK	10	—	—	μs
	"L" Level	t_{BLW}		10	—	—	
Clock Pulse Width (2)	"H" Level	t_{CC}	$\overline{CCE}$	6	—	—	μs
Delay Time (1)	t_{CB}	—	$\overline{CCE} \rightarrow \text{BUCK}$	—	—	6	μs
Delay Time (2)	t_{WB}	—	Command Data $\rightarrow$ BUCK	0	—	—	
Delay Time (3)	t_{CS}	—	$\overline{CCE} \rightarrow$ Status Output	—	—	6	
Delay Time (4)	t_{BC}	—	BUCK $\rightarrow \overline{CCE}$	6	—	—	
Setup Time (1)	t_{RD}	—	BUCK $\rightarrow$ Read Data Output	—	—	6	μs
Setup Time (2)	t_{BA}	—	BUCK $\rightarrow$ ACK, Each Parity Output	—	—	6	
Hold time (1)	t_{SZ1}	—	BUCK $\rightarrow$ Status, ACK, Each Parity Output	—	—	6	μs
Hold time (2)	t_{SZ2}	—	$\overline{CCE} \rightarrow$ Status Output	—	—	6	
Hold time (3)	t_{WH}	—	BUCK $\rightarrow$ Command Data	6	—	—	

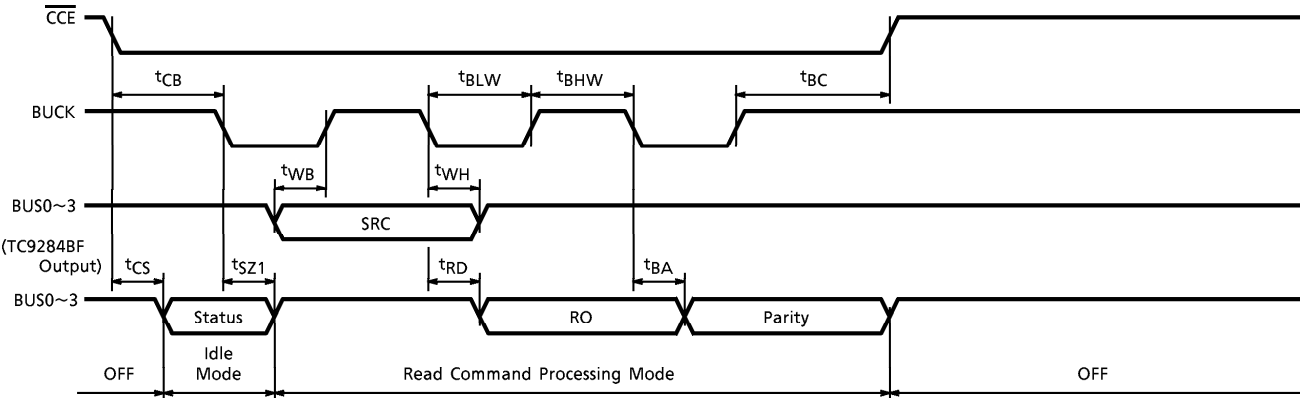
(a) Write command processing mode

(Microcomputer output)



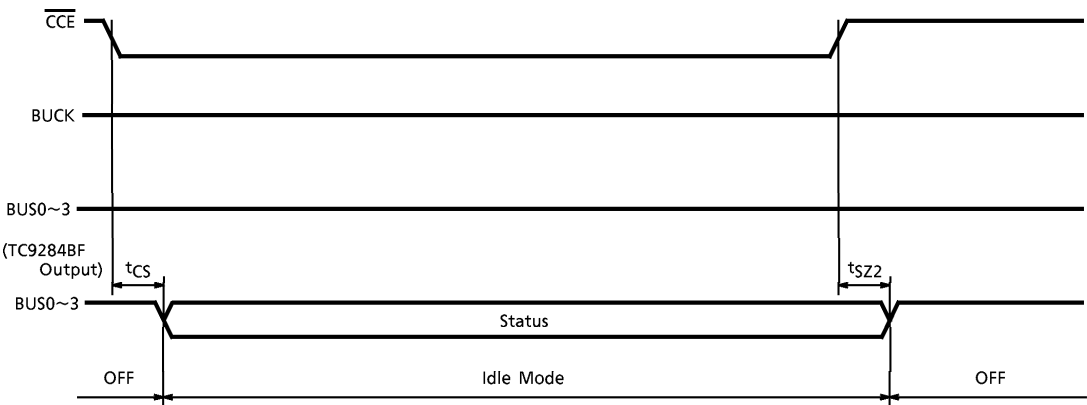
(b) Read command processing mode

(Microcomputer Output)



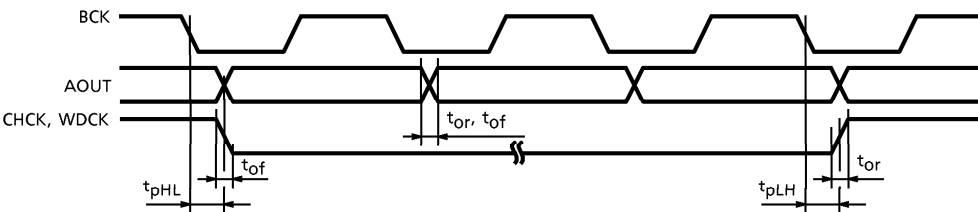
(c) Idle mode

(Microcomputer Output)



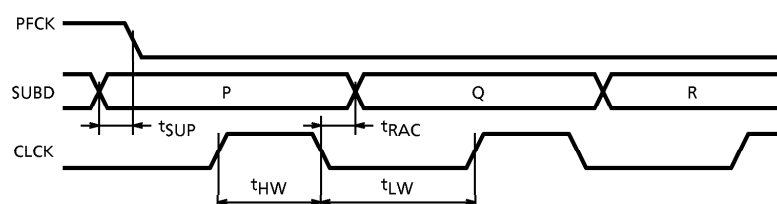
(3) Data output timing

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	—	BCK→AOUT, WDCK, CHCK	—	—	30	ns
	"L" Level	t_{pLH}	—		—	—	30	
Output Rising Time		t_{or}	—	AOUT, WDCK, CHCK	—	—	15	ns
Output Falling Time		t_{of}	—		—	—	15	



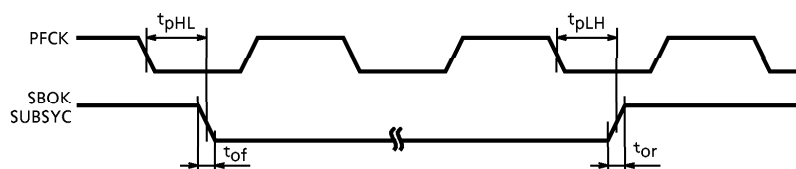
(4) Output timing for subcode P~W

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	"H" Level	t_{HW}	—	CLK	2	—	—	μs
	"L" Level	t_{LW}	—		2	—	—	
Setup Time		t_{SUP}	—	PFCK→SUBD	0.4	—	—	μs
Read Access Time		t_{RAC}	—	CLK→SUBD	1.2	—	—	



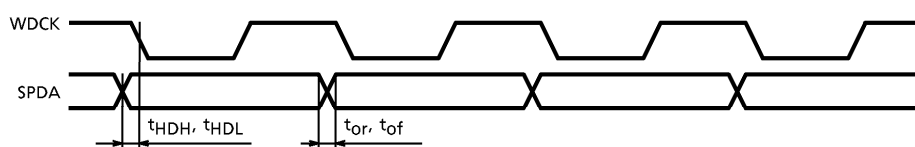
(5) Output timing for subcode Q

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	—	PFCK→SBOK, SUBSYC	-50	—	200	ns
	"L" Level	t_{pLH}	—		-50	—	200	
Output Rising Time		t_{or}	—	SBOK, SUBSYC	—	—	40	ns
Output Falling Time		t_{of}	—		—	—	40	



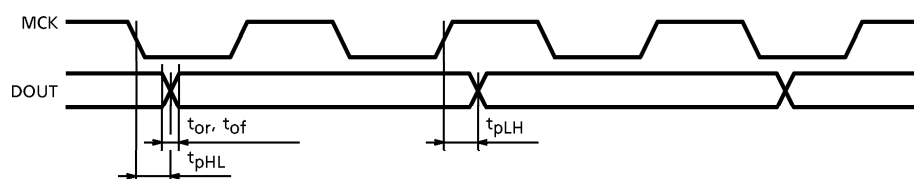
(6) Status signal output timing

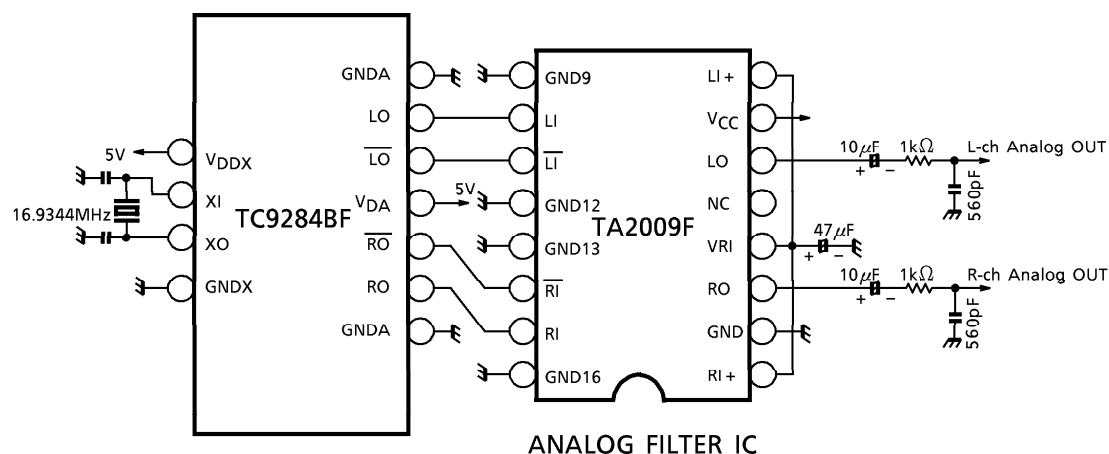
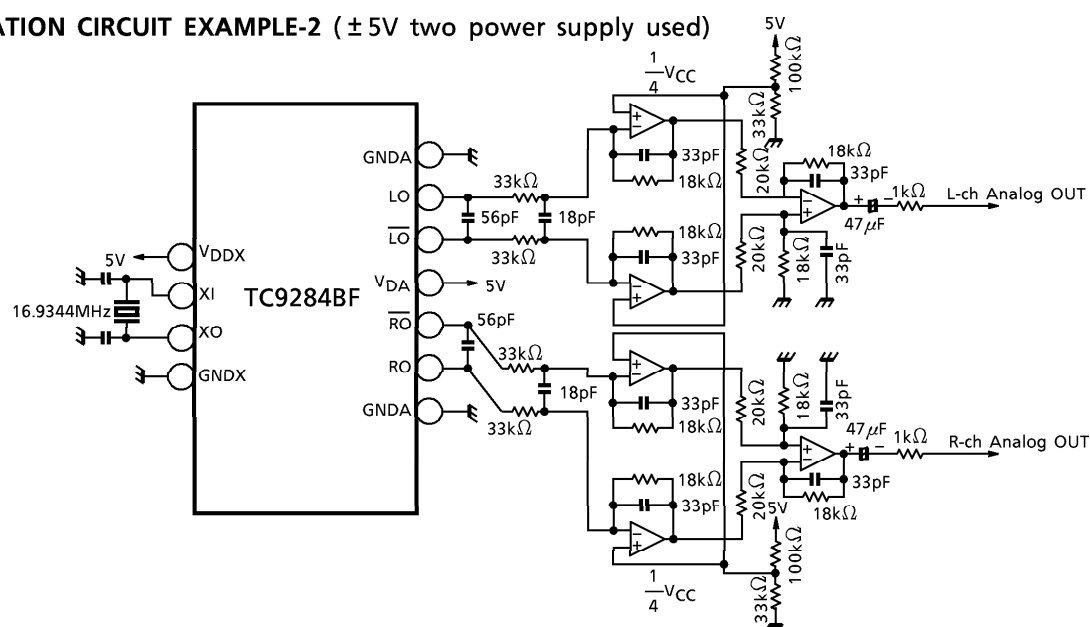
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Hold Time	"H" Level	t_{HDH}	—	WDCK→SPDA	—	—	200	ns
	"L" Level	t_{HDL}	—		—	—	200	
Output Rising Time		t_{or}	—	SPDA	—	—	40	ns
Output Falling Time		t_{of}	—		—	—	40	



(7) Digital out output timing

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer Time	"H" Level	t_{pHL}	—	MCK→DOUT	—	—	60	ns
	"L" Level	t_{pLH}	—		—	—	60	
Output Rising Time		t_{or}	—	DOUT	—	—	14	ns
Output Falling Time		t_{of}	—		—	—	14	



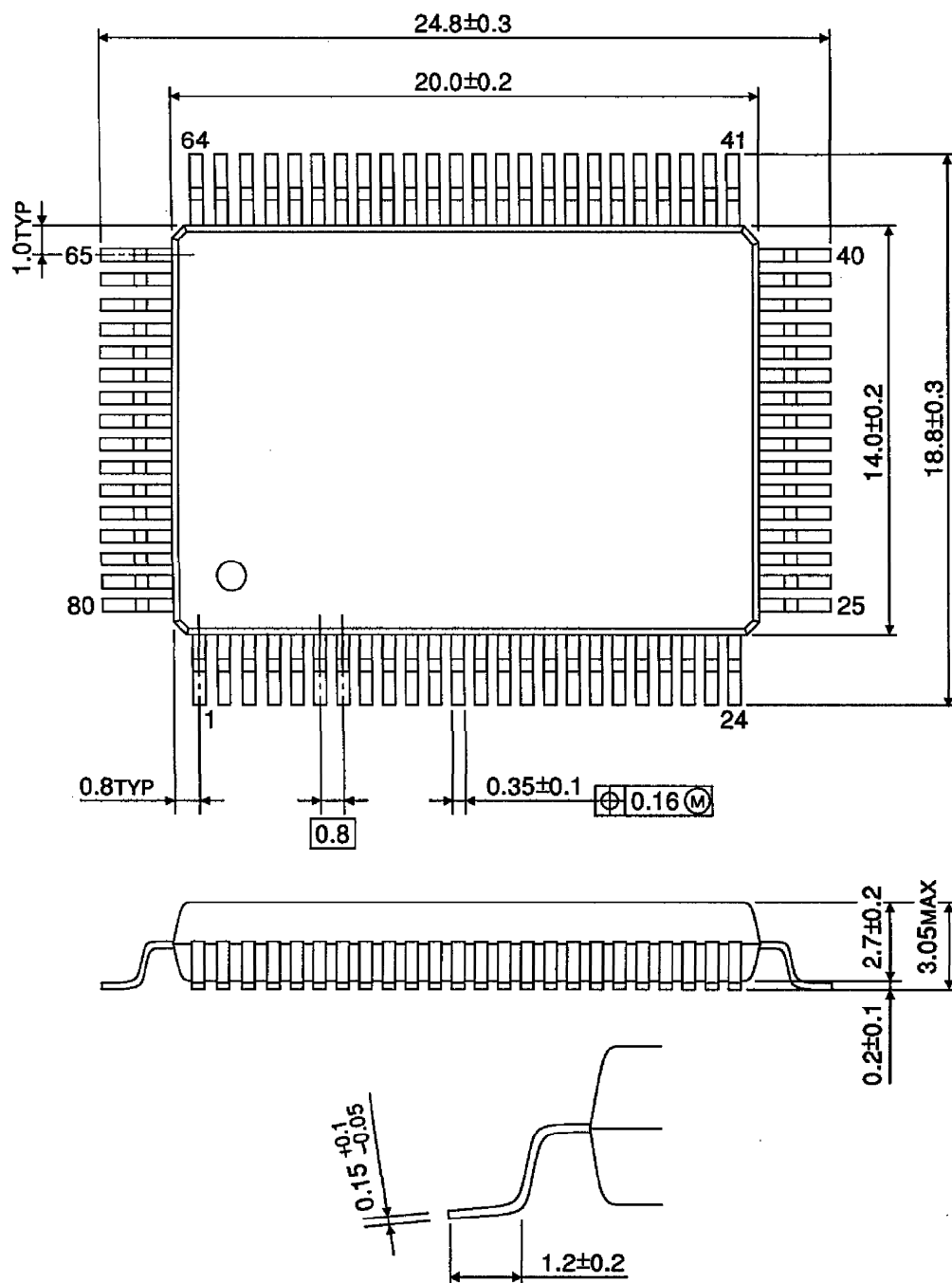
APPLICATION CIRCUIT EXAMPLE-1 (+5V single power supply used)

ANALOG FILTER IC
APPLICATION CIRCUIT EXAMPLE-2 (±5V two power supply used)

(Cautions)

- Quality of crystal oscillation wave form largely affect S/N ratio and noise distortion. Further, this is also true then system clock is input externally through the XI terminal.
- The wiring between the TC9284BF output and the TA2009F input must be made the shortest.
- The condenser between VDD and GND shall be connected as close to the pin as possible.

OUTLINE DRAWING

QFP80-P-1420-0.80A

Unit : mm



Weight : 1.57g (Typ.)