

SN54LS224A, SN74LS224A 16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

- Independent Synchronous Inputs and Outputs
- 16 Words by 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates up to 10 MHz
- Fall-Through Time 50 ns Typical
- Data Terminals Arranged for Printed Circuit Board Layout
- Expandable, Using External Gating
- Packaged in Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Chip Carriers (FK)

description

The SN54LS224A and SN74LS224A 64-bit, low-power Schottky memories are organized as 16 words by 4 bits each. They can be expanded in multiples of $15m + 1$ words or $4n$ bits, or both (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array); however, some external gating is required. For longer words, the input-ready (IR) signals of the first-rank packages and output-ready (OR) signals of the last-rank packages must be ANDed for proper synchronization.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written to and read from its array at independent data rates. These FIFOs are designed to process data at rates up to 10 MHz in a bit-parallel format, word by word.

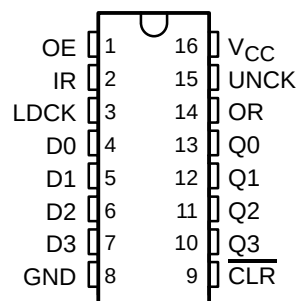
The load clock (LDCK) normally is held low, and data is written into memory on the high-to-low transition of LDCK. The unload clock (UNCK) normally is held high, and data is read out on the low-to-high transition of UNCK. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the IR and OR flags that indicate not-full and not-empty conditions. IR is high only when the memory is not full and LDCK is low. OR is high only when the memory is not empty and UNCK is high.

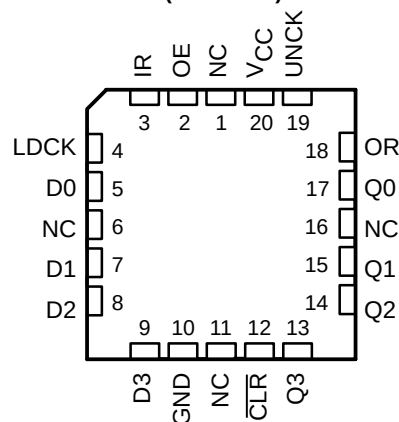
A low level on the clear ($\overline{\text{CLR}}$) input resets the internal stack-control pointers and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting, with respect to the data inputs, and are at high impedance when the output-enable (OE) input is low. OE does not affect the IR and OR outputs.

The SN74LS224A is characterized for operation from 0°C to 70°C. The SN54LS224A is characterized over the full military temperature range of –55°C to 125°C.

SN54LS224A . . . J PACKAGE
SN74LS224A . . . N PACKAGE
(TOP VIEW)



SN54LS224A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

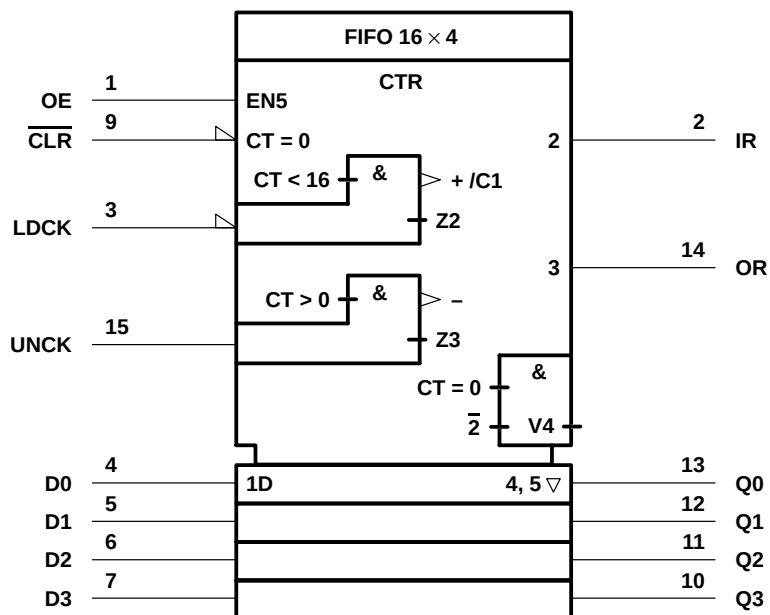
SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. This symbol is functionally accurate, but does not show the details of implementation; for these details, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0. Pin numbers shown are for the J and N packages.

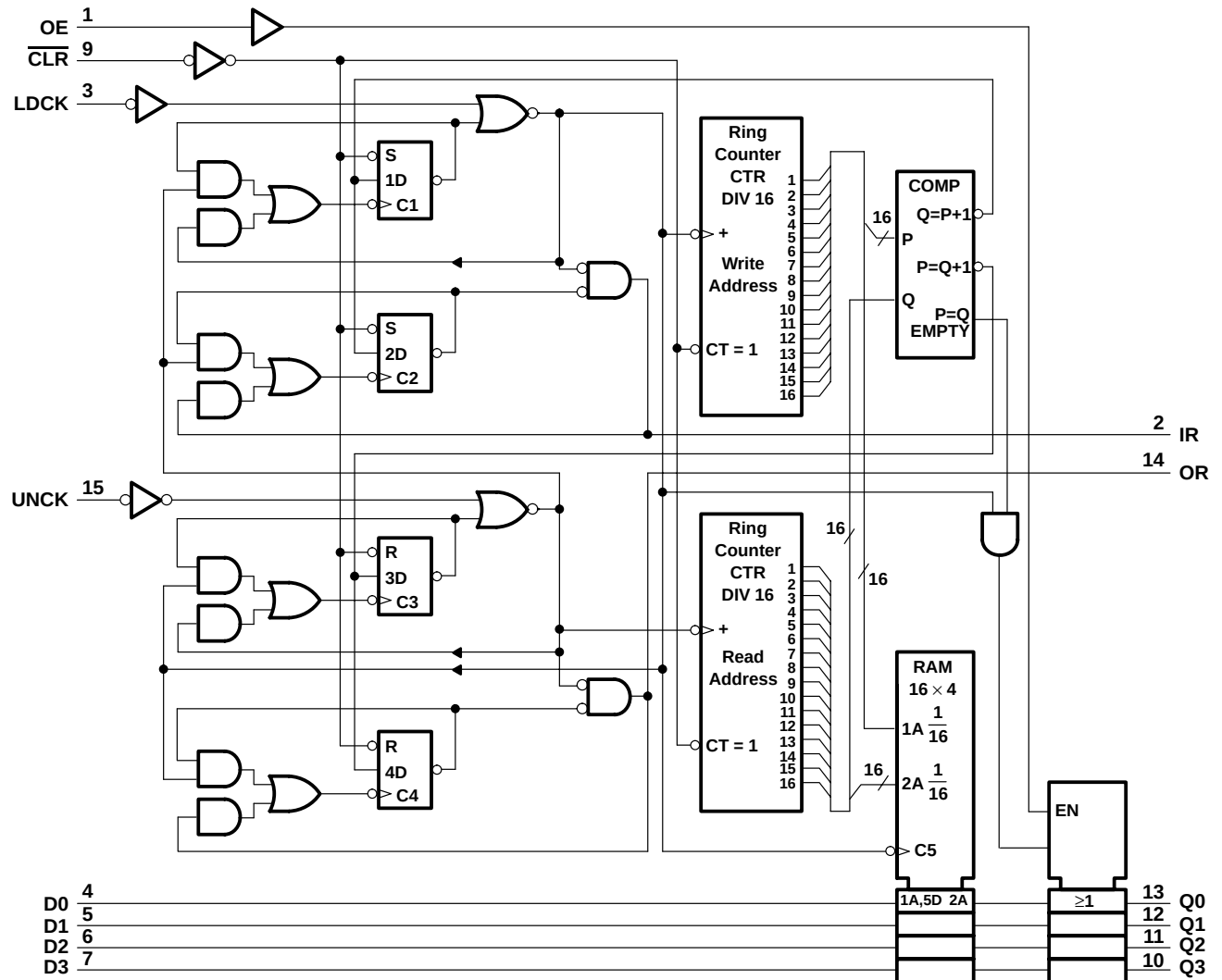
SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

logic diagram (positive logic)



Pin numbers shown are for the J and N packages.

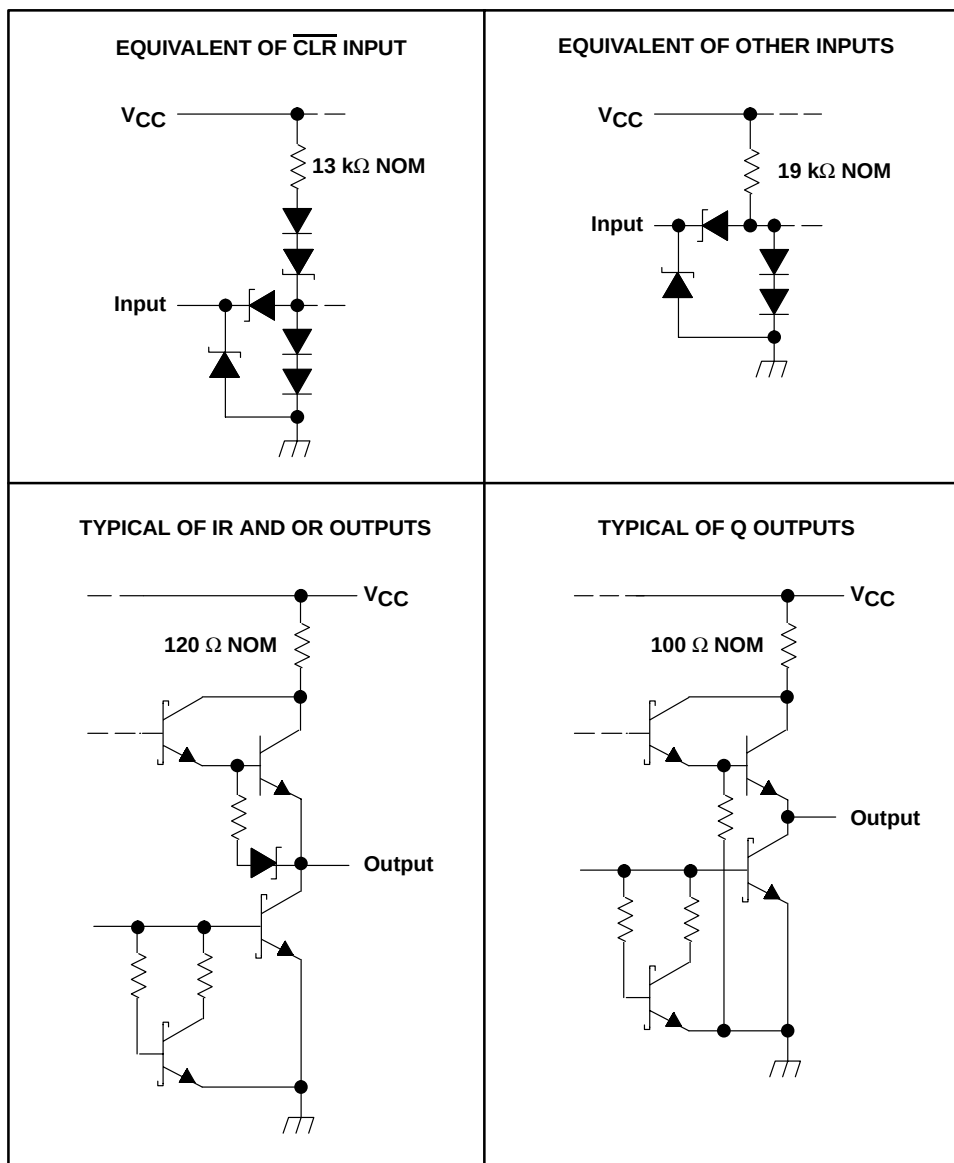
SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

schematics of inputs and outputs



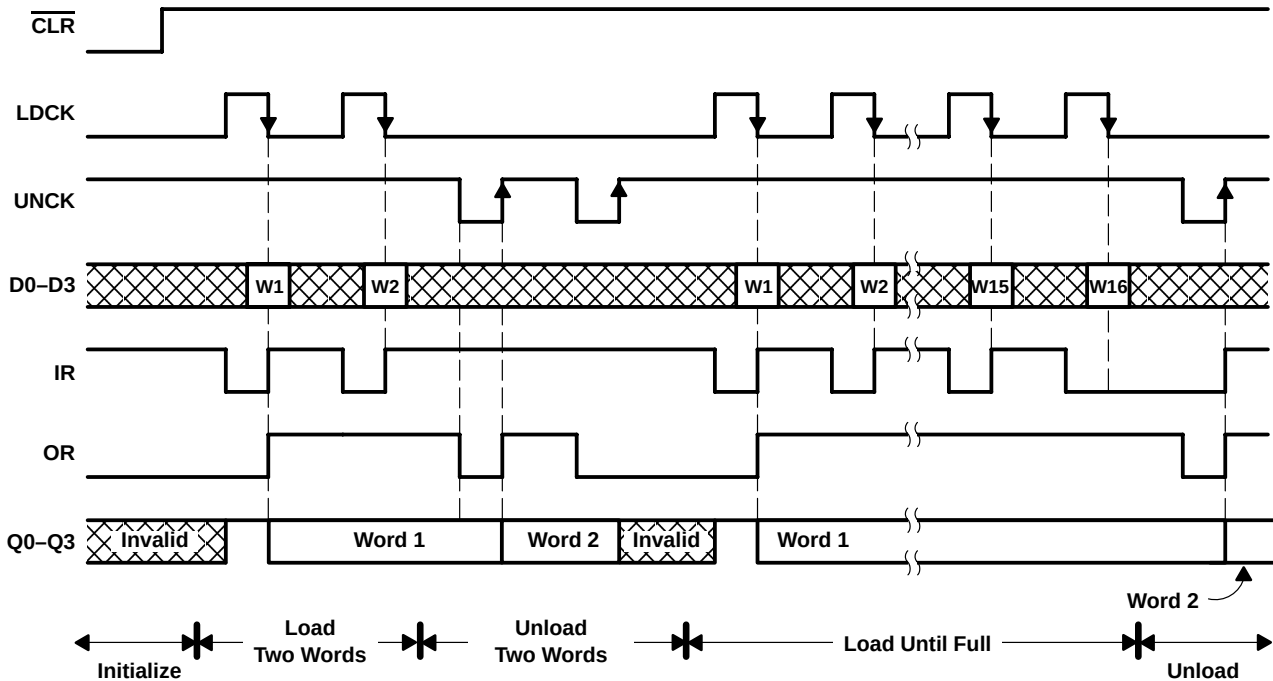
SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input voltage range, V_I	–0.5 V to 7 V
Off-state output voltage range, V_O	–0.5 V to 5.5 V
Package thermal impedance, θ_{JA} : N package (see Note 2)	67°C/W
N package (see Note 3)	88°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

3. The package thermal impedance is calculated in accordance with JESD 51-3.

SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

recommended operating conditions (see Note 4)

			SN54LS224A			SN74LS224A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current	Q outputs	−1			−2.6			mA
		IR, OR	−0.4			−0.4			
I _{OL}	Low-level output current	Q outputs	12			24			mA
		IR, OR	4			8			
T _A	Operating free-air temperature		−55	125		0	70		°C

NOTE 4: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS224A			SN74LS224A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN,	I _I = –18 mA			–1.5			–1.5	V
V _{OH}	Q outputs	V _{CC} = MIN	I _{OH} = –2.6 mA				2.4	3.4		V
	IR, OR	V _{CC} = MIN,	I _{OH} = –0.4 mA	2.4	3.3					
V _{OL}	Q outputs	V _{CC} = MIN	I _{OL} = 12 mA	0.25	0.4		0.25	0.4		V
			I _{OL} = 24 mA				0.35	0.5		
	IR, OR	V _{CC} = MIN	I _{OL} = 4 mA	0.25	0.4		0.25	0.4		
			I _{OL} = 8 mA				0.35	0.5		
I _{OZH}	Q outputs	V _{CC} = MAX,	V _O = 2.7 V			20			20	μA
I _{OZL}	Q outputs	V _{CC} = MAX,	V _O = 0.4 V			–20			–20	μA
I _I		V _{CC} = MAX,	V _I = 7 V			0.1			0.1	mA
I _{IH}		V _{CC} = MAX,	V _I = 2.7 V			20			20	μA
I _{IL}		V _{CC} = MAX,	V _I = 0.4 V			–0.4			–0.4	mA
I _{OS} §	Q outputs	V _{CC} = MAX		–30		–130	–30		–130	mA
	IR, OR			–20		–100	–20		–100	
I _{CC}	V _{CC} = MAX		Outputs high	84	135		84	135		mA
			Outputs low	87	155		87	155		
			Outputs disabled	89	155		89	155		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.



SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

timing requirements over recommended operating conditions (see Note 4 and Figure 1)

		SN54LS224A		SN74LS224A		UNIT
		MIN	MAX	MIN	MAX	
t_W Pulse duration	LDCK high	60		60		ns
	LDCK low	15		15		
	UNCK low	30		30		
	UNCK high	30		30		
	CLR low	20		20		
t_{su} Setup time	Data to LDCK↓	50		50		ns
	LDCK↓ before UNCK↓	50		50		
	UNCK↑ before LDCK↑	50		50		
t_h Hold time	Data from LDCK↓	10		10		ns

NOTE 4: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL} , V_{IH} , or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	LDCK↓	IR	R _L = 2 kΩ, C _L = 15 pF	25	40	ns	
t _{PHL}	LDCK↑			36	50		
t _{PLH}	LDCK↓	OR	R _L = 2 kΩ, C _L = 15 pF	48	70	ns	
t _{PLH}	UNCK↑	OR	R _L = 2 kΩ, C _L = 15 pF	29	45	ns	
t _{PHL}	UNCK↓			28	45		
t _{PLH}	UNCK↑	IR	R _L = 2 kΩ, C _L = 15 pF	49	70	ns	
t _{PLH}	$\overline{\text{CLR}}\downarrow$	IR	R _L = 2 kΩ, C _L = 15 pF	36	55	ns	
t _{PHL}		OR		25	40		
t _{PHL}	LDCK↓	Q	R _L = 667 Ω, C _L = 45 pF	34	50	ns	
t _{PLH}	UNCK↑	Q	R _L = 667 Ω, C _L = 45 pF	54	80	ns	
t _{PHL}				45	70		
t _{PZL}	OE↑	Q	R _L = 667 Ω, C _L = 45 pF	22	35	ns	
t _{PZH}				21	35		
t _{PLZ}	OE↓	Q	R _L = 667 Ω, C _L = 5 pF	16	30	ns	
t _{PHZ}				18	30		

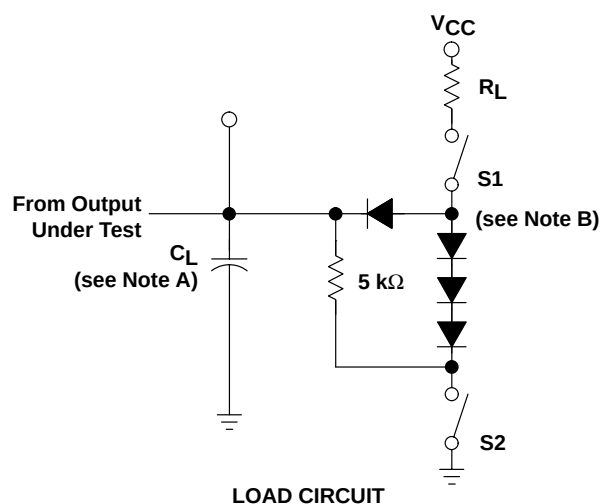
SN54LS224A, SN74LS224A

16 × 4 SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

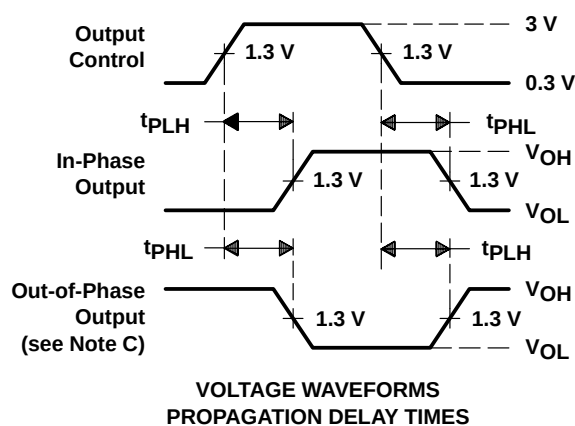
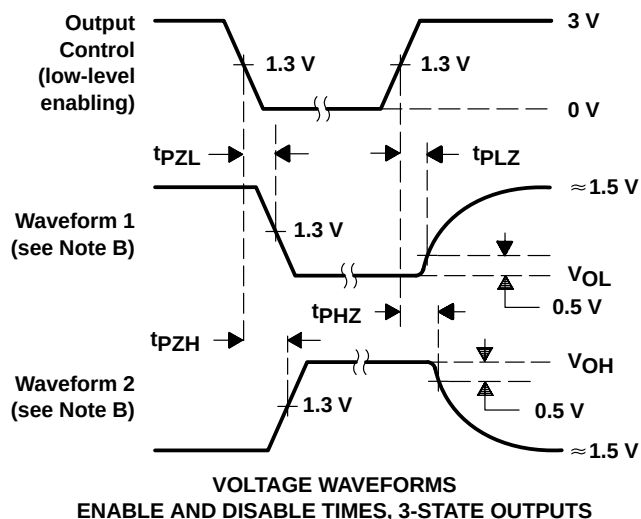
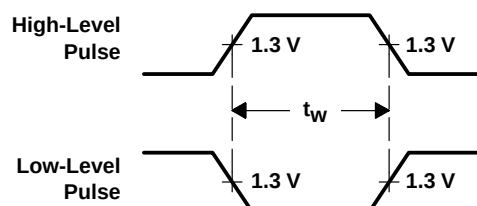
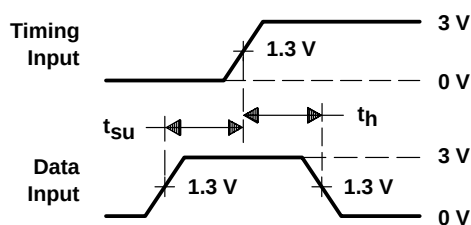
WITH 3-STATE OUTPUTS

SDLS023E – JANUARY 1991 – REVISED APRIL 2003

PARAMETER MEASUREMENT INFORMATION



TEST	S1	S2
t_{pZL}	Closed	Open
t_{pZH}	Open	Closed
t_{pLZ}/t_{pHZ}	Closed	Closed
t_{pLH}/t_{pHL}	Closed	Closed



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r < 15$ ns, $t_f < 6$ ns, $Z_O \approx 50 \Omega$.
 D. All diodes are 1N916 or 1N3064.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54LS224AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS224AN	ACTIVE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS224AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54LS224AFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS224AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

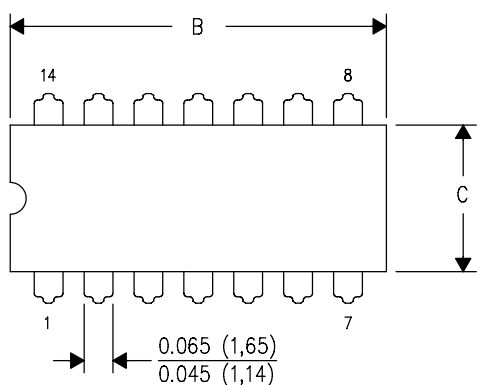
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

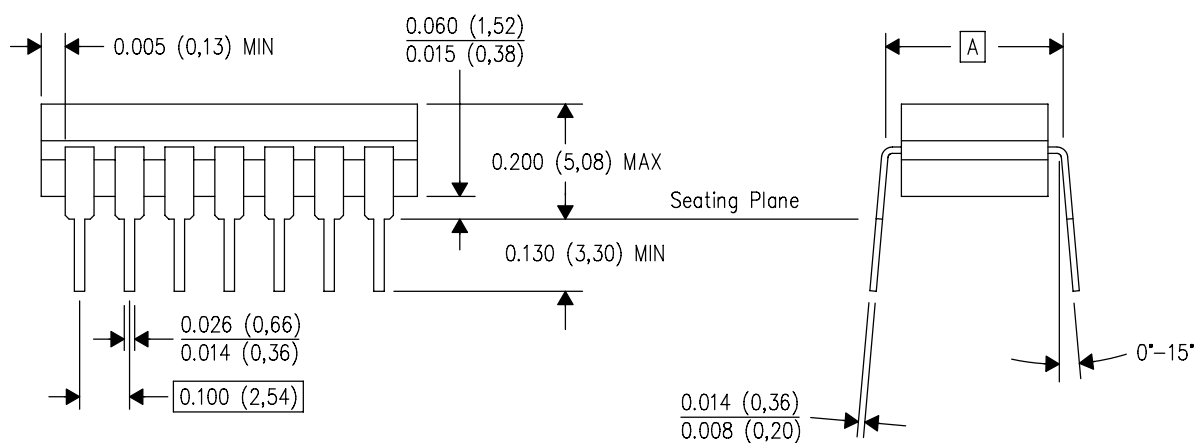
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



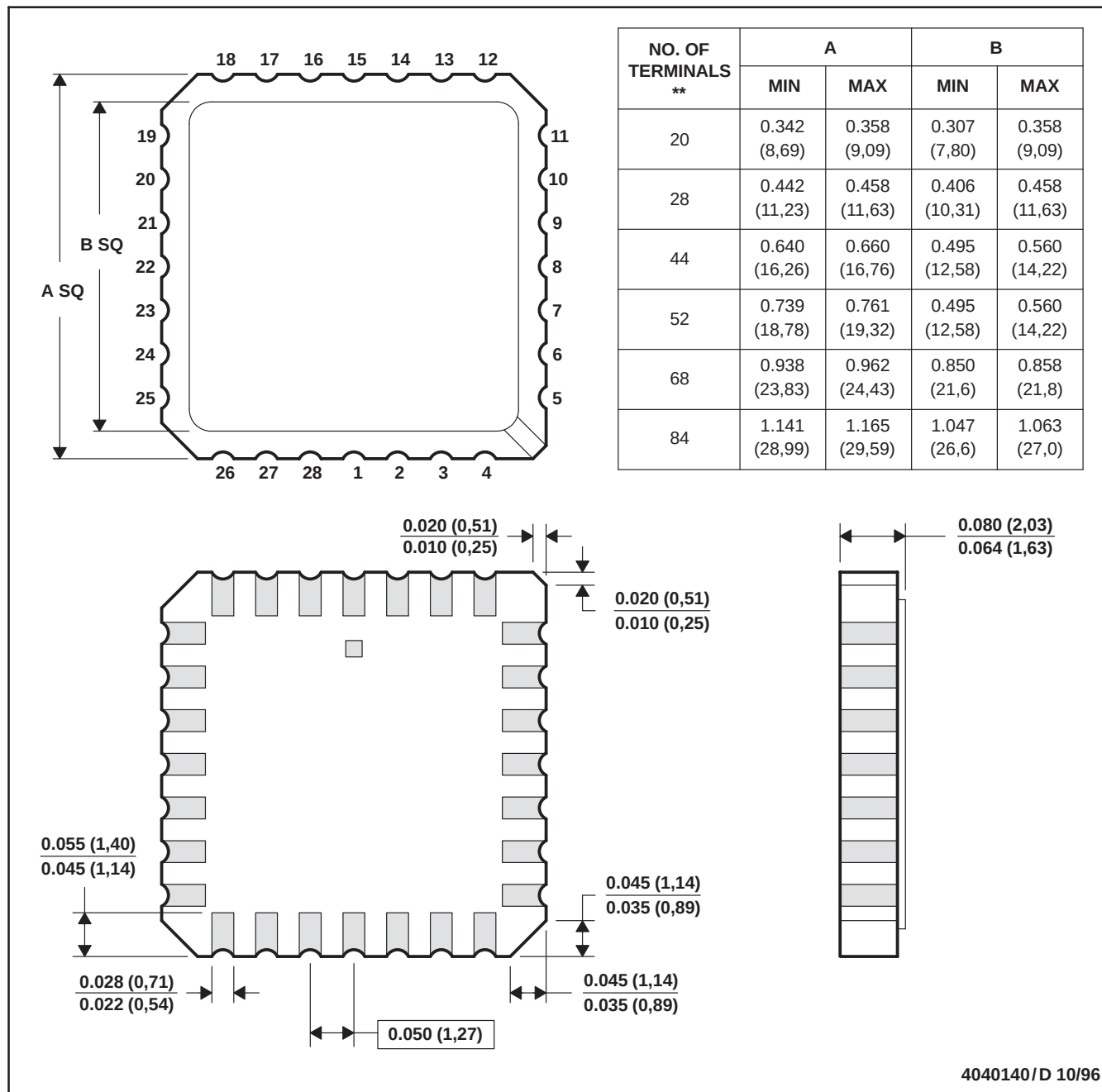
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

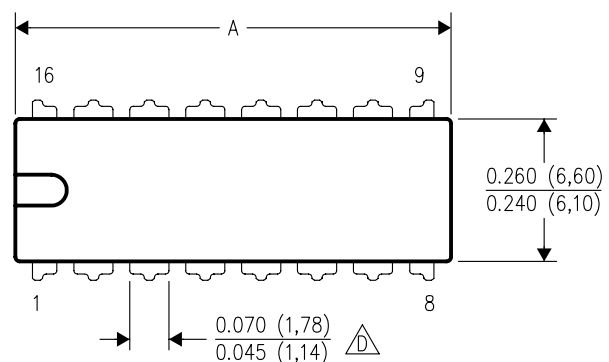


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

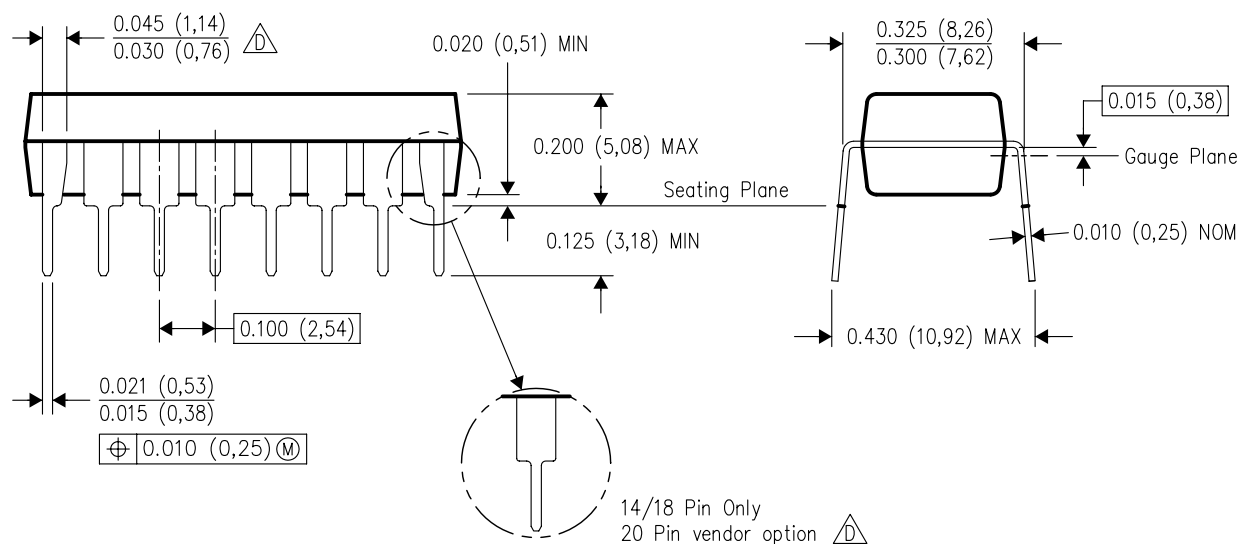
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated