

IR21303C

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 11.1 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic

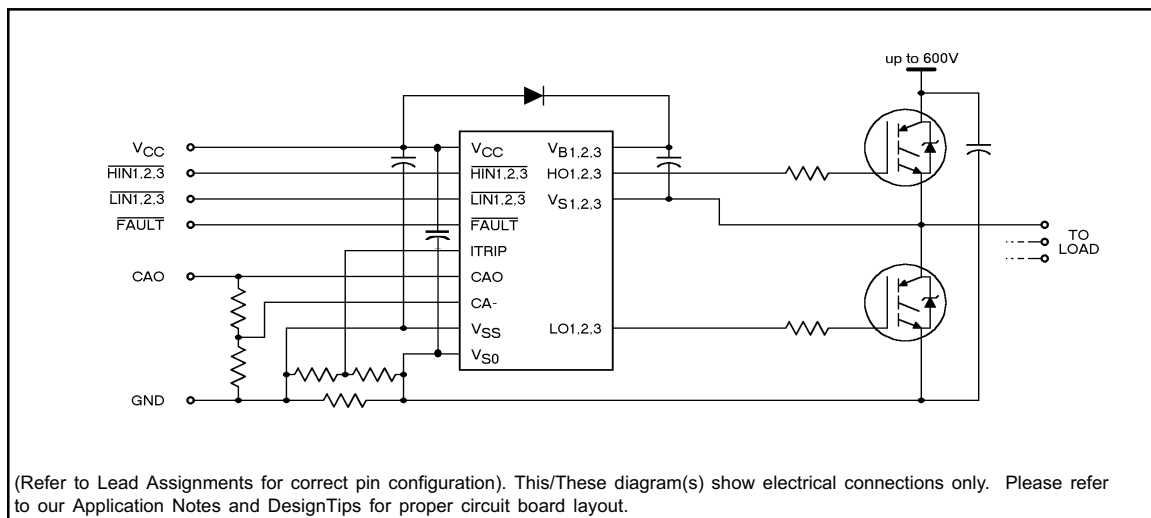
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	11.1 - 20V
t_{on/off} (typ.)	675 & 425 ns
Deadtime (typ.)	600 ns

Description

The IR21303C is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain $\overline{\text{FAULT}}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{S0} . The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	625	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	$V_{CC} - 25$	$V_{CC} + 0.3$	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage (HIN1,2,3, LIN1,2,3 & ITRIP)	$V_{SS} - 0.3$	($V_{SS} + 15$) or ($V_{CC} + 0.3$) whichever is lower	
V_{FLT}	FAULT Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{CAO}	Operational Amplifier Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{CA-}	Operational Amplifier Inverting Input Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
T_J	Junction Temperature	—	150	°C

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0} . The V_S offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3} + 13.3$	$V_{S1,2,3} + 20$	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	13.3	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage (HIN1,2,3, LIN1,2,3 & ITRIP)	V_{SS}	$V_{SS} + 5$	
V_{FLT}	FAULT Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	$V_{SS} + 5$	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	$V_{SS} + 5$	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of ($V_{S0} - 5V$) to ($V_{S0} + 600V$). Logic state held for V_S of ($V_{S0} - 5V$) to ($V_{S0} - V_{BS}$). (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} , C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	11	450	675	850	ns	$V_{IN} = 0$ & 5V $V_{S1,2,3} = 0$ to 600V
t_{off}	Turn-Off Propagation Delay	12	300	425	550		
t_r	Turn-On Rise Time	13	—	80	125		
t_f	Turn-Off Fall Time	14	—	35	55		
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	15	400	660	920		V_{IN} , $V_{ITRIP} = 0$ & 5V
t_{bl}	ITRIP Blanking Time	—	—	400	—		$V_{ITRIP} = 1V$
t_{flt}	ITRIP to $\overline{FAULT}$ Indication Delay	16	335	590	845		V_{IN} , $V_{ITRIP} = 0$ & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	—	310	—	ns	$V_{IN} = 0$ & 5V
t_{fltclr}	LIN1,2,3 & HIN1,2,3 to $\overline{FAULT}$ Clear Time	17	6.0	9.0	12.0		V_{IN} , $V_{ITRIP} = 0$ & 5V
DT	Deadtime	—	300	600	900	V/ μ s	$V_{IN} = 0$ & 5V
SR+	Operational Amplifier Slew Rate (+)	18	4.4	6.2	—		
SR-	Operational Amplifier Slew Rate (-)	19	2.4	3.2	—		

NOTE: For high side PWM, HIN pulse width must be $\geq 1.5\mu$ sec

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	20	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	21	—	—	0.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	—	436.8	480	529.2	mV	
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	22	—	—	100		$V_{IN} = 0V$, $I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	23	—	—	100	μ A	$V_{IN} = 5V$, $I_O = 0A$
I_{LK}	Offset Supply Leakage Current	24	—	—	50		$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} Supply Current	25	—	15	30	mA	$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	26	—	3.0	4.0		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	27	—	450	650	μ A	$V_{IN} = 0V$
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	28	—	225	400		$V_{IN} = 5V$
I_{ITRIP+}	"High" ITRIP Bias Current	29	—	75	150	nA	ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	30	—	—	100		ITRIP = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	—	10.8	12	13.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	—	9	10	11		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	—	10.8	12	13.2		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	—	9.0	10	11		
$R_{on,FLT}$	$\overline{FAULT}$ Low On-Resistance	31	—	55	75	Ω	

Static Electrical Characteristics -- Continued

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: $HO1,2,3$ or $LO1,2,3$.

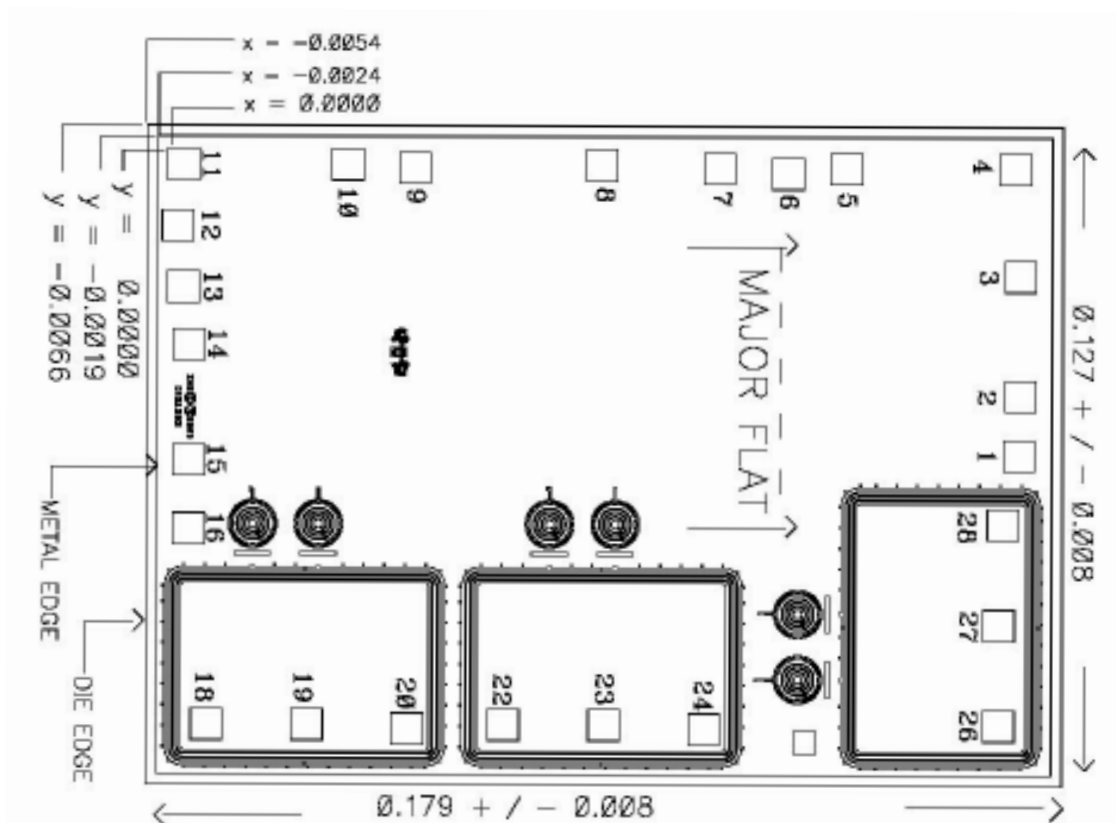
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
I_{O+}	Output High Short Circuit Pulsed Current	32	200	250	—	mA	$V_O = 0V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	33	420	500	—		$V_O = 15V$, $V_{IN} = 5V$ $PW \leq 10 \mu s$
V_{OS}	Operational Amplifier Input Offset Voltage	—	-14	—	14	mV	$V_{S0} = V_{CA-} = 0.2V$
I_{CA-}	CA- Input Bias Current	34	—	—	4.0	nA	$V_{CA-} = 2.5V$
CMRR	Op. Amp. Common Mode Rejection Ratio	35	60	80	—	dB	$V_{S0}=V_{CA-}=0.1V$ & $5V$
PSRR	Op. Amp. Power Supply Rejection Ratio	36	55	75	—		$V_{S0} = V_{CA-} = 0.2V$ $V_{CC} = 14V$ & $20V$
$V_{OH,AMP}$	Op. Amp. High Level Output Voltage	37	5.0	5.2	5.4	V	$V_{CA-} = 0V$, $V_{S0} = 1V$
$V_{OL,AMP}$	Op. Amp. Low Level Output Voltage	38	—	—	20	mV	$V_{CA-} = 1V$, $V_{S0} = 0V$
$I_{SRC,AMP}$	Op. Amp. Output Source Current	39	2.3	4.0	—	mA	$V_{CA-} = 0V$, $V_{S0} = 1V$ $V_{CAO} = 4V$
$I_{SINK,AMP}$	Op. Amp. Output Sink Current	40	1.0	2.1	—		$V_{CA-} = 1V$, $V_{S0} = 0V$ $V_{CAO} = 2V$
$I_{O+,AMP}$	Operational Amplifier Output High Short Circuit Current	41	—	4.5	6.5		$V_{CA-} = 0V$, $V_{S0} = 5V$ $V_{CAO} = 0V$
$I_{O-,AMP}$	Operational Amplifier Output Low Short Circuit Current	42	—	3.2	5.2		$V_{CA-} = 5V$, $V_{S0} = 0V$ $V_{CAO} = 5V$

Lead Definitions

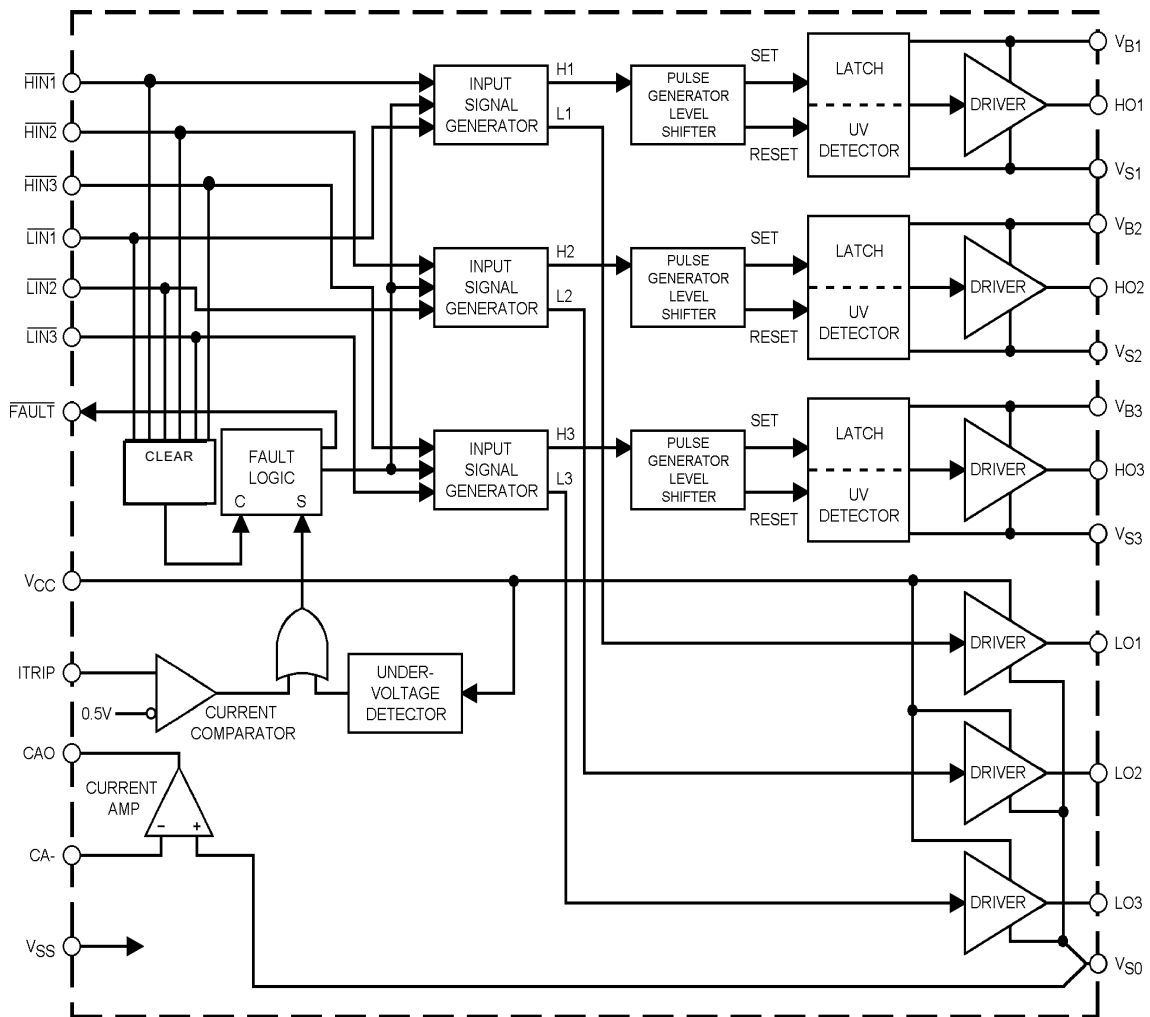
Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs ($HO1,2,3$), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output ($LO1,2,3$), out of phase
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
$HO1,2,3$	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
$LO1,2,3$	Low side gate drive outputs
V_{S0}	Low side return and positive input of current amplifier

Pad Assignments

Pin #		Pin #	
1	Vcc1	14	LO 3
2	HIN 1	15	LO 2
3	HIN 2	16	LO 1
4	HIN 3	18	VS 3
5	LIN 1	19	HO 3
6	LIN 2	20	VB 3
7	LIN 3	22	VS 2
8	FAULT	23	HO 2
9	ITRIP	24	VB 2
10	CAO	26	VS 1
11	CA-	27	HO 1
12	VSS	28	VB 1
13	VS0		



Functional Block Diagram





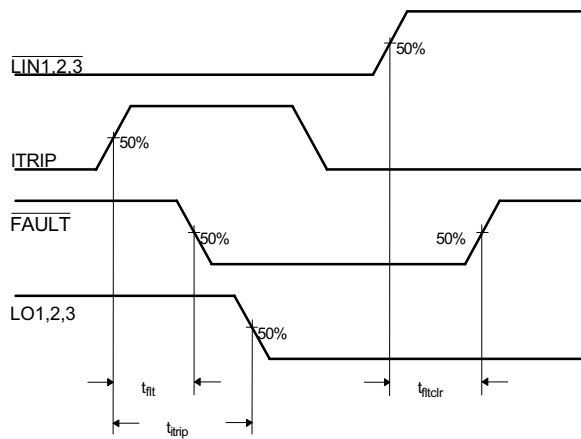


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

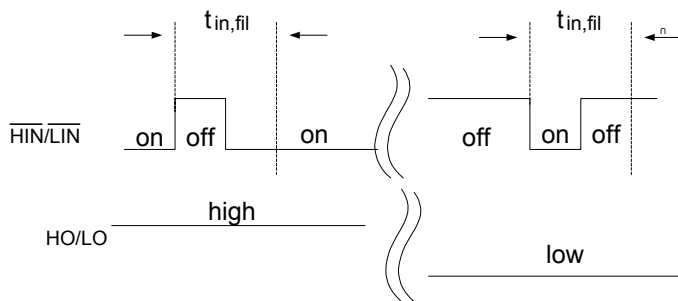


Figure 5.5 Input Filter Function

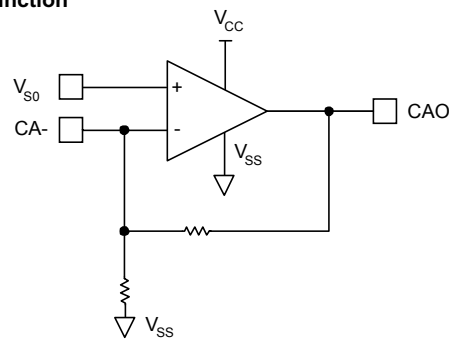


Figure 6. Diagnostic Feedback Operational Amplifier Circuit

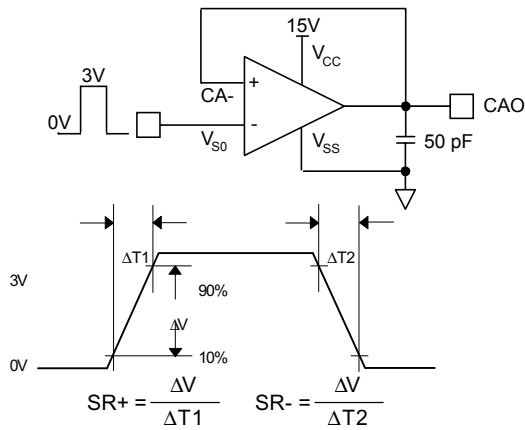


Figure 7. Operational Amplifier Slew Rate Measurement

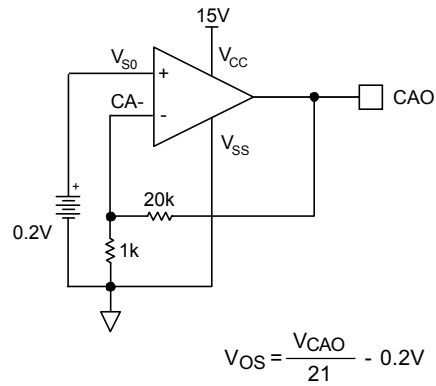


Figure 8. Operational Amplifier Input Offset Voltage Measurement

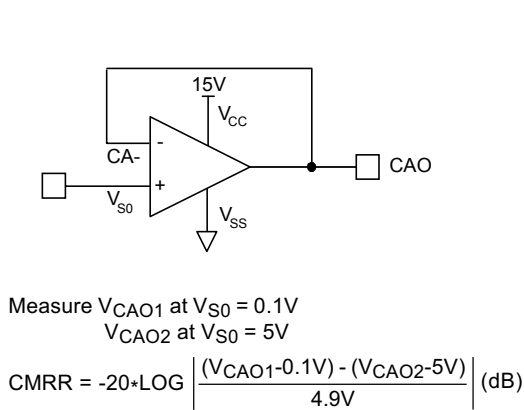


Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements

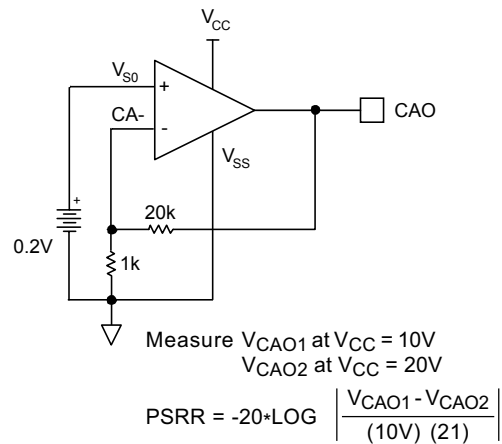


Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

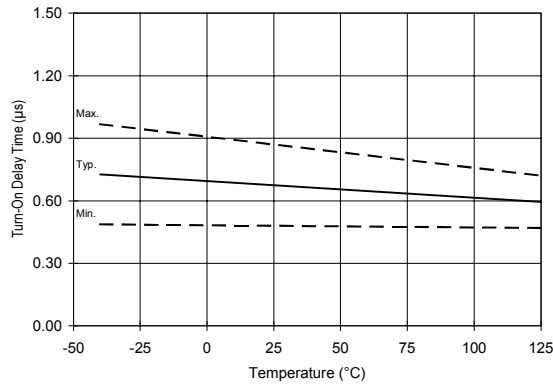


Figure 11A. Turn-On Time vs. Temperature

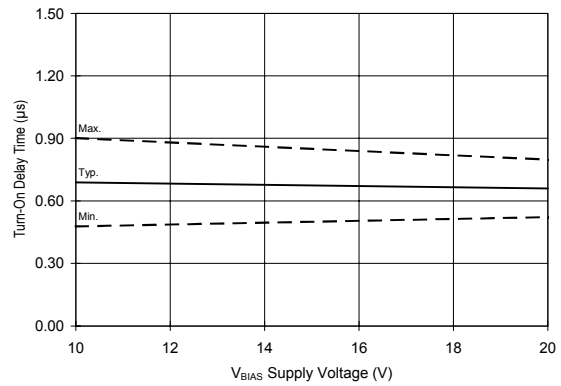


Figure 11B. Turn-On Time vs. Supply Voltage

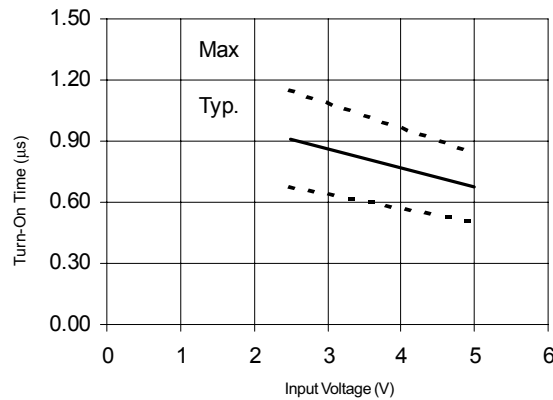


Figure 11C. Turn-On Time vs. Voltage

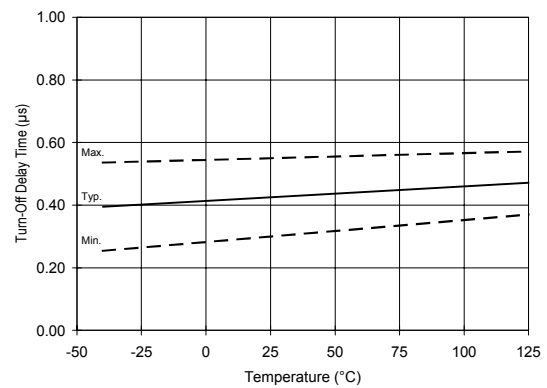


Figure 12A. Turn-Off Time vs. Temperature

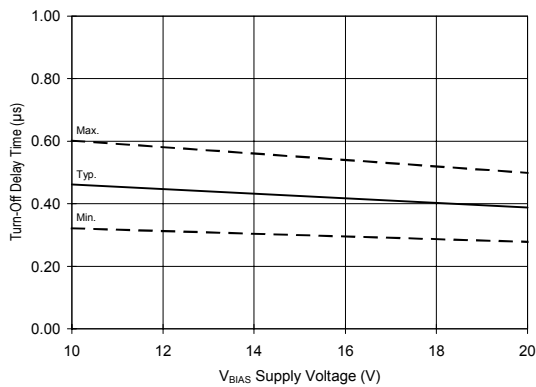


Figure 12B. Turn-Off Time vs. Supply Voltage

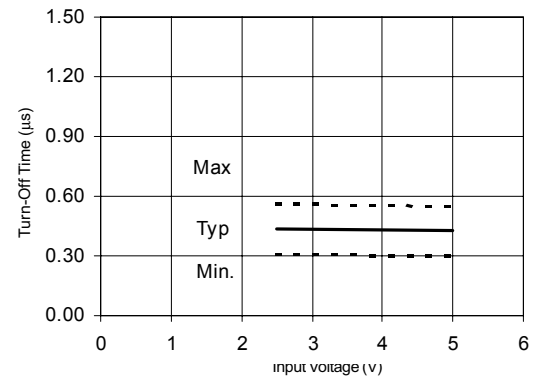


Figure 12C. Turn-Off Time vs. Input Voltage

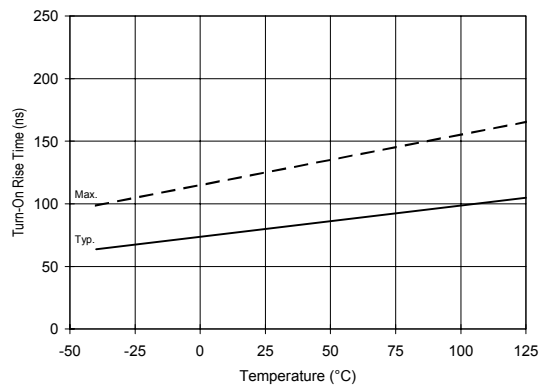


Figure 13A. Turn-On Rise Time vs. Temperature

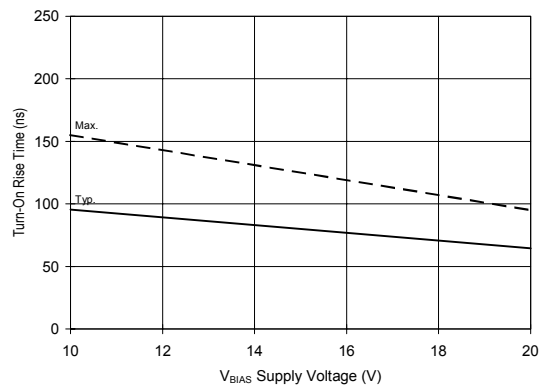


Figure 13B. Turn-On Rise Time vs. Voltage

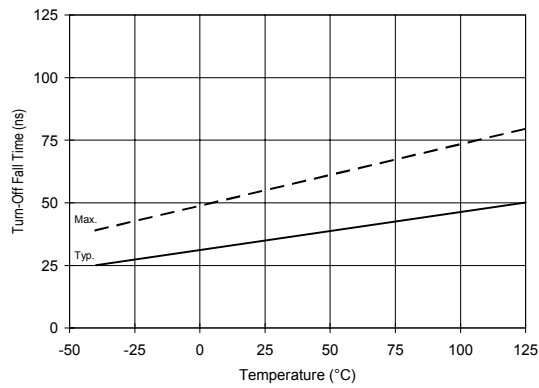


Figure 14A. Turn-Off Fall Time vs. Temperature

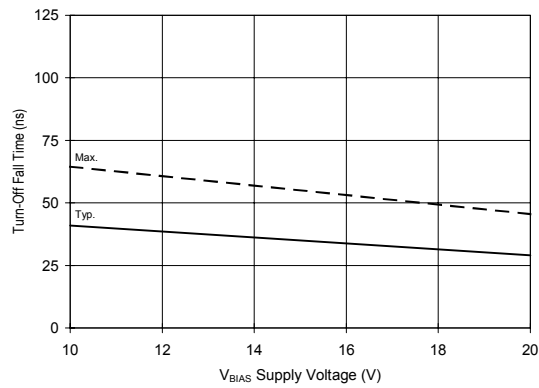


Figure 14B. Turn-Off Fall Time vs. Voltage

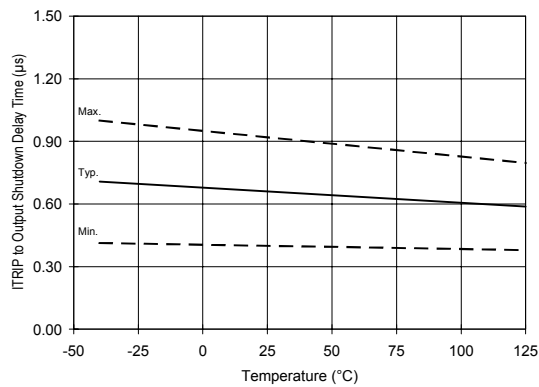


Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

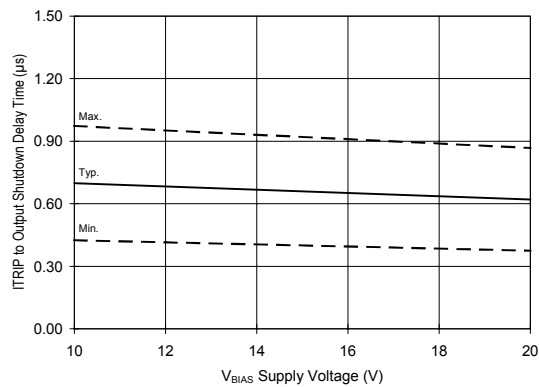


Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

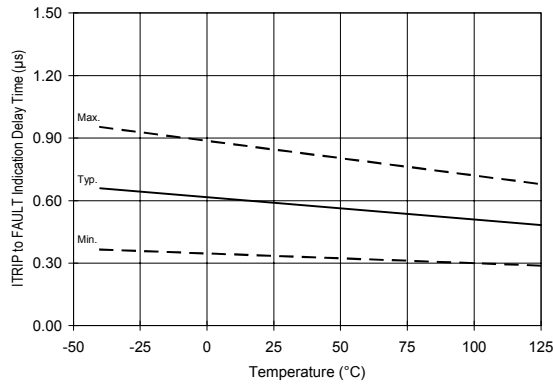


Figure 16A. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Temperature

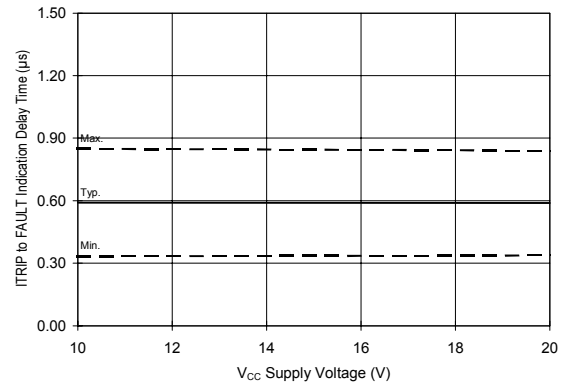


Figure 16B. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Voltage

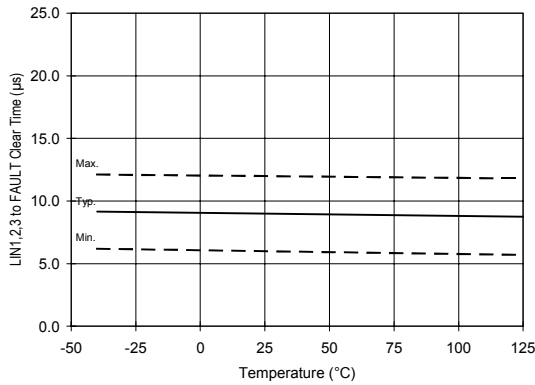


Figure 17A. $\overline{\text{LIN1,2,3}}$ & $\overline{\text{HIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Temperature

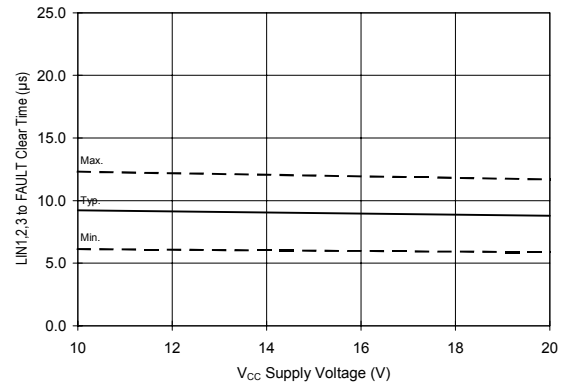


Figure 17B. $\overline{\text{LIN1,2,3}}$, $\overline{\text{HIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Voltage

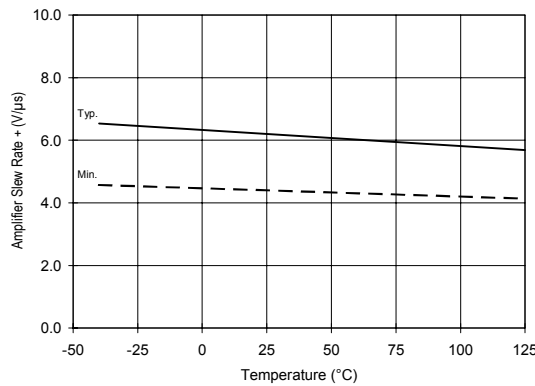


Figure 18A. Amplifier Slew Rate (+) vs. Temperature

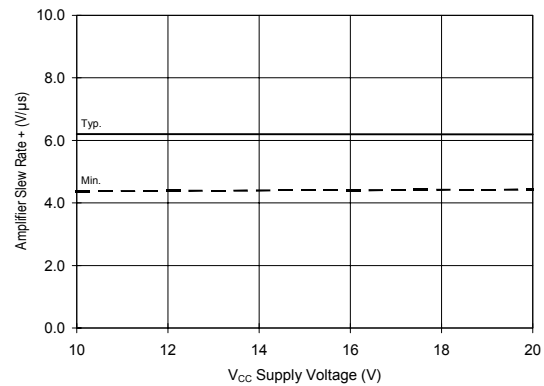


Figure 18B. Amplifier Slew Rate (+) vs. Voltage

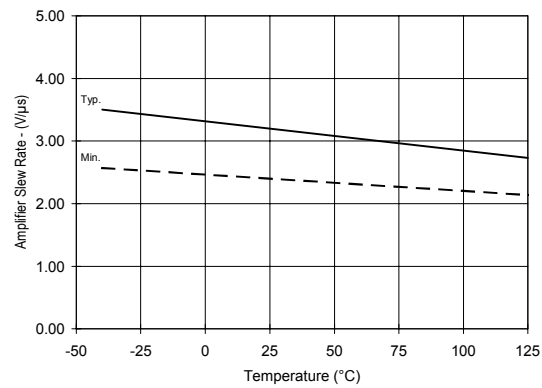


Figure 19A. Amplifier Slew Rate (-) vs. Temperature

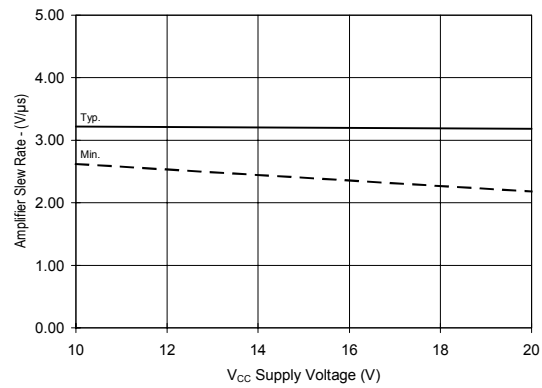


Figure 19B. Amplifier Slew Rate (-) vs. Voltage

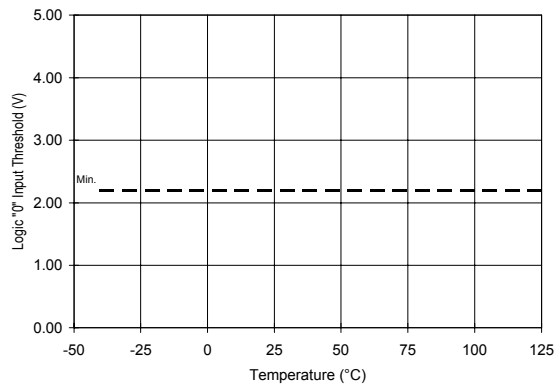


Figure 20A. Logic "0" Input Threshold vs. Temperature

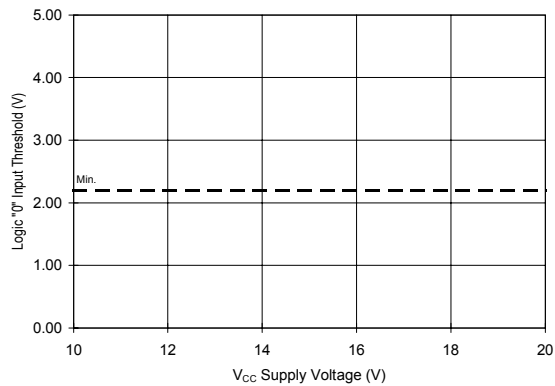


Figure 20B. Logic "0" Input Threshold vs. Voltage

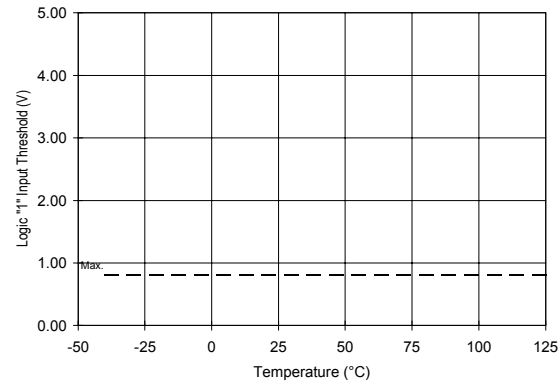


Figure 21A. Logic "1" Input Threshold vs. Temperature

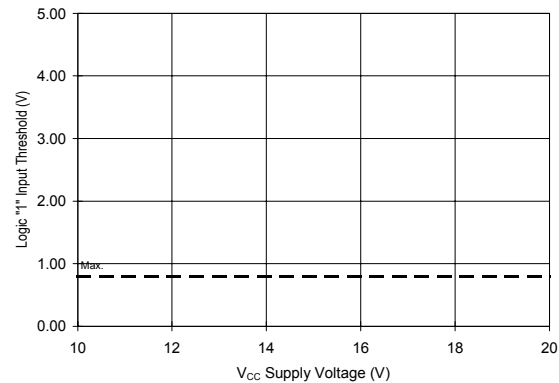


Figure 21B. Logic "1" Input Threshold vs. Voltage

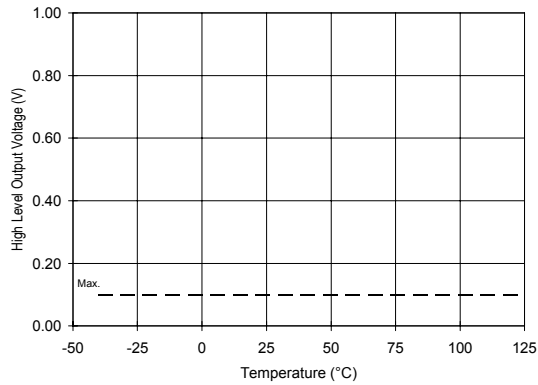


Figure 22A. High Level Output vs. Temperature

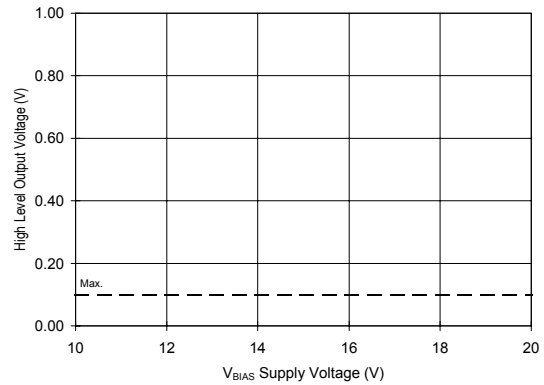


Figure 22B. High Level Output vs. Voltage

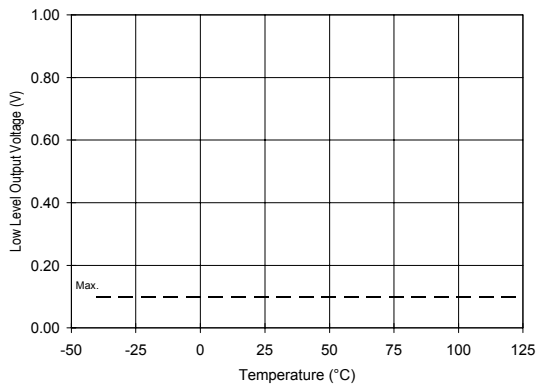


Figure 23A. Low Level Output vs. Temperature

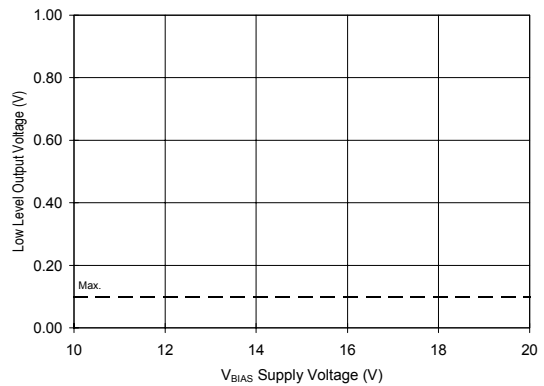


Figure 23B. Low Level Output vs. Voltage

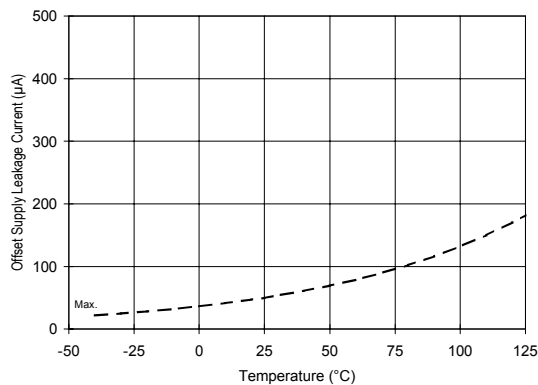


Figure 24A. Offset Supply Leakage Current vs. Temperature

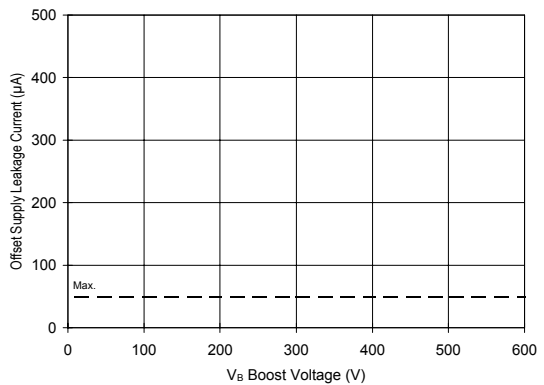


Figure 24B. Offset Supply Leakage Current vs. Voltage

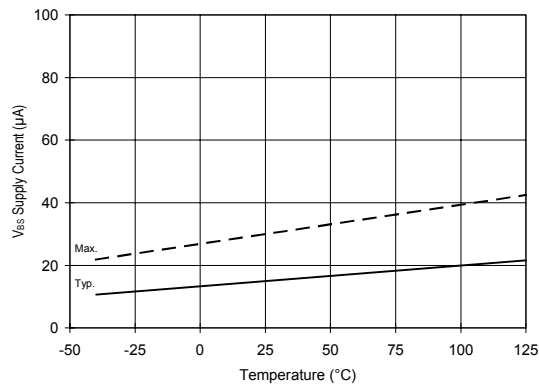


Figure 25A. V_{BS} Supply Current vs. Temperature

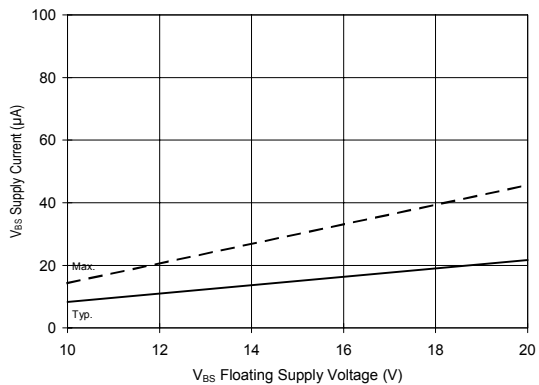


Figure 25B. V_{BS} Supply Current vs. Voltage

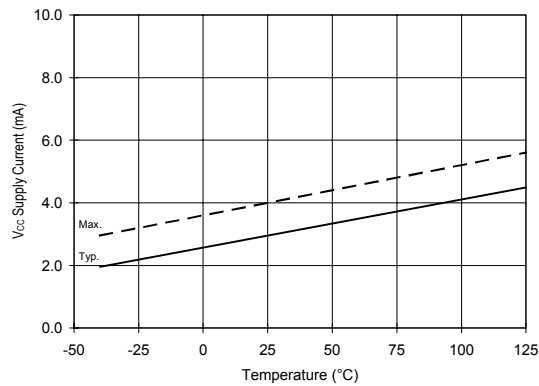


Figure 26A. V_{CC} Supply Current vs. Temperature

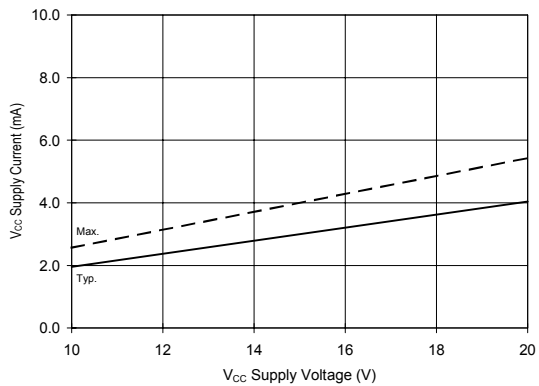


Figure 26B. V_{CC} Supply Current vs. Voltage

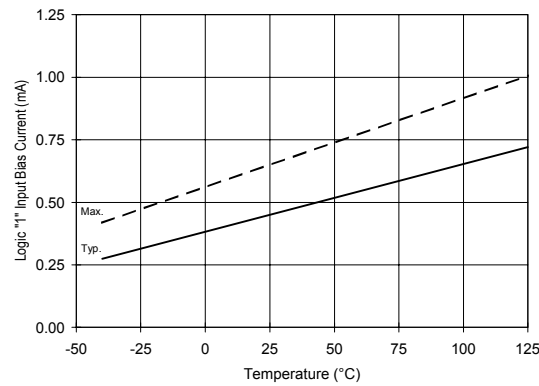


Figure 27A. Logic "1" Input Current vs. Temperature

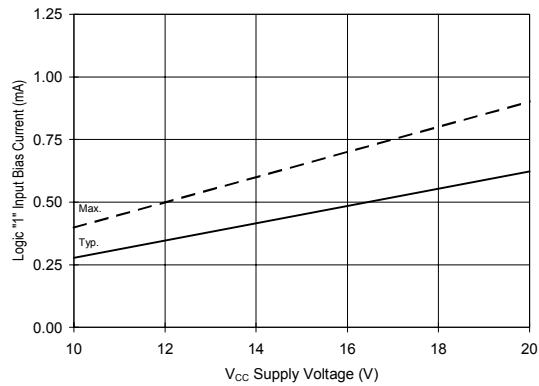


Figure 27A. Logic "1" Input Current vs. Voltage

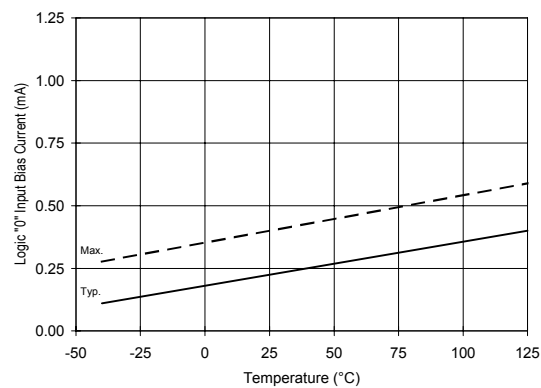


Figure 28A. Logic “0” Input Current vs. Temperature

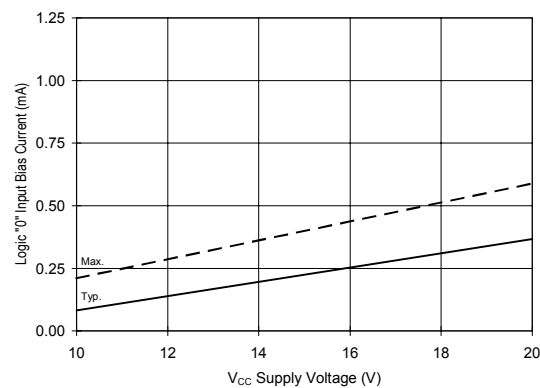


Figure 28B. Logic “0” Input Current vs. Voltage

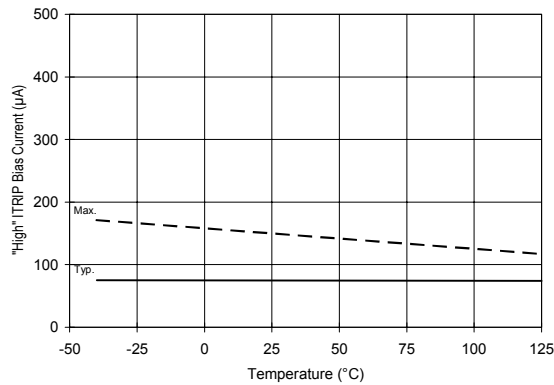


Figure 29A. “High” ITRIP Current vs. Temperature

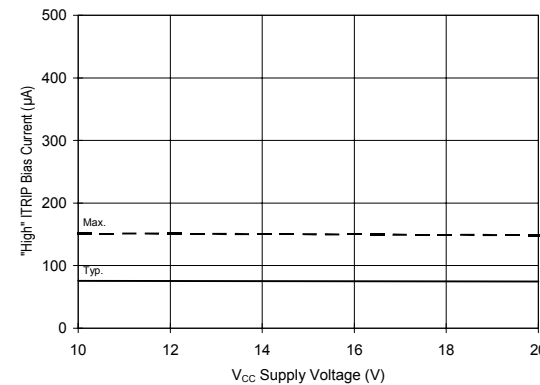


Figure 29B. “High” ITRIP Current vs. Voltage

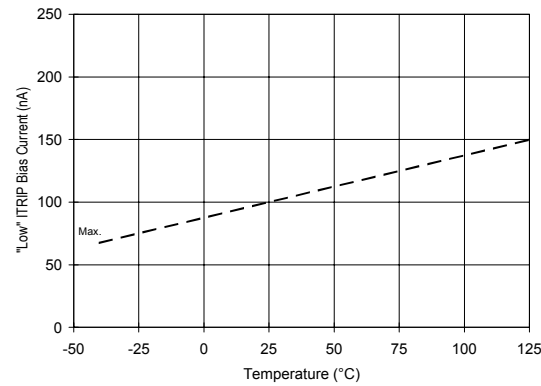


Figure 30A. “Low” ITRIP Current vs. Temperature

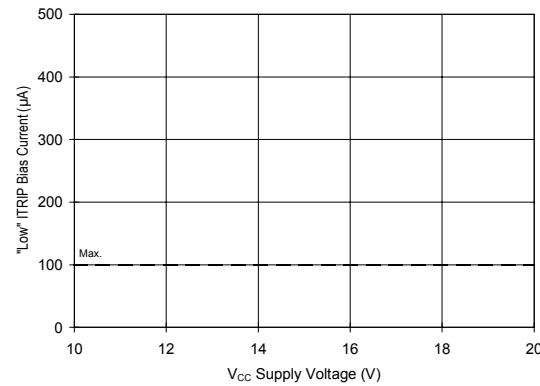


Figure 30B. “Low” ITRIP Current vs. Voltage

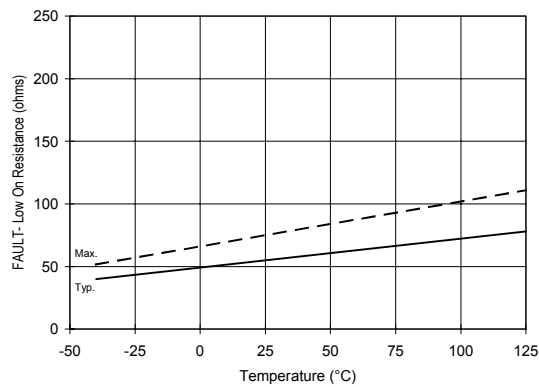


Figure 31A. $\overline{\text{FAULT}}$ Low On Resistance vs. Temperature

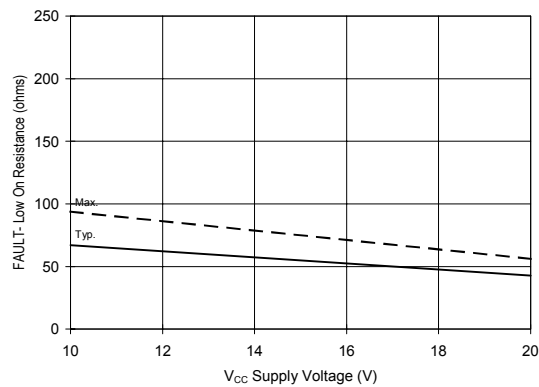


Figure 31B. $\overline{\text{FAULT}}$ Low On Resistance vs. Voltage

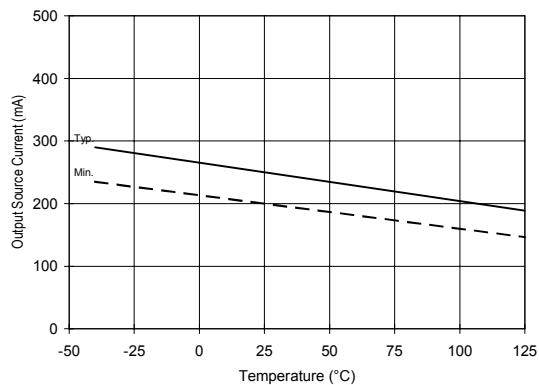


Figure 32A. Output Source Current vs. Temperature

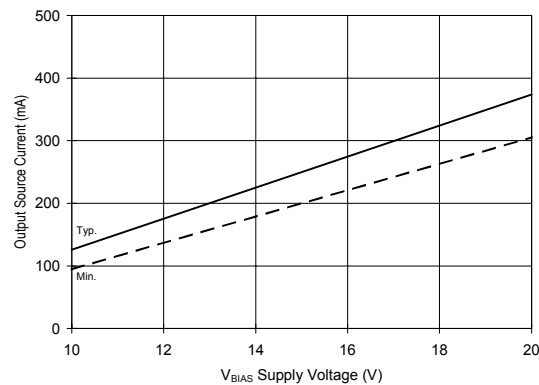


Figure 32B. Output Source Current vs. Voltage

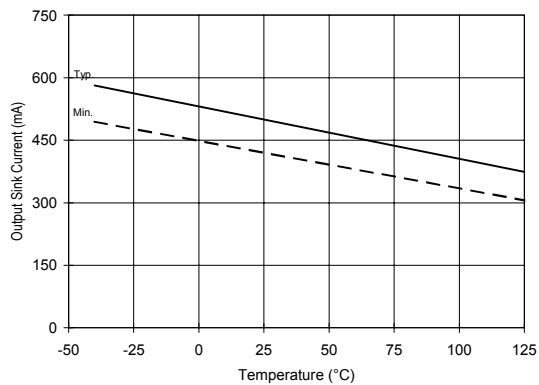


Figure 33A. Output Sink Current vs. Temperature

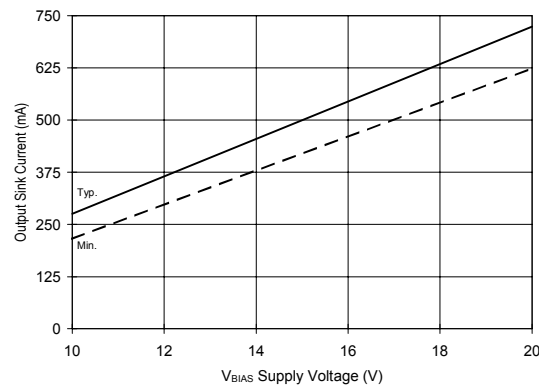


Figure 33B. Output Sink Current vs. Voltage

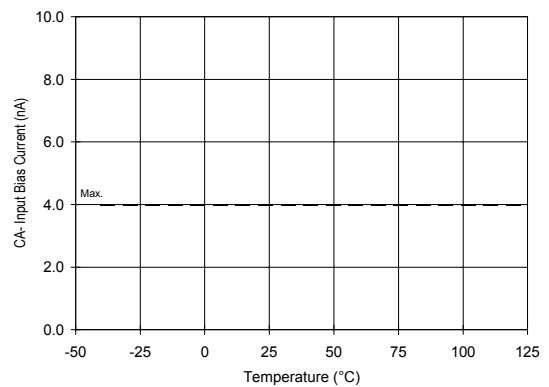


Figure 34A. CA- Input Current vs. Temperature

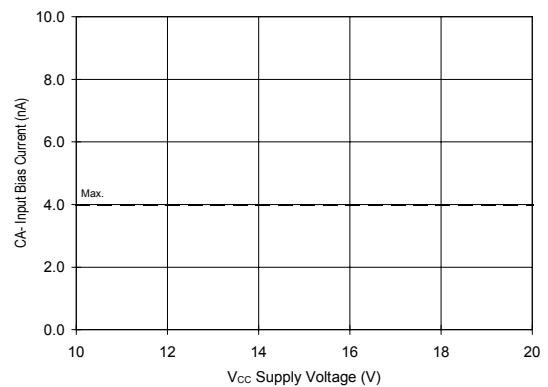


Figure 34B. CA- Input Current vs. Voltage

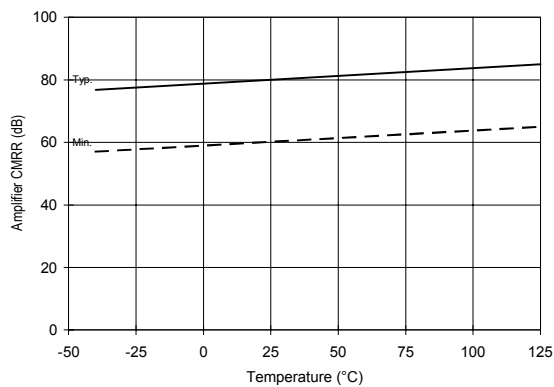


Figure 35A. Amplifier CMRR vs. Temperature

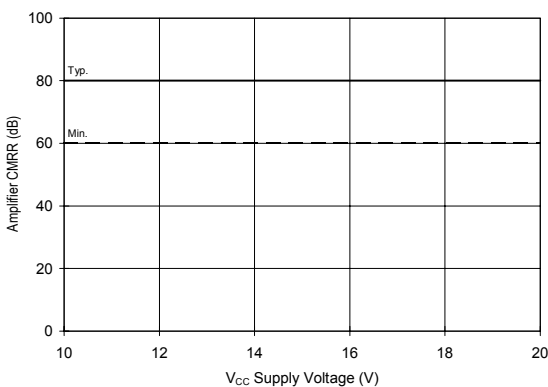


Figure 35B. Amplifier CMRR vs. Voltage

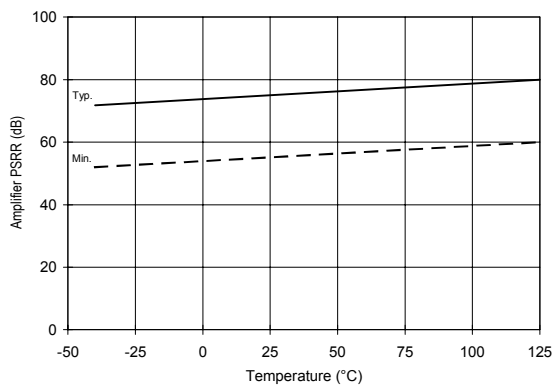


Figure 36A. Amplifier PSRR vs. Temperature

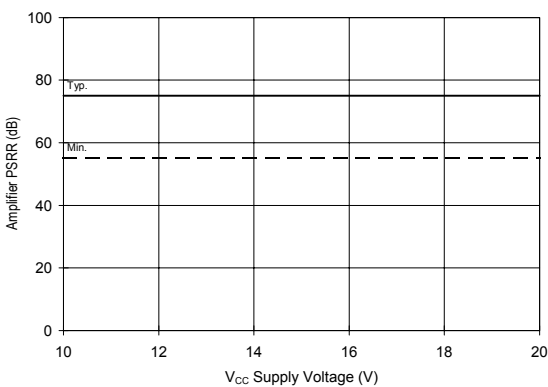


Figure 36B. Amplifier PSRR vs. Voltage

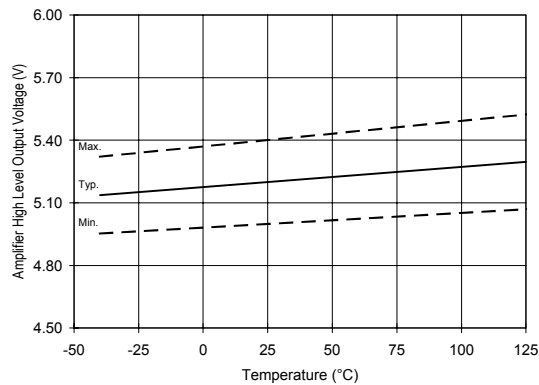


Figure 37A. Amplifier High Level Output vs. Temperature

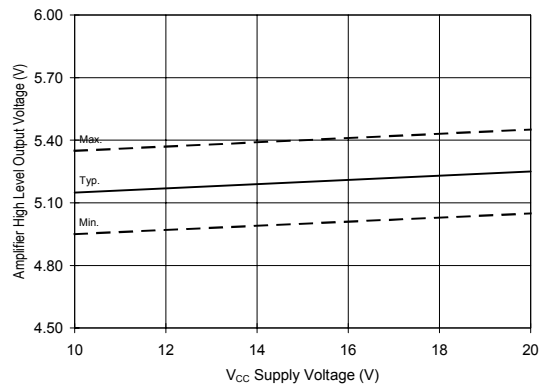


Figure 37B. Amplifier High Level Output vs. Voltage

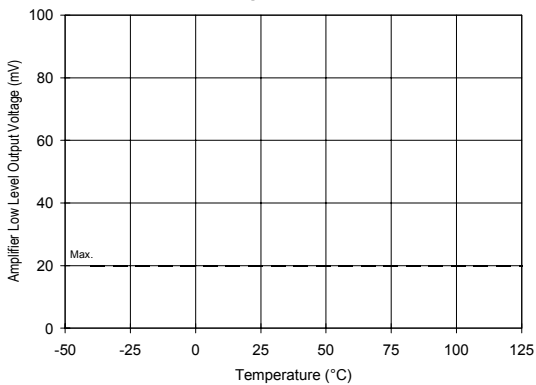


Figure 38A. Amplifier Low Level Output vs. Temperature

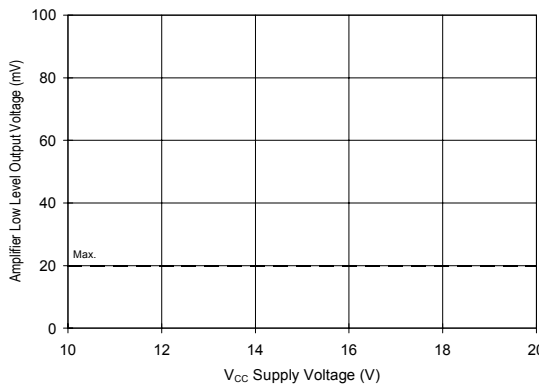


Figure 38B. Amplifier Low Level Output vs. Voltage

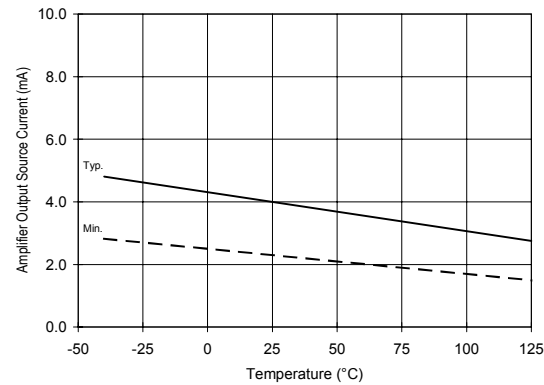


Figure 39A. Amplifier Output Source Current vs. Temperature

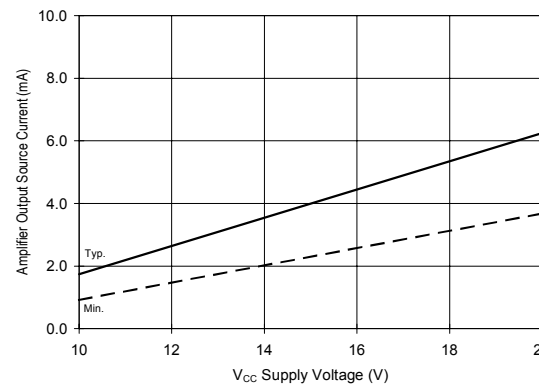


Figure 39B. Amplifier Output Source Current vs. Voltage

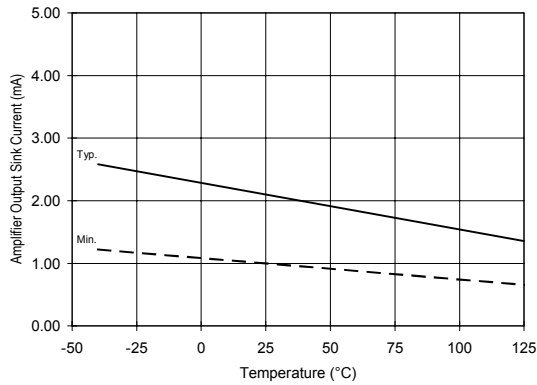


Figure 40A. Amplifier Output Sink Current vs. Temperature

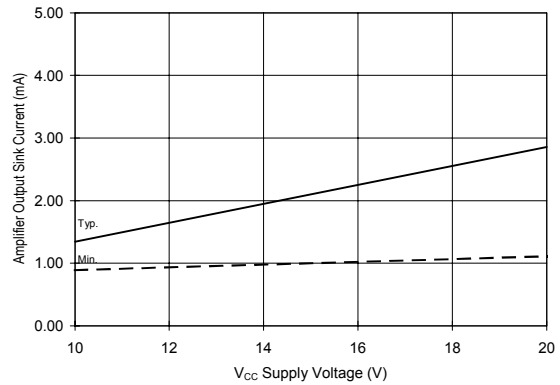


Figure 40B. Amplifier Output Sink Current vs. Voltage

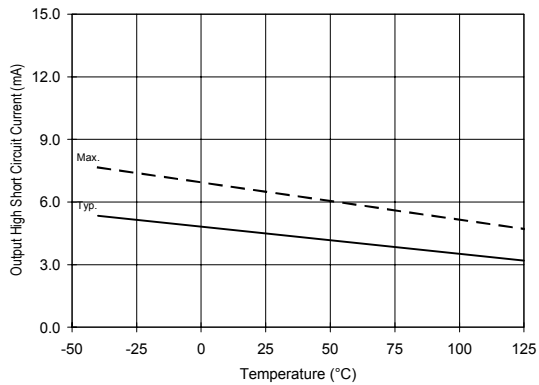


Figure 41A. Amplifier Output High Short Circuit Current vs. Temperature

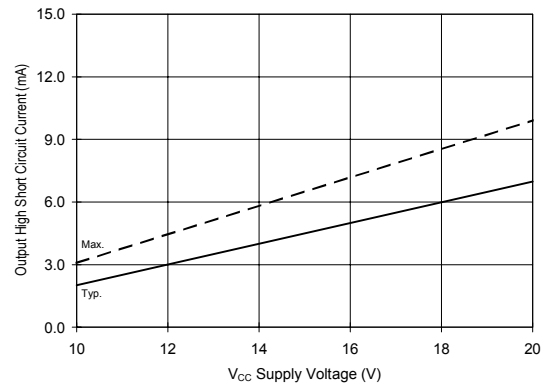


Figure 41B. Amplifier Output High Short Circuit Current vs. Voltage

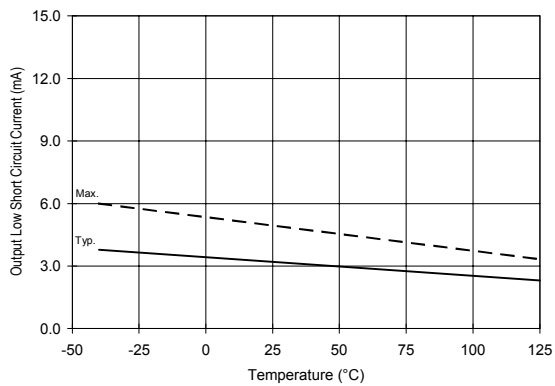


Figure 42A. Amplifier Output Low Short Circuit Current vs. Temperature

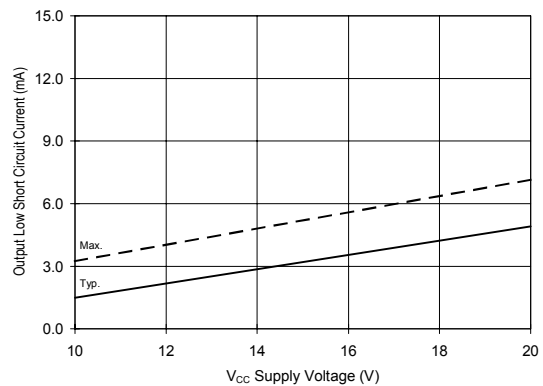


Figure 42B. Amplifier Output Low Short Circuit Current vs. Voltage

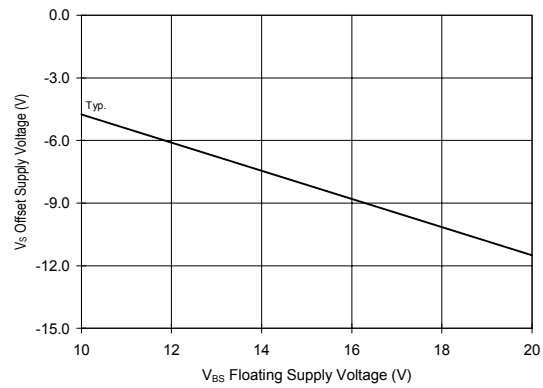


Figure 4-3. Maximum VS Negative Offset vs. V_{BS} Supply Voltage