1.5A Ultra-LDO with Programmable Soft-Start

Check for Samples: TPS742xx

FEATURES

- **Soft-Start (SS) Pin Provides a Linear Startup with Ramp Time Set by External Capacitor**
- **1% Accuracy Over Line, Load, and Temperature**
- **Supports Input Voltages as Low as 0.9V with External Bias Supply**
- **Adjustable Output (0.8V to 3.6V)**
- **Fixed Output (0.9V to 3.6V)**
- **Ultra-Low Dropout: 55mV at 1.5A (typ)**
- **Stable with Any or No Output Capacitor**
- **Excellent Transient Response**
- **Available in 5mm × 5mm × 1mm QFN and DDPAK-7 Packages**
- **Open-Drain Power-Good (5 × 5 QFN)**
- **Active High Enable**

APPLICATIONS

- **FPGA Applications**
- **DSP Core and I/O Voltages**
- **Post-Regulation Applications**
- **Applications with Special Start-Up Time or Sequencing Requirements**
- **Hot-Swap and Inrush Controls**

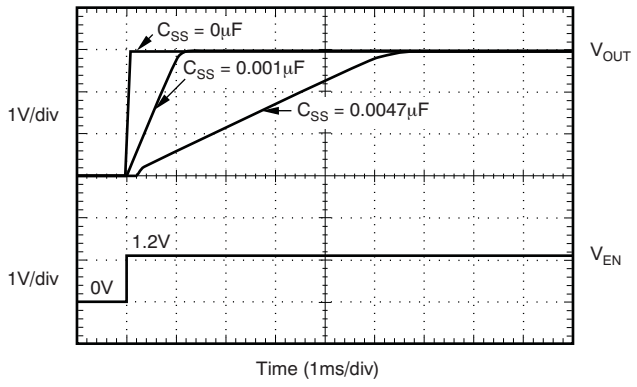


Figure 1. Turn-On Response

DESCRIPTION

The TPS742xx low-dropout (LDO) linear regulators provide an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that will meet the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. Each LDO is stable with low-cost ceramic output capacitors and the family is fully specified from –40°C to +125°C. The TPS742xx is offered in a small (5mm × 5mm) QFN package, yielding a highly compact total solution size. For applications that require additional power dissipation, the DDPAK (KTW) package is also available.

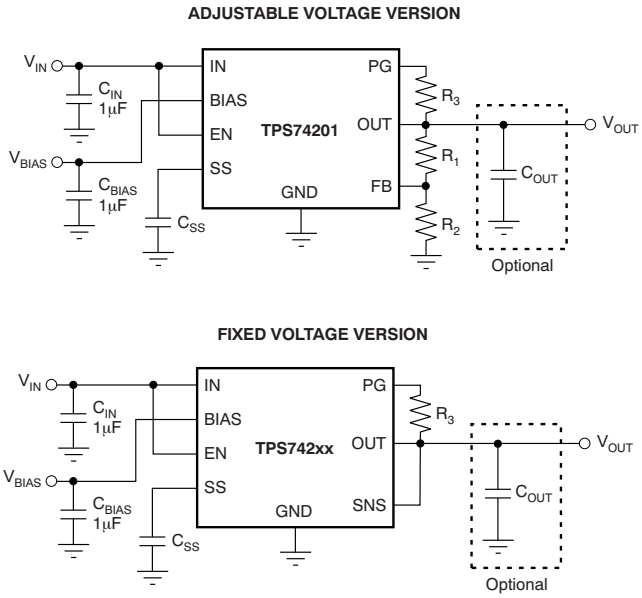


Figure 2. Typical Application Circuits

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS742**xx yyy z**	**XX** is nominal output voltage (for example, 12 = 1.2V, 15 = 1.5V, 01 = Adjustable).(3) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 0.9V to 1.5V in 50mV increments and 1.5V to 3.3V in 100mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 0.8V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

		TPS742xx	UNIT
V_{IN}, V_{BIAS}	Input voltage range	–0.3 to +6	V
V_{EN}	Enable voltage range	–0.3 to +6	V
V_{PG}	Power-good voltage range	–0.3 to +6	V
I_{PG}	PG sink current	0 to +1.5	mA
V_{SS}	SS pin voltage range	–0.3 to +6	V
V_{FB}	Feedback pin voltage range	–0.3 to +6	V
V_{OUT}	Output voltage range	–0.3 to V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited	
	Output short circuit duration	Indefinite	
P_{DISS}	Continuous total power dissipation	See *Thermal Information* Table	
T_J	Operating junction temperature range	–40 to +125	°C
T_{STG}	Storage junction temperature range	–55 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1][2]		TPS742xx[3]		UNITS
		RGW (20 PINS)	KTW (7 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance[4]	30.5	20.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[5]	27.6	2.1	
θ_{JB}	Junction-to-board thermal resistance[6]	N/A	N/A	
ψ_{JT}	Junction-to-top characterization parameter[7]	0.37	4.2	
ψ_{JB}	Junction-to-board characterization parameter[8]	10.6	6.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[9]	4.1	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW and KTW packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. RGW: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array.
  ii. KTW: The exposed pad is connected to the PCB ground layer through a 6x6 thermal via array.
  (b) Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, refer to the *Power Dissipation* and *Estimating Junction Temperature* sections.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

At V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, C_{IN} = C_{BIAS} = 0.1µF, C_{OUT} = 10µF, I_{OUT} = 50mA, V_{BIAS} = 5.0V, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	TPS742xx			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.375		5.25	V
V_{REF}	Internal reference (Adj.)	T_J = +25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5V, I_{OUT} = 1.5A, V_{BIAS} = 5V	V_{REF}		3.6	V
	Accuracy(1)	2.375V ≤ V_{BIAS} ≤ 5.25V, V_{OUT} + 1.62V ≤ V_{BIAS} 50mA ≤ I_{OUT} ≤ 1.5A	–1	±0.2	1	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5V, QFN		0.0005	0.05	%/V
		$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5V, DDPAK		0.0005	0.06	
V_{OUT}/I_{OUT}	Load regulation	0mA ≤ I_{OUT} ≤ 50mA		0.013		%/mA
		50mA ≤ I_{OUT} ≤ 1.5A		0.04		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 1.5A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62V, QFN		55	100	mV
		I_{OUT} = 1.5A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62V, DDPAK		60	120	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5A, V_{IN} = V_{BIAS}			1.4	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$	1.8		4	A
I_{BIAS}	Bias pin current	I_{OUT} = 0mA to 1.5A		2	4	mA
I_{SHDN}	Shutdown supply current (V_{IN})	V_{EN} ≤ 0.4V		1	100	µA
I_{FB}, I_{SNS}	Feedback, Sense pin current(3)	I_{OUT} = 50mA to 1.5A	–250	68	250	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		73		dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		42		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		62		dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		50		
Noise	Output noise voltage	100Hz to 100kHz, I_{OUT} = 1.5A, C_{SS} = 0.001µF		16 × V_{OUT}		μV_{RMS}
V_{TRAN}	$\%V_{OUT}$ droop during load transient	I_{OUT} = 50mA to 1.5A at 1A/µs, C_{OUT} = none		3.5		$\%V_{OUT}$
t_{STR}	Minimum startup time	I_{OUT} = 1.5A, C_{SS} = open		100		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4V	0.5	0.73	1	µA
$V_{EN,\ HI}$	Enable input high level		1.1		5.5	V
$V_{EN,\ LO}$	Enable input low level		0		0.4	V
$V_{EN,\ HYS}$	Enable pin hysteresis			50		mV
$V_{EN,\ DG}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG,\ LO}$	PG output low voltage	I_{PG} = 1mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = 5.25V, V_{OUT} > V_{IT}		0.03	1	µA
T_J	Operating junction temperature		–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+155		°C
		Reset, temperature decreasing		+140		

(1) Adjustable devices tested at 0.8V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
(3) I_{FB}, I_{SNS} current flow is out of the device.

BLOCK DIAGRAMS

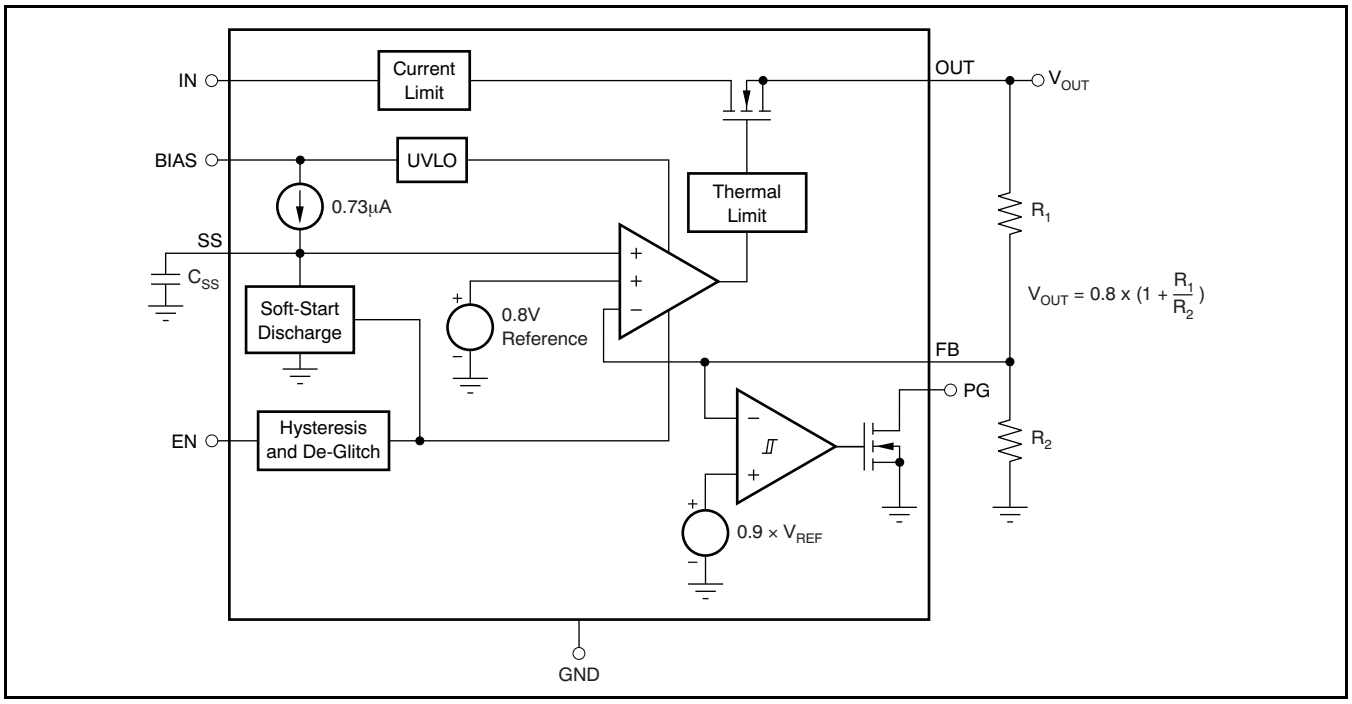


Figure 3. Adjustable Voltage Version

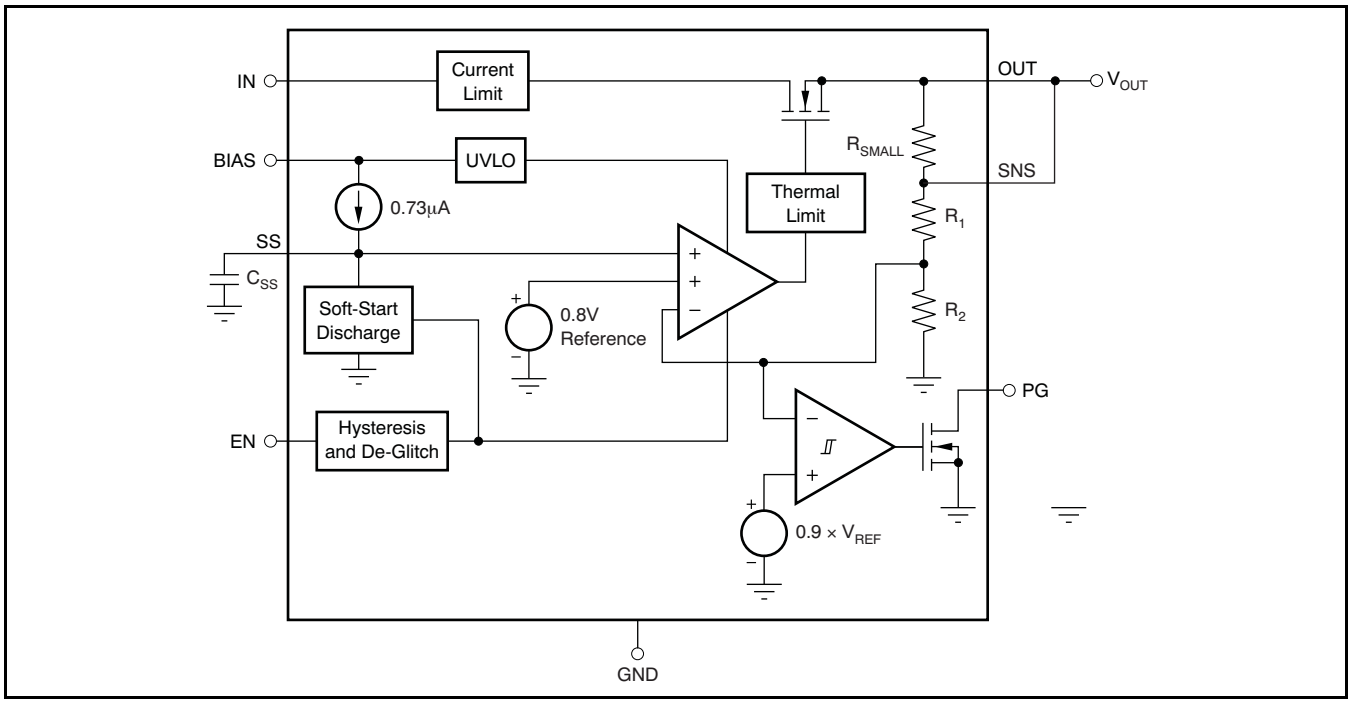


Figure 4. Fixed Voltage Versions

Table 1. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R1/R2)$

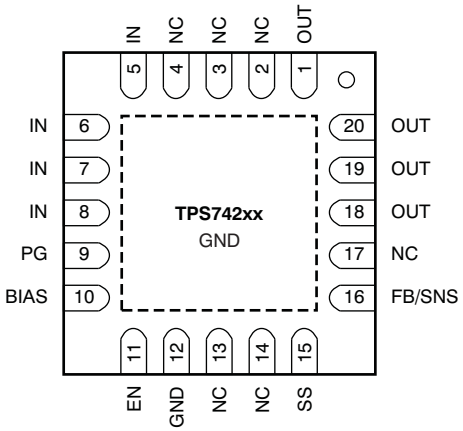
Table 2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1ms
470pF	0.5ms
1000pF	1ms
4700pF	5ms
0.01μF	10ms
0.015μF	16ms

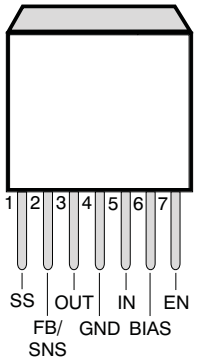
(1) $$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.73\mu A}$$ where $t_{SS}(s)$ = soft-start time in seconds.

PIN CONFIGURATIONS

RGW PACKAGE
5 × 5 QFN-20
(TOP VIEW)



KTW PACKAGE
DDPAK-7
SURFACE-MOUNT



PIN DESCRIPTIONS

NAME	KTW (DDPAK)	RGW (QFN)	DESCRIPTION
IN	5	5–8	Unregulated input to the device.
EN	7	11	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
SS	1	15	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100μs.
BIAS	6	10	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	N/A	9	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10kΩ to 1MΩ should be connected from this pin to a supply up to 5.5V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
FB	2	16	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating. (Adjustable version only.)
SNS			This pin is the sense connection to the load device. This pin must be connected to V_{OUT} and must not be left floating. (Fixed versions only.)
OUT	3	1, 18–20	Regulated output voltage. No capacitor is required on this pin for stability.
NC	N/A	2–4, 13, 14, 17	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	4	12	Ground
PAD/TAB			Should be soldered to the ground plane for increased thermal performance.

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF, unless otherwise noted.

LOAD REGULATION

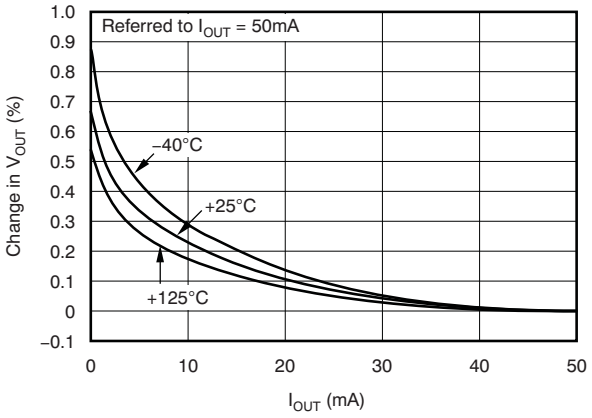


Figure 5.

LOAD REGULATION

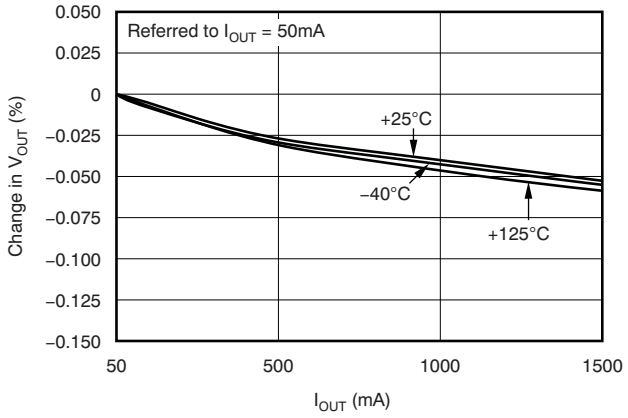


Figure 6.

LINE REGULATION

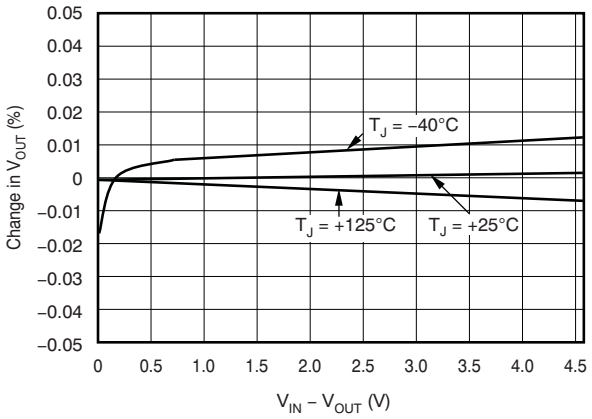


Figure 7.

V_{IN} DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE (T_J)

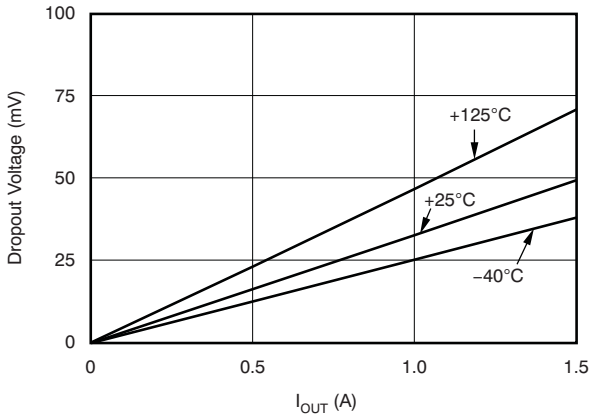


Figure 8.

V_{IN} DROPOUT VOLTAGE vs V_{BIAS} − V_{OUT} AND TEMPERATURE (T_J)

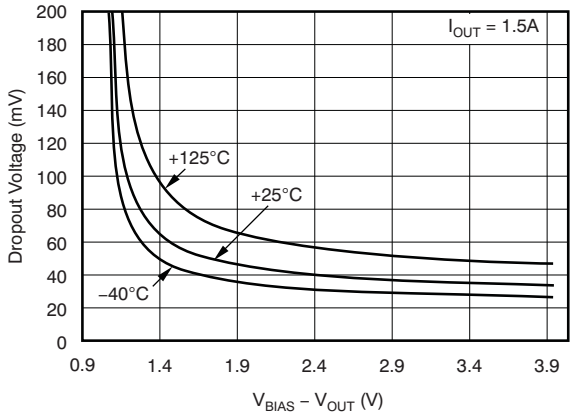


Figure 9.

V_{IN} DROPOUT VOLTAGE vs V_{BIAS} − V_{OUT} AND TEMPERATURE (T_J)

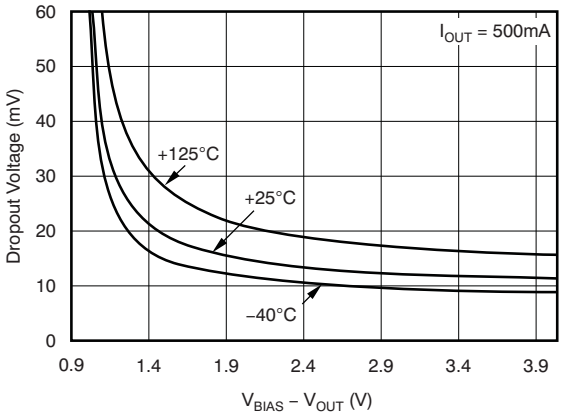


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF, unless otherwise noted.

V_{BIAS} DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE

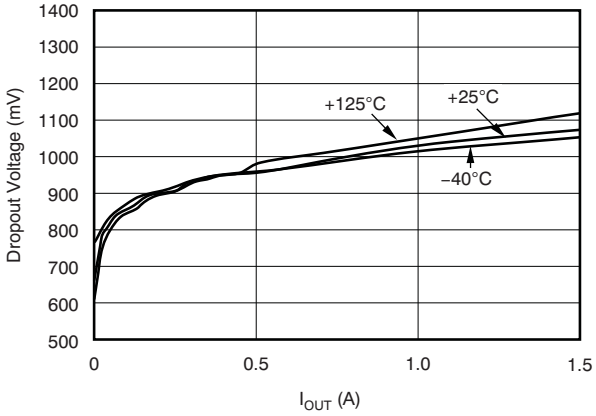


Figure 11.

V_{BIAS} PSRR vs FREQUENCY

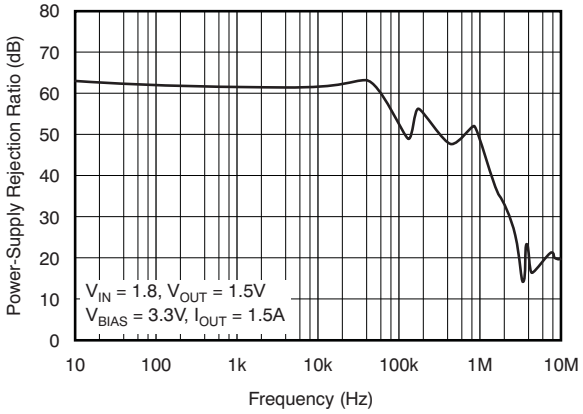


Figure 12.

V_{IN} PSRR vs FREQUENCY

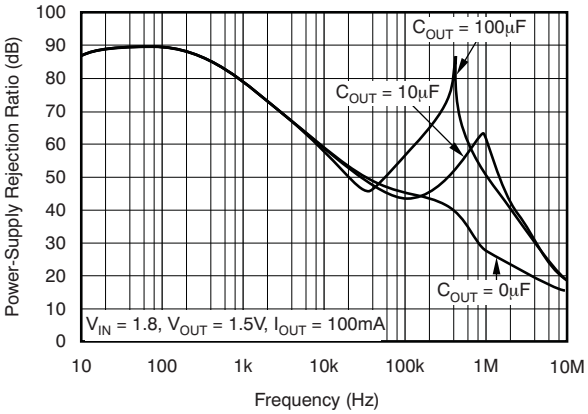


Figure 13.

V_{IN} PSRR vs FREQUENCY

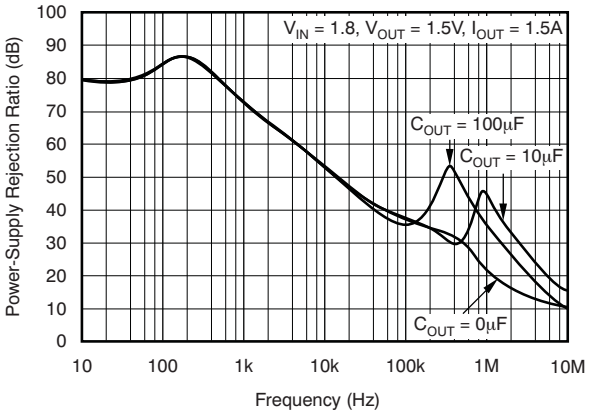


Figure 14.

V_{IN} PSRR vs V_{IN} – V_{OUT}

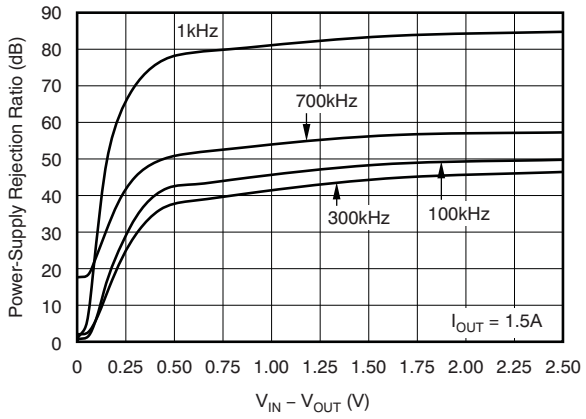


Figure 15.

NOISE SPECTRAL DENSITY

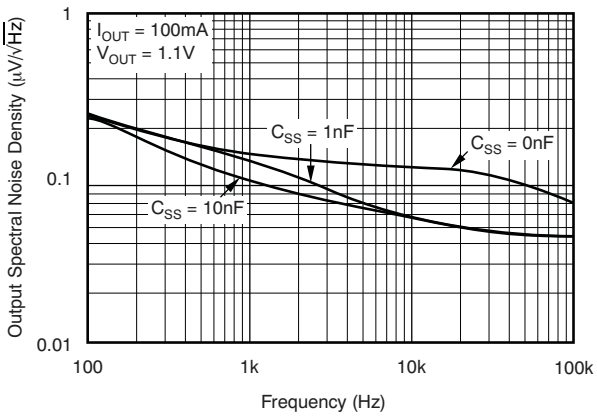


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF, unless otherwise noted.

I_{BIAS} vs I_{OUT} AND TEMPERATURE

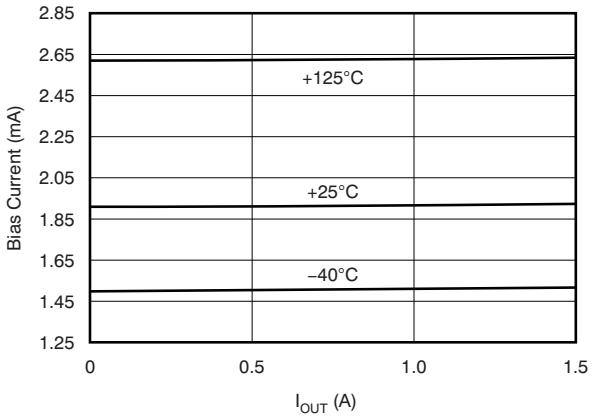


Figure 17.

I_{BIAS} vs V_{BIAS} AND V_{OUT}

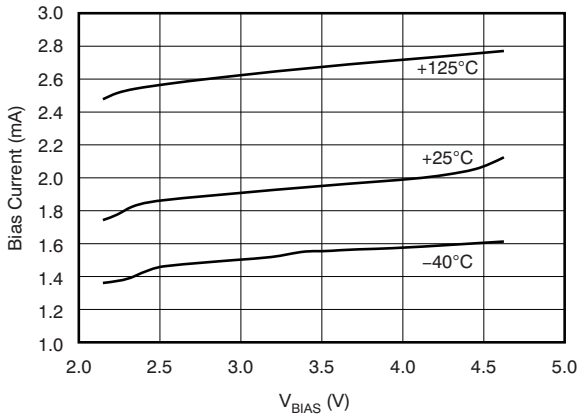


Figure 18.

I_{BIAS} SHUTDOWN vs TEMPERATURE

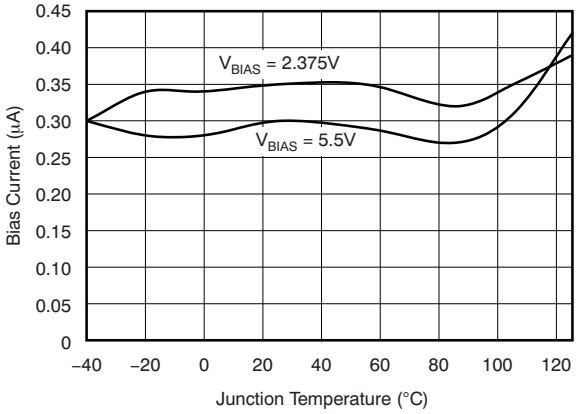


Figure 19.

SOFT-START CHARGING CURRENT (I_{SS}) vs TEMPERATURE

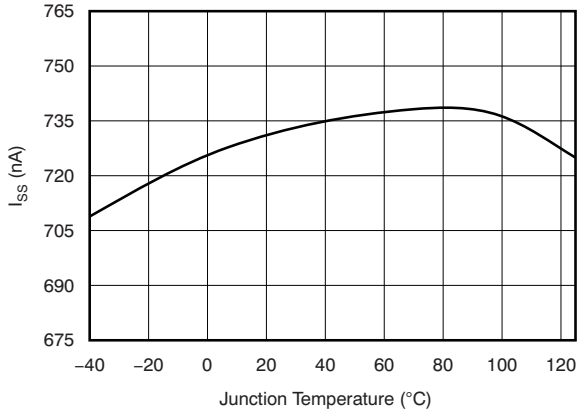


Figure 20.

LOW-LEVEL PG VOLTAGE vs PG CURRENT

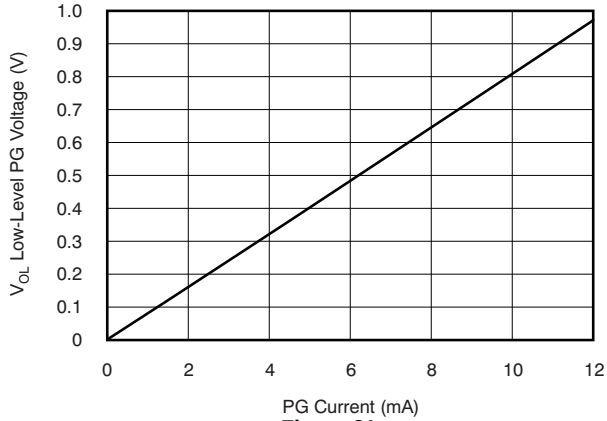


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{BIAS} = 3.3V, I_{OUT} = 50mA, EN = V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF, and C_{OUT} = 10µF, unless otherwise noted.

V_{BIAS} LINE TRANSIENT (1.5A)

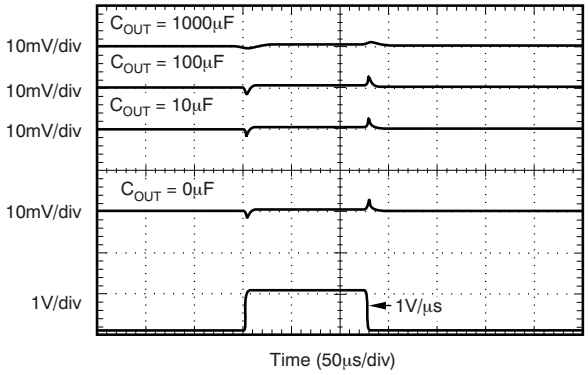


Figure 22.

V_{IN} LINE TRANSIENT

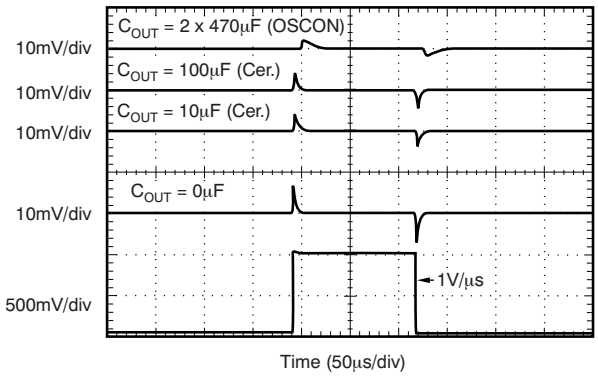


Figure 23.

OUTPUT LOAD TRANSIENT RESPONSE

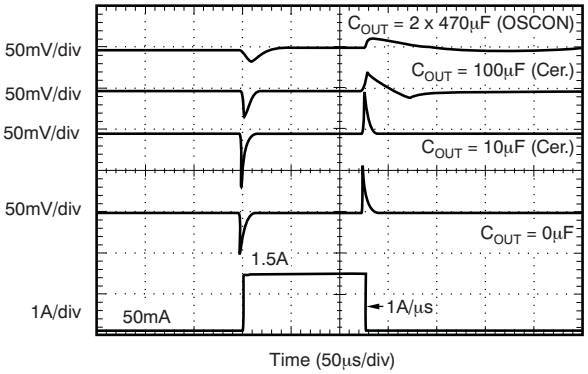


Figure 24.

TURN-ON RESPONSE

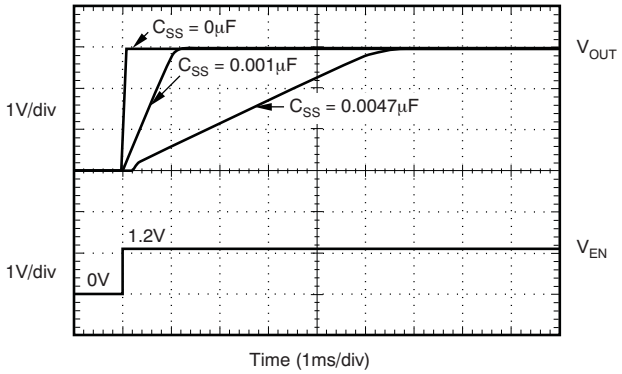


Figure 25.

POWER-UP/POWER-DOWN

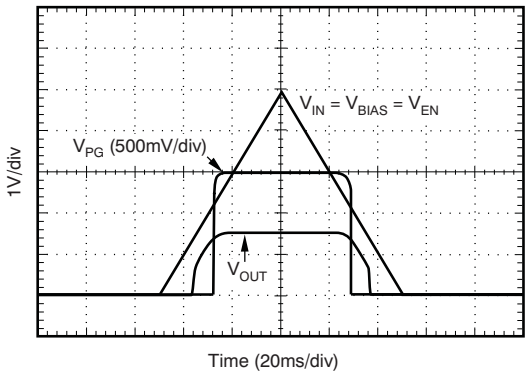


Figure 26.

OUTPUT SHORT-CIRCUIT RECOVERY

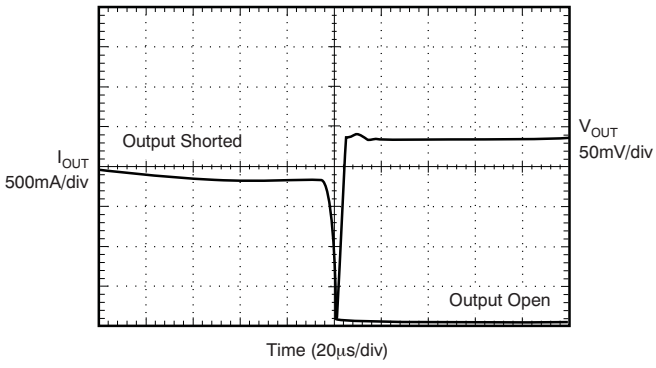


Figure 27.

APPLICATION INFORMATION

The TPS742xx belongs to a family of new generation ultra-low dropout regulators that feature soft-start and tracking capabilities. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS742xx to be stable with any or even no output capacitor. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS742xx features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

ADJUSTABLE VOLTAGE PART AND SETTING

Figure 28 is a typical application circuit for the TPS74201 adjustable output device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 28. Refer to Table 1 for sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 should be ≤ 4.99kΩ.

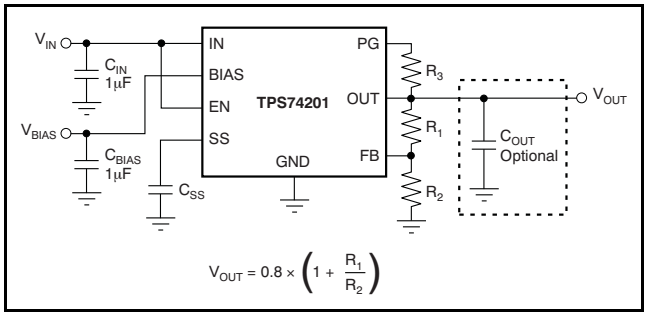


Figure 28. Typical Application Circuit for the TPS74201 (Adjustable Version)

FIXED VOLTAGE AND SENSE PIN

Figure 29 illustrates a typical application circuit for the TPS742xx fixed output device.

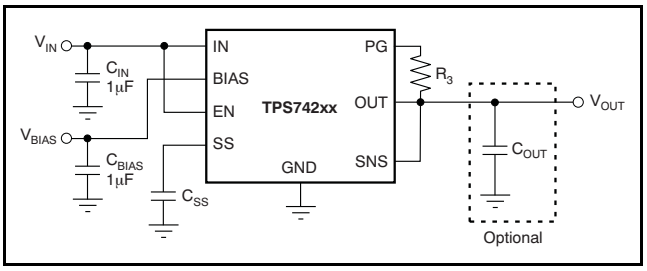


Figure 29. Typical Application Circuit for the TPS742xx (Fixed Voltage)

A fixed voltage version of the TPS742xx has a sense pin (SNS) so that the device can monitor its output voltage at the load device pin(s) as closely as possible. Unlike other TI fixed-voltage LDOs, however, this pin must ***not*** be left floating; it ***must*** be connected to an output node. See the TI application report, *Ultimate Regulation of with Fixed Output Versions of the TPS742xx, TPS743xx, and TPS744xx* (literature number SBVA024), available for download from the TI web site.

INPUT, OUTPUT, AND BIAS CAPACITOR REQUIREMENTS

The device does not require any output capacitor for stability. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins is strongly dependent on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7µF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

TRANSIENT RESPONSE

The TPS742xx was designed to have transient response within 5% for most applications without any output capacitor. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time. Refer to Figure 24 in the Typical Characteristics section. Since the TPS742xx is stable without an output capacitor, many applications may allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

DROPOUT VOLTAGE

The TPS742xx offers industry-leading dropout performance, making it well-suited for high-current low V_{IN}/low V_{OUT} applications. The extremely low dropout of the TPS742xx allows the device to be used in place of a DC/DC converter and still achieve good efficiencies. This efficiency allows the user to rethink the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS742xx. The first specification (illustrated in Figure 30) is referred to as *V_{IN} Dropout* and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62V above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3V rail with 5% tolerance and with V_{OUT} = 1.5V. If V_{BIAS} is higher than 3.3V × 0.95 or V_{OUT} is less than 1.5V, V_{IN} dropout is less than specified.

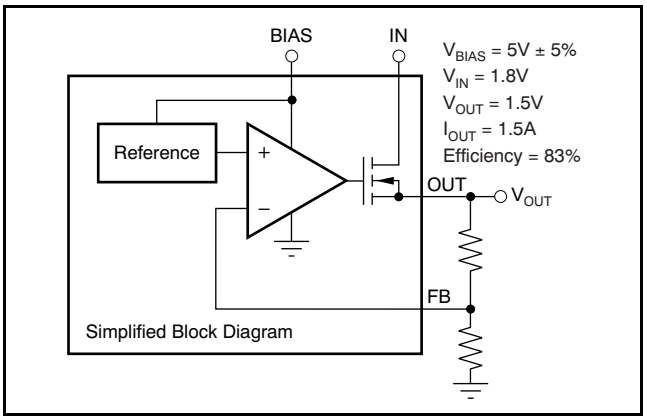


Figure 30. Typical Application of the TPS742xx Using an Auxiliary Bias Rail

The second specification (shown in Figure 31) is referred to as *V_{BIAS} Dropout* and is for users who wish to tie IN and BIAS together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.4V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

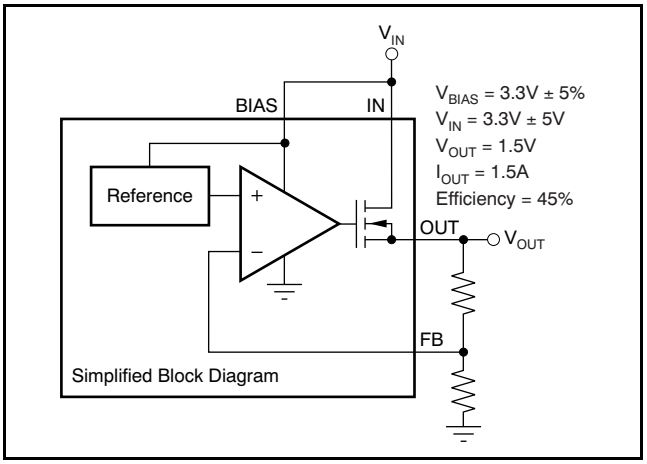


Figure 31. Typical Application of the TPS742xx Without an Auxiliary Bias

PROGRAMMABLE SOFT-START

The TPS742xx features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic soft-start, the TPS742xx error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (2)$$

$V_{OUT(NOM)}$ is the nominal set output voltage as set by the user, C_{OUT} is the output capacitance, and $I_{CL(MIN)}$ is the minimum current limit for the device. In applications where monotonic startup is required, the soft-start time given by Equation 1 should be set to be greater than Equation 2.

The maximum recommended soft-start capacitor is 0.015μF. Larger soft-start capacitors can be used and will not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 0.015μF could be a problem in applications where the user needs to rapidly pulse the enable pin and still requires the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Refer to Table 2 for suggested soft-start capacitor values.

SEQUENCING REQUIREMENTS

The device can have V_{IN}, V_{BIAS}, and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} and V_{BIAS} are present is preferred, and can be accomplished using a digital output from a processor or supply supervisor. An analog signal from an external RC circuit, as shown in Figure 32, can also be used as long as the delay time is long enough for V_{IN} and V_{BIAS} to be present.

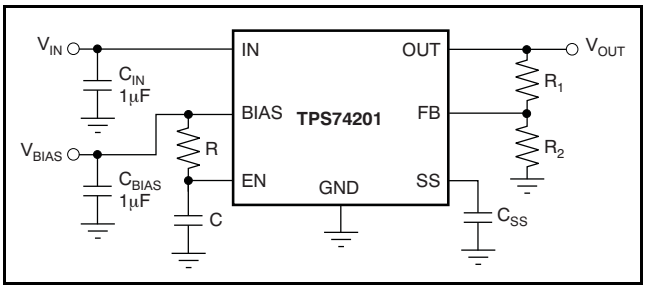


Figure 32. Soft-Start Delay Using an RC Circuit on Enable

If a signal is not available to enable the device after IN and BIAS, simply connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1V and the ramp rate of V_{IN} and V_{BIAS} is faster the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output will track the slower supply minus the dropout voltage until it reaches the set output voltage. If EN is connected to BIAS, the device will soft-start as programmed provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired then V_{OUT} will track V_{IN}.

NOTE: When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50μA of current from OUT. Although this condition will not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10kΩ.

OUTPUT NOISE

The TPS742xx provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001μF soft-start capacitor, the output noise is reduced by half and is typically $30\mu V_{RMS}$ for a 1.2V output (10Hz to 100kHz). Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001μF soft-start capacitor is given in Equation 3.

$$V_N(\mu V_{RMS}) = 25\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

The low output noise of the TPS742xx makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

ENABLE/SHUTDOWN

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4V turns the regulator off, while V_{EN} above 1.1V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow-ramping analog signals. This configuration allows the TPS742xx to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50mV of hysteresis and a deglitch circuit to help avoid on-off cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8V and varies with temperature and process variations. Temperature variation is approximately –1mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, a fast rise-time signal should be used to enable the TPS742xx.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

POWER-GOOD (QFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5V or lower rail through an external pull-up resistor. This pin requires at least 1.1V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1mA, so the pull-up resistor for PG should be in the range of 10kΩ to 1MΩ. PG is only provided on the QFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

INTERNAL CURRENT LIMIT

The TPS742xx features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1.8A and maintain regulation. The current limit responds in about 10μs to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Figure 27 in the Typical Characteristics section for a graph of I_{OUT} versus V_{OUT} performance.

The internal current limit protection circuitry of the TPS742xx is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS742xx above the rated current degrades device reliability.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS742xx is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS742xx into thermal shutdown degrades device reliability.

LAYOUT RECOMMENDATIONS AND POWER DISSIPATION

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 28 should be connected as close as possible to the load. If BIAS is connected to IN it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

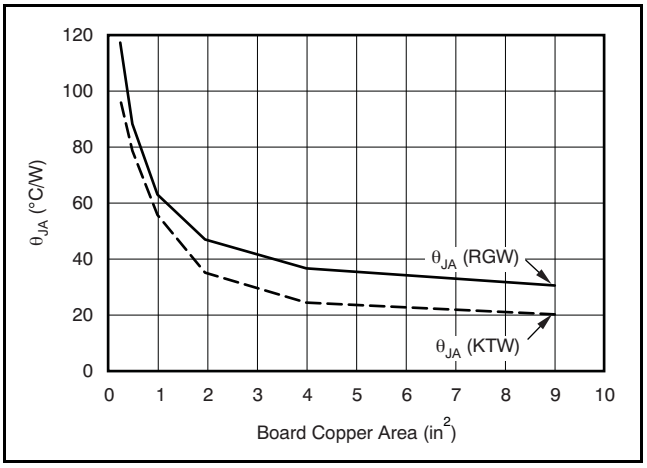
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the QFN (RGW) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device will not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 33.



Note: θ_{JA} value at board size of $9in^2$ (that is, 3in × 3in) is a JEDEC standard.

Figure 33. θ_{JA} vs Board Size

Figure 33 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

ESTIMATING JUNCTION TEMPERATURE

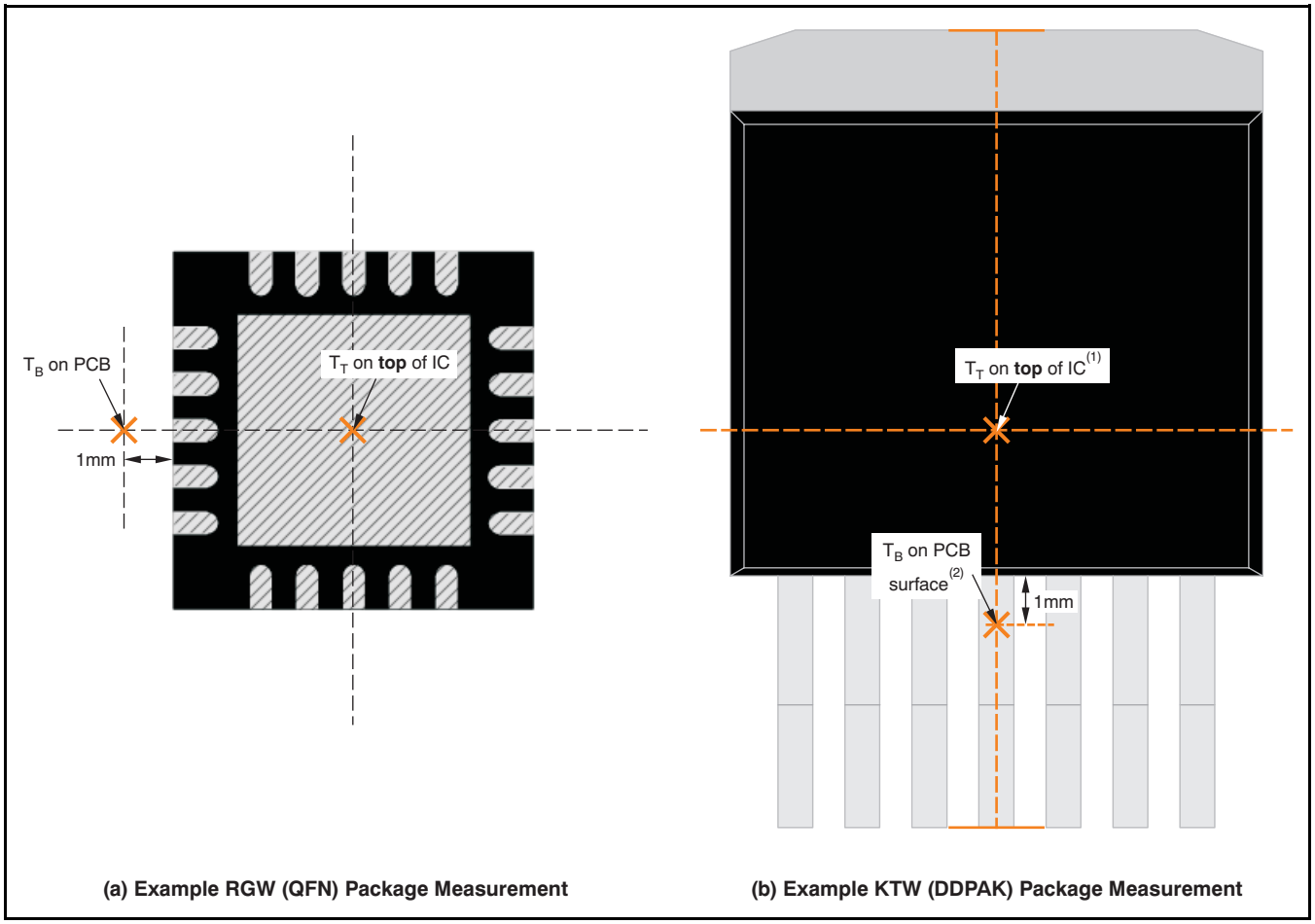
Using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

Where P_D is the power dissipation shown by Equation 4, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 34 shows).

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.



(a) Example RGW (QFN) Package Measurement

(b) Example KTW (DDPAK) Package Measurement

(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured ***below*** the package lead **on the PCB surface**.

Figure 34. Measuring Points for T_T and T_B

Compared with θ_{JA}, the new thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size, but they do have a small dependency. Figure 35 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Looking at Figure 35, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point-symmetric to an IC center. In the KTW package, for example (see Figure 34), silicon is not beneath the measuring point of T_T which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point-symmetry, device heat distribution on the PCB is not point-symmetric, either, so that Ψ_{JB} has a dependency.

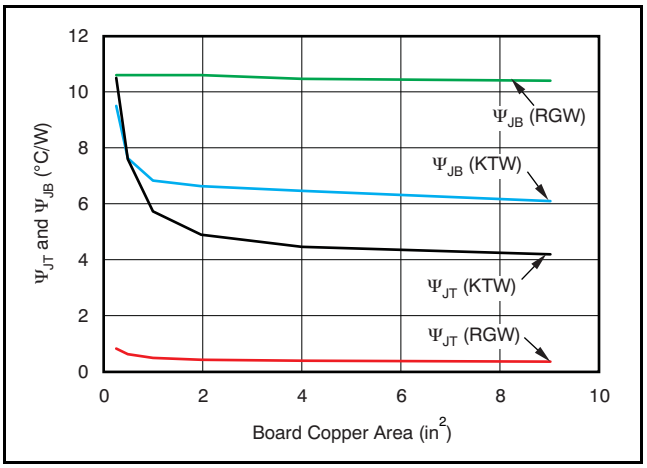


Figure 35. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using θ_{JC},Top to determine thermal characteristics, refer to the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com. Also, refer to the application note *IC Package Thermal Metrics* (SPRA953) (also available on the TI web site) for further information.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (August, 2010) to Revision L **Page**

- Corrected equation for Table 2 6

Changes from Revision J (December, 2009) to Revision K **Page**

- Replaced the *Dissipation Ratings* table with the *Thermal Information* table 3
- Revised *Layout Recommendations and Power Dissipation* section 16
- Changed final paragraph of *Power Dissipation* section 16
- Revised *Estimating Junction Temperature* section 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS74201KTWR	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	TPS74201	Samples
TPS74201KTWRG3	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	TPS74201	Samples
TPS74201KTWT	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	TPS74201	Samples
TPS74201KTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	TPS74201	Samples
TPS74201RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74201	Samples
TPS74201RGWRG4	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74201	Samples
TPS74201RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74201	Samples
TPS74201RGWTG4	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

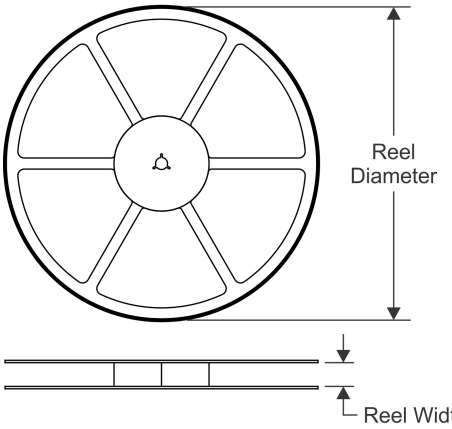
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

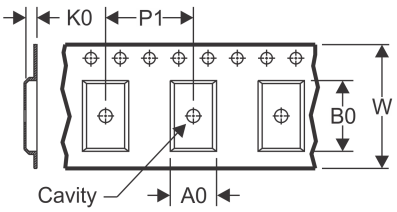
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

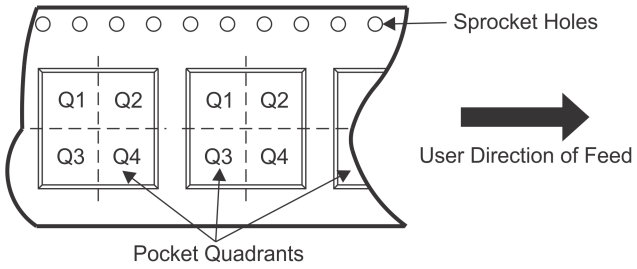


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

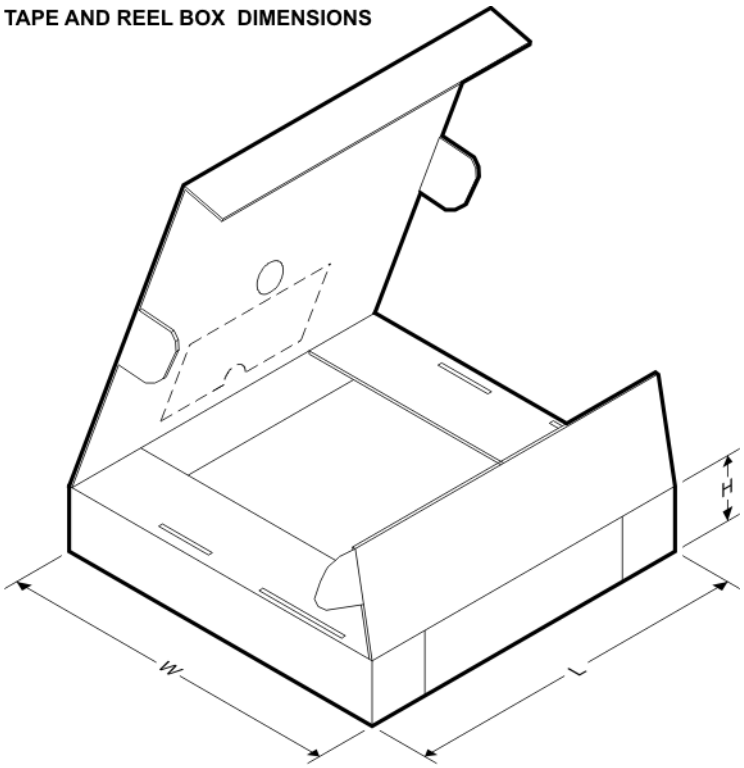
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74201KTWR	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74201KTWT	DDPAK/ TO-263	KTW	7	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74201RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74201RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

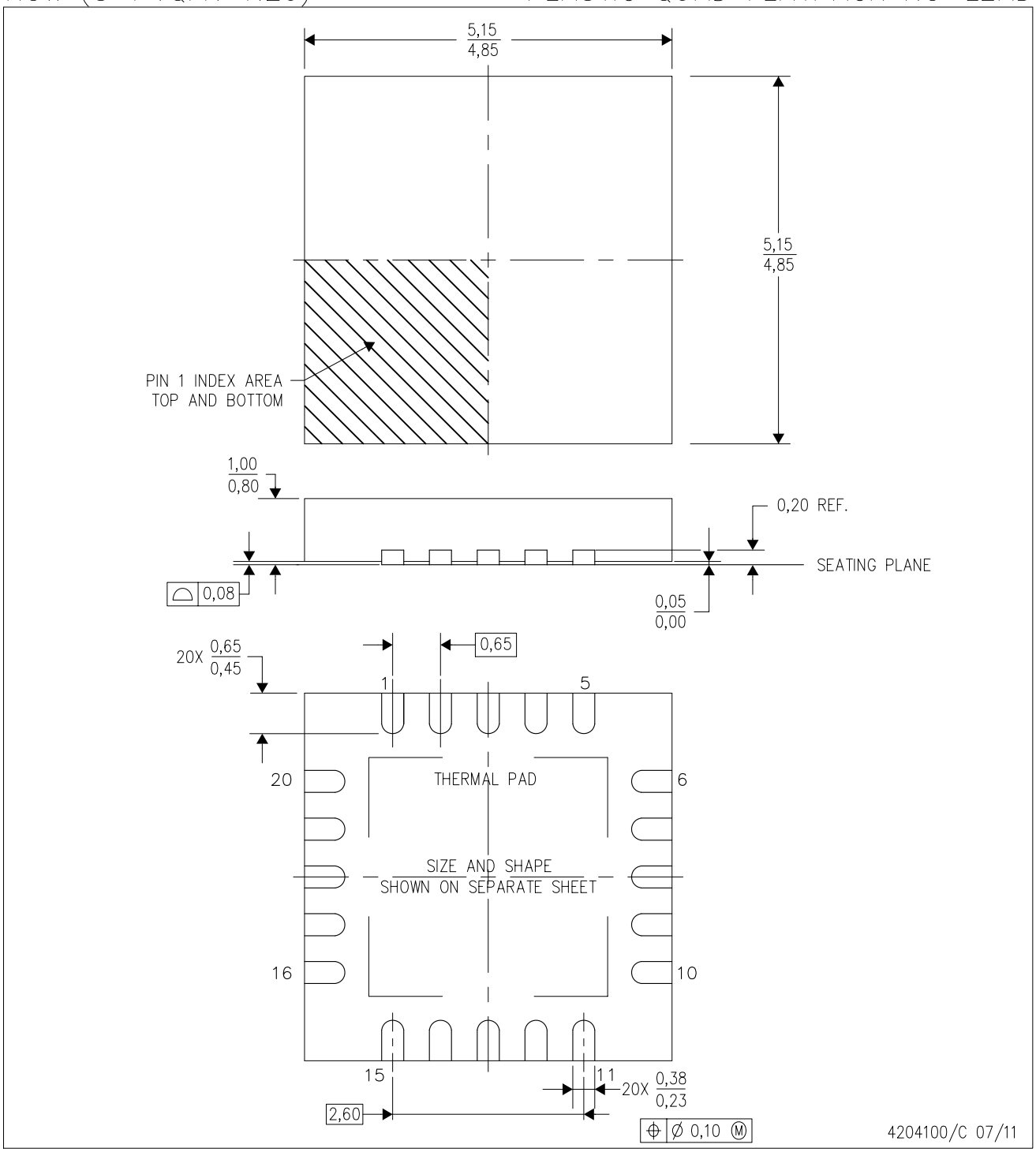
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74201KTWR	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0
TPS74201KTWT	DDPAK/TO-263	KTW	7	50	367.0	367.0	45.0
TPS74201RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74201RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

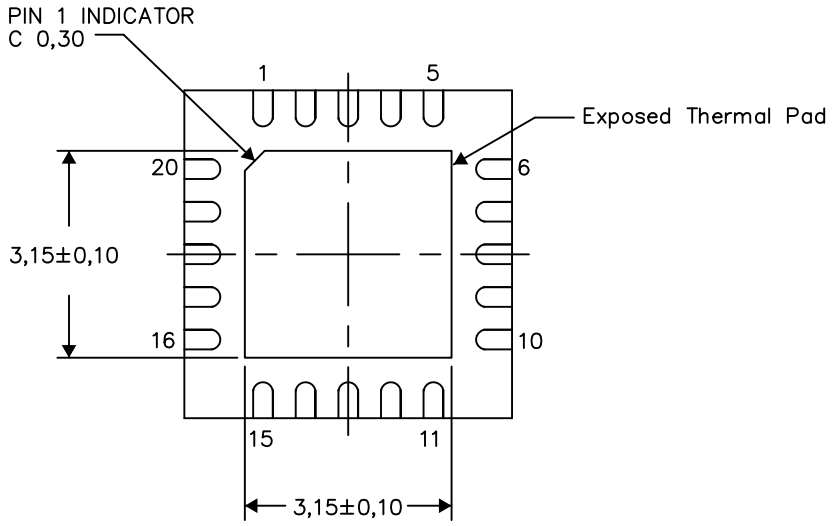
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



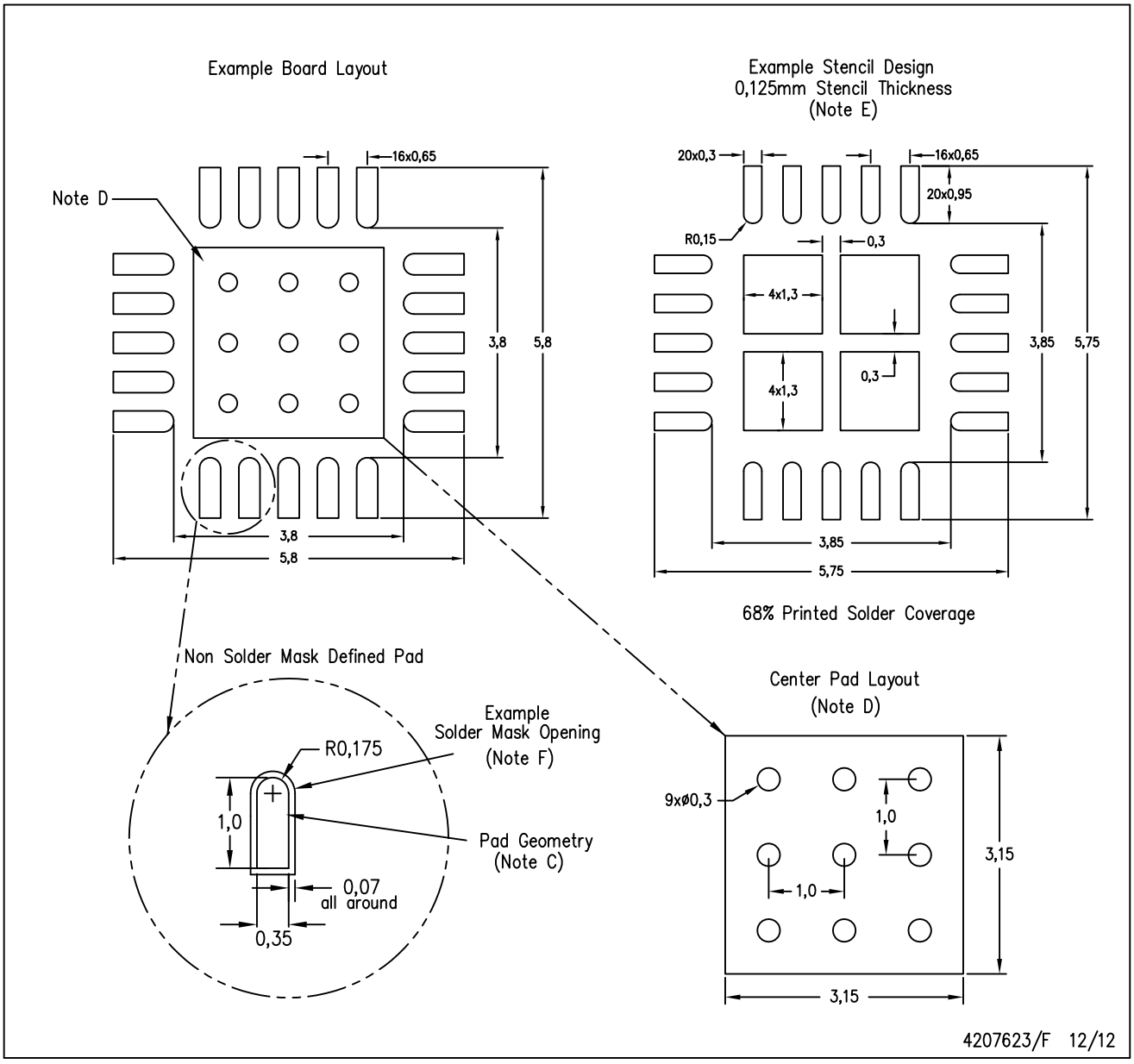
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/K 12/12

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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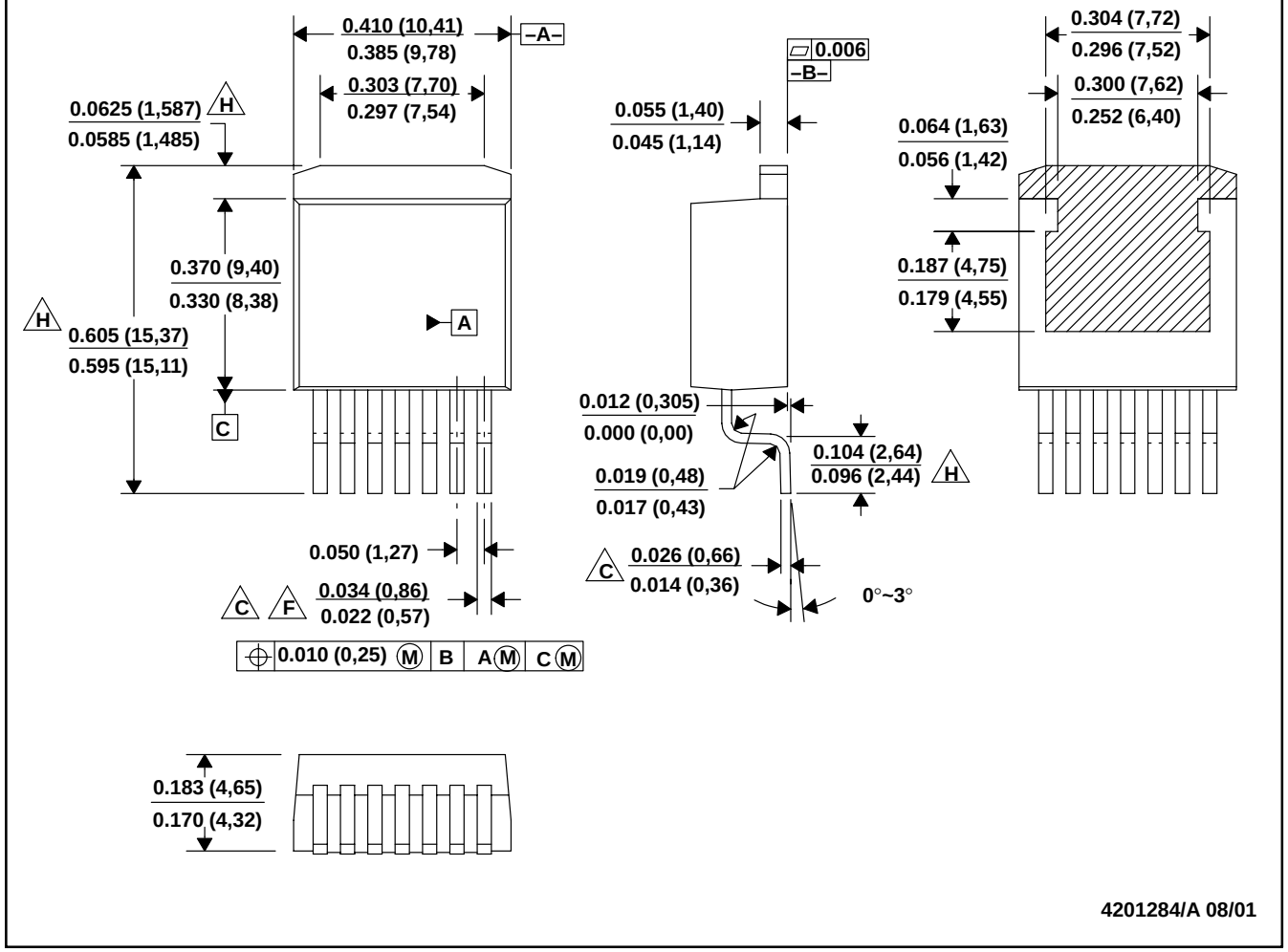
KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

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