FAIRCHILD SEMICONDUCTOR™

January 1997
Revised August 2004

NC7ST08
TinyLogic® HST 2-Input AND Gate

General Description

The NC7ST08 is a single 2-Input high performance CMOS AND Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NM OS/CMOS interfacing. Device performance is similar to MM74HCT but with 1/2 the output current drive of HC/HCT.

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed:
  t_{PD} 6 ns (typ), V_{CC} = 5V, C_L = 15 pF, T_A = 25°C
- Low Quiescent Power, I_{CC} < 1 µA, V_{CC} = 5.5V
- Balanced Output Drive; 2 mA I_{OL}, −2 mA I_{OH}
- TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7ST08M5X	MA05B	8S08	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7ST08P5X	MAA05A	T08	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7ST08L6X	MAC06A	NN	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Logic Symbol

IEEE/IEC

Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

Function Table

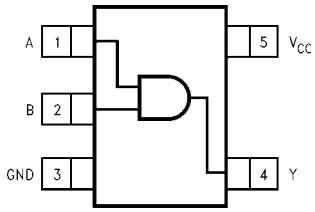
Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level L = LOW Logic Level

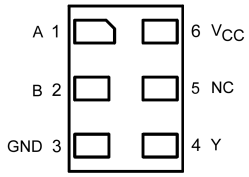
Connection Diagrams

Pin Assignments for SC70 and SOT23



(Top View)

Pad Assignment for MicroPak



(Top Thru View)

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@V_{IN} < −0.5V	−20 mA
@V_{IN} ≥ V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_{IN})	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_{OUT} < −0.5V	−20 mA
V_{OUT} > V_{CC} + 0.5V	+20 mA
Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_{OUT})	±12.5 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	±25 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (T_L); (Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @+85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage	4.5V to 5.5V
Input Voltage (V_{IN})	0.0V to V_{CC}
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 5.0V	0 ns to 500 ns
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

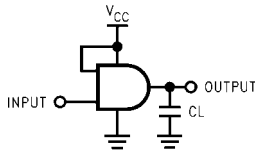
Symbol	Parameter	V_{CC}	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions
		(V)	Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	4.5–5.5	2.0			2.0		V	
V_{IL}	LOW Level Input Voltage	4.5–5.5			0.8		0.8	V	
V_{OH}	HIGH Level Output Voltage	4.5	4.4	4.5		4.4			I_{OH} = −20 μA
		4.5	4.18	4.35		4.13		V	I_{OH} = −2 mA
									V_{IN} = V_{IH}
V_{OL}	LOW Level Output Voltage	4.5		0	0.1		0.1		I_{OL} = 20 μA
		4.5		0.10	0.26		0.33	V	I_{OL} = 2 mA
									V_{IN} = V_{IL}
I_{IN}	Input Leakage Current	5.5			±0.1		±1.0	μA	0 ≤ V_{IN} ≤ 5.5V
I_{CC}	Quiescent Supply Current	5.5			1.0		10.0	μA	V_{IN} = V_{CC} or GND
I_{CCT}	I_{CC} per Input	5.5			2.0		2.9	mA	One Input V_{IN} = 0.5V or 2.4V, Other Input V_{CC} or GND

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay	5.0		4	12			ns	$C_L = 15$ pF	Figures 1, 3
				6	17					
		4.5		6	16		20	ns	$C_L = 50$ pF	
				12	27		31			
		5.5		5	14		18			
				11	26		30			
t_{TLH}, t_{THL}	Output Transition Time	5.0		4	10			ns	$C_L = 15$ pF	Figures 1, 3
		4.5		11	25		31	ns	$C_L = 50$ pF	
		5.5		10	21		26			
C_{IN}	Input Capacitance	Open			10			pF		
C_{PD}	Power Dissipation Capacitance	5.0		6				pF	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}\text{static})$.

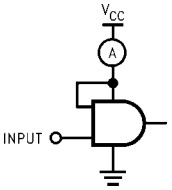
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; PRR = variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

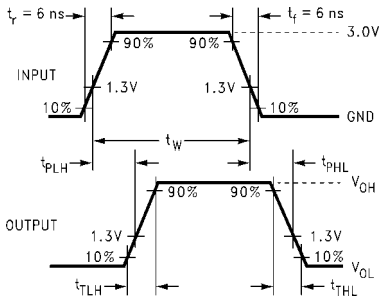


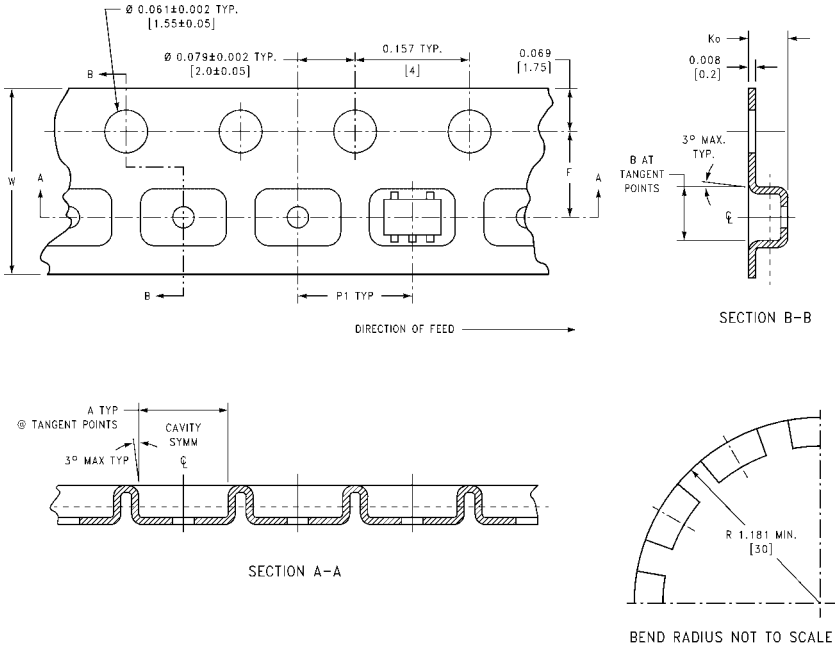
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SC70 and SOT23

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

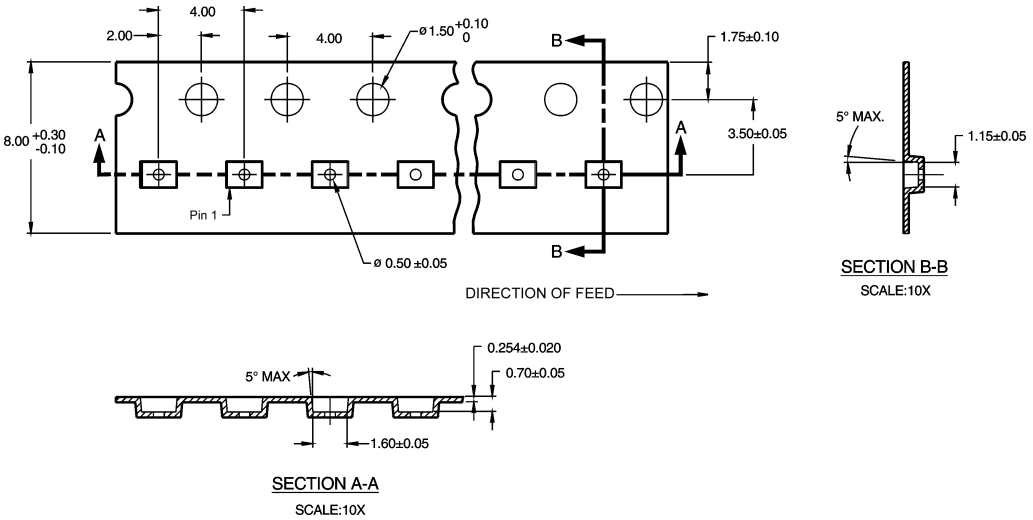


Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

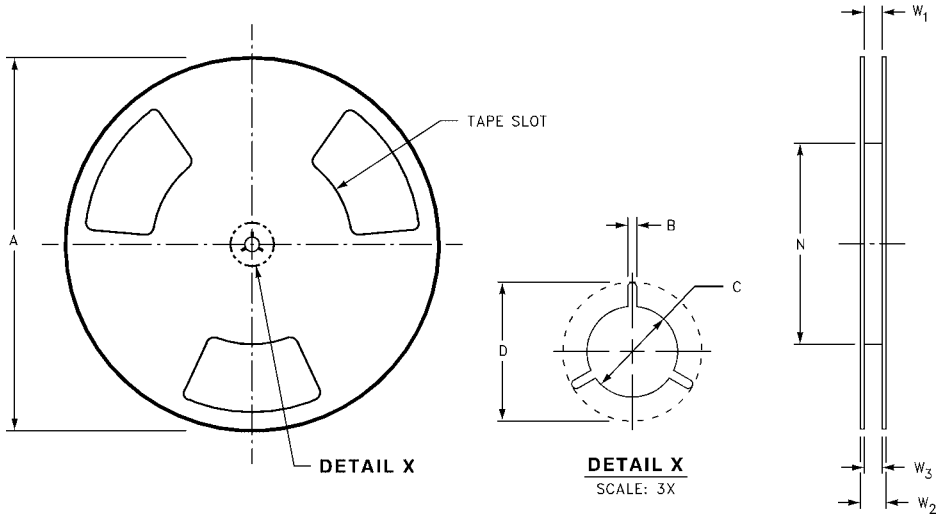
Tape and Reel Specification (Continued)

TAPE FORMAT for MircoPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

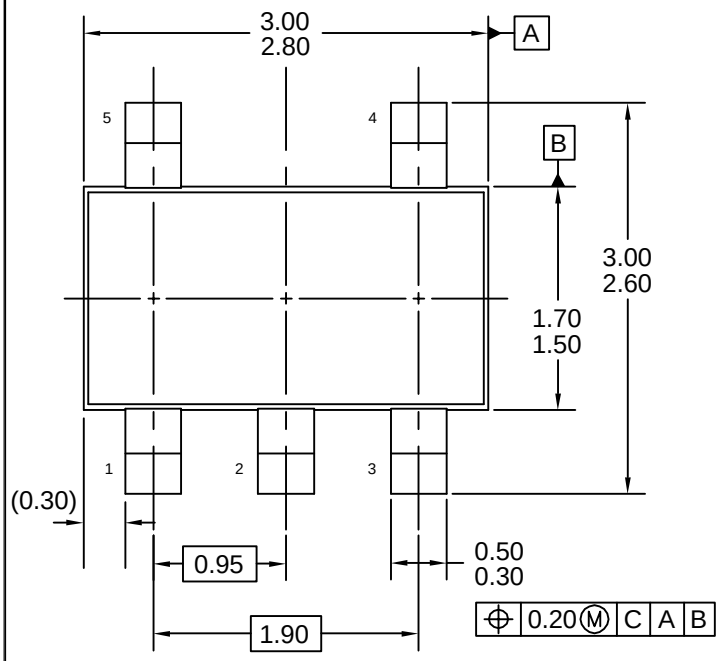


REEL DIMENSIONS inches (millimeters)

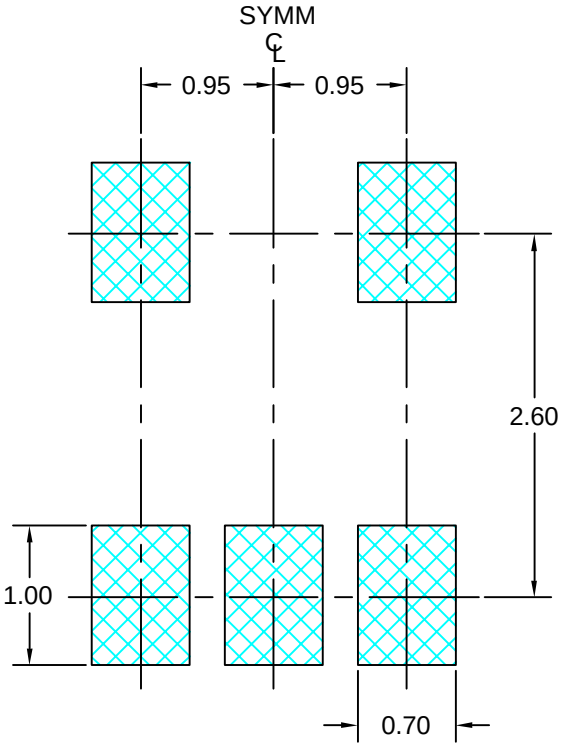


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

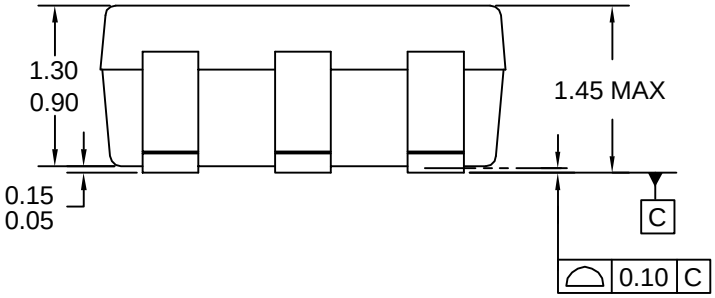
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11208	12/07/95	TL
B	REDRAW PER CURRENT STANDARD	11531	07/31/96	LUA
C	REDRAW AS PER JEDEC NEW ISSUE FROM A TO B. CHANGE DRAWING TEMPLATE FROM LANDSCAPE TO PORTRAIT. CHANGE DIMENSION UNIT FROM INCHES TO MILLIMETERS.			
4	CHANGED BOTTOM VIEW TO TOP VIEW, REMOVED DATE FROM NOTES, ADDED NOTE C, CHANGED FONT STYLE		27 JUNE 07	L.HUEBENER
5	BODY THICKNESS, TERMINAL THICKNESS, PACKAGE HEIGHT ADJUSTED TO MEET JEDEC STD		17 JULY 07	L.HUEBENER

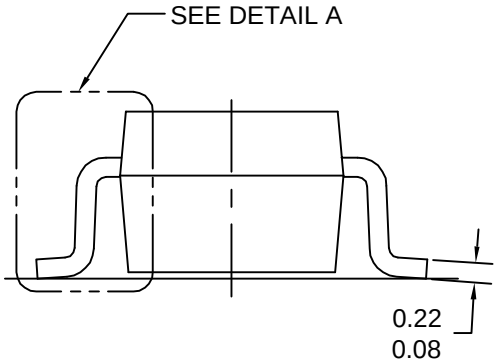


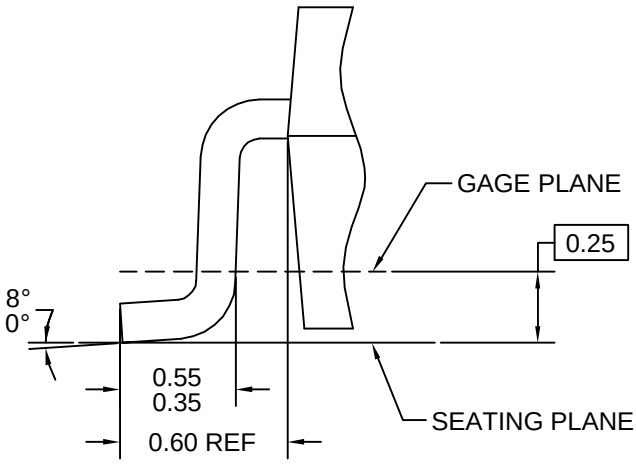
TOP VIEW



LAND PATTERN RECOMMENDATION







NOTES: UNLESS OTHEWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) MA05Brev5

APPROVALS	DATE
DRAWN: L.HUEBENER	17 JULY 07
CHECKED: H.ALLEN	19 JULY 07
APPROVED:	

PROJECTION

FAIRCHILD SEMICONDUCTOR™

5LD,SOT23,JEDEC MO-178,1.6MM

SCALE	SIZE	DRAWING NUMBER	REV
NA	NA	MKT-MA05B	5

FORMERLY: N/A

SHEET : 1 OF 1

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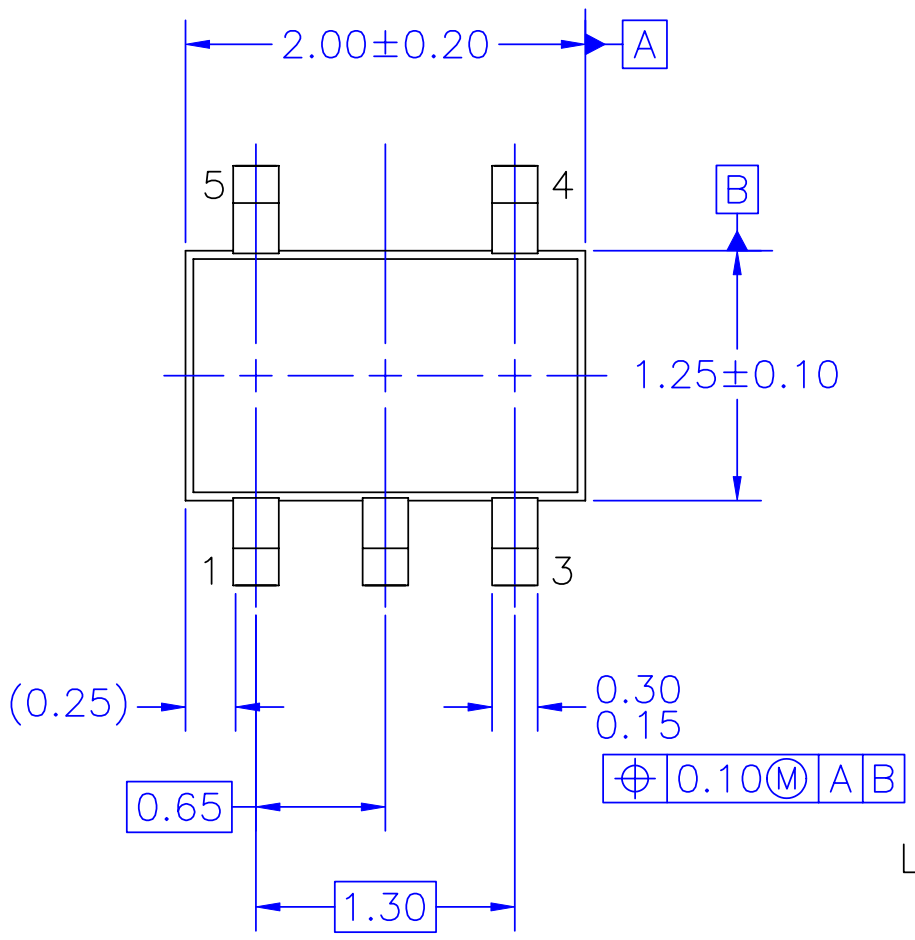
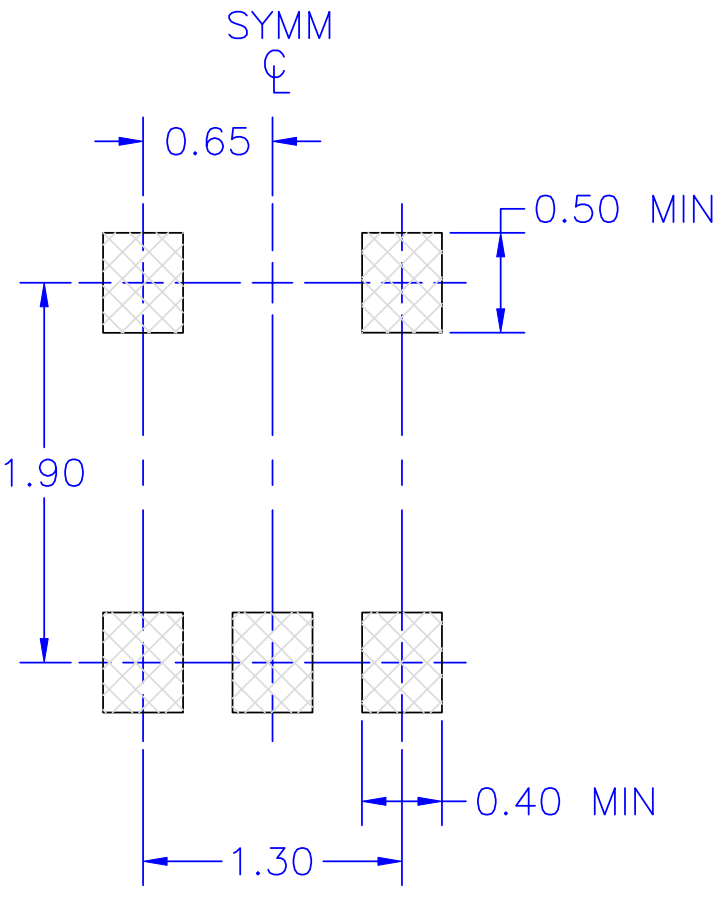
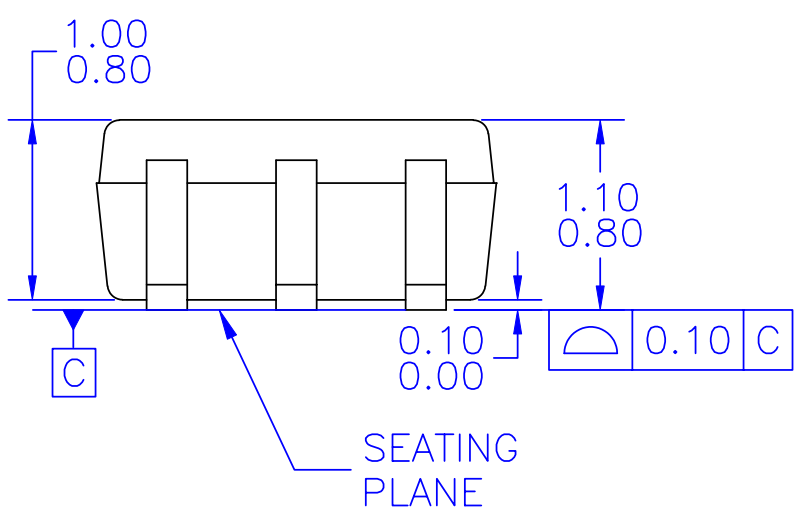
REVISIONS

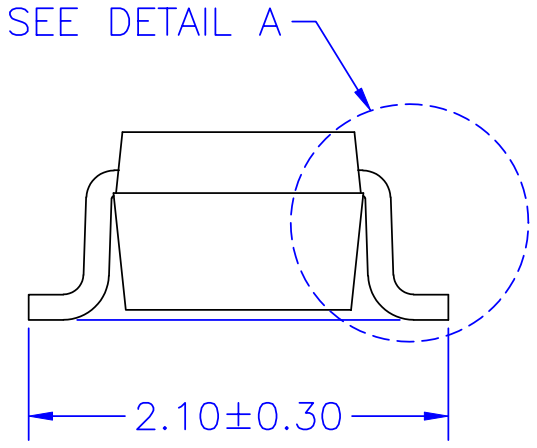
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL			
B	REDRAW AS PER FAIRCHILD TEMPLATE, REDUCE LEAD SPREAD DISTANCE FROM 0.083±0.004 TO 0.082±0.004.			
C	COMPLETE REDRAW AS PER EIAJ SC88A	57500	JUL.22,1998	H. ALLEN
D	REDRAW AS PER STANDARD DRAWING TEMPLATE; ADD MIN FOOT LENGHT DIM; CHANGE DIMENSION STYLE FROM DEVIATION TO LIMITS. REARRANGE DWG TITLE. ADD DWG NUMBER&REV. AT LOWER LEFT CORNER OF TEMPLATE.	04899	AUG.02,1999	MAG
5	CHG LD SPREAD DIM FR 2.10±0.10 TO 2.10±0.30; DETAIL A: CHG LD TIP DIM FR $^{0.45}_{0.30}$ TO $^{0.46}_{0.26}$; REM LD DIM (0.43)	CB/013/07	17JAN2007	SR

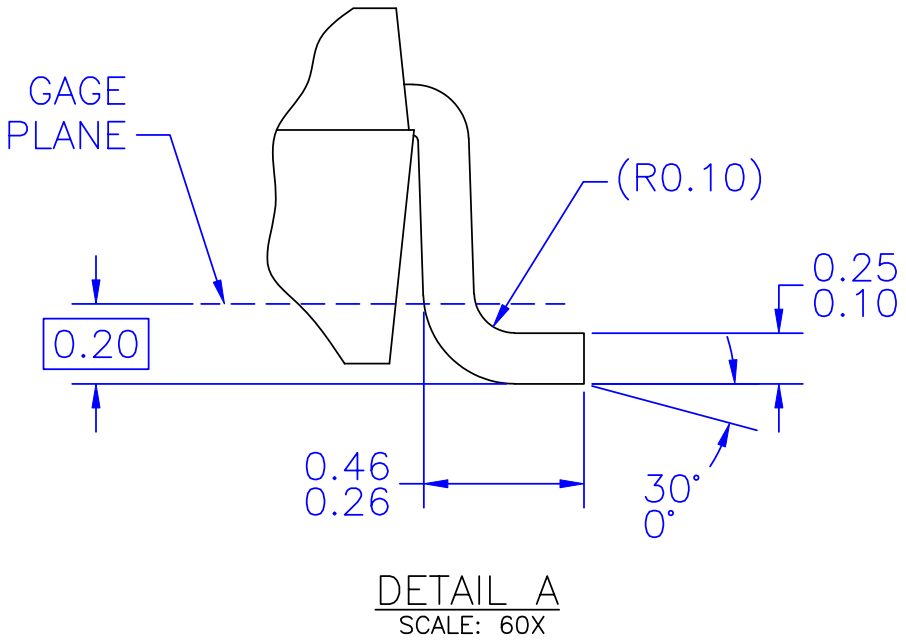




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 60X

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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

APPROVALS	DATE
DRAWN: J. GOMEZ	17JAN2007
CHECKED: B.M. RULONA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

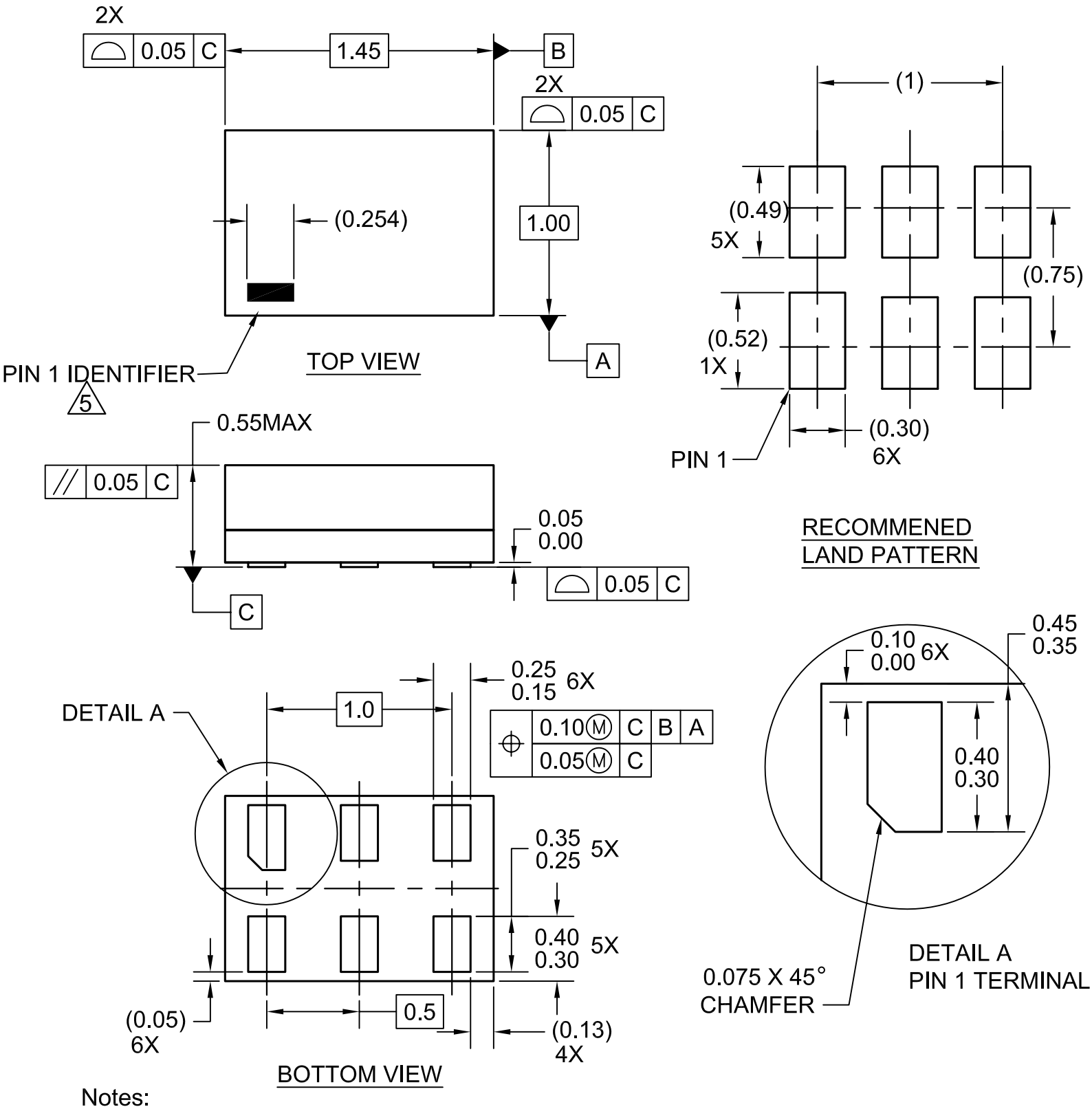
FAIRCHILD SEMICONDUCTOR™ CEBU PHILIPPINES

5LD, SC-70,
EIAJ SC-88A, 1.25MM WIDE

SCALE	SIZE	DRAWING NUMBER	REV
30:1	A3	MKT-MAA05A	5

FORMERLY: N/A SHEET : 1 OF 1

MAA05AREV5



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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