

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT573

**Octal D-type transparent latch;
3-state**

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT573

FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable (\overline{OE}) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at

the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay | C _L = 15 pF; V _{CC} = 5 V | | | |
| | D _n to Q _n | | 14 | 17 | ns |
| | LE to Q _n | | 15 | 15 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per latch | notes 1 and 2 | 26 | 26 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF; V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

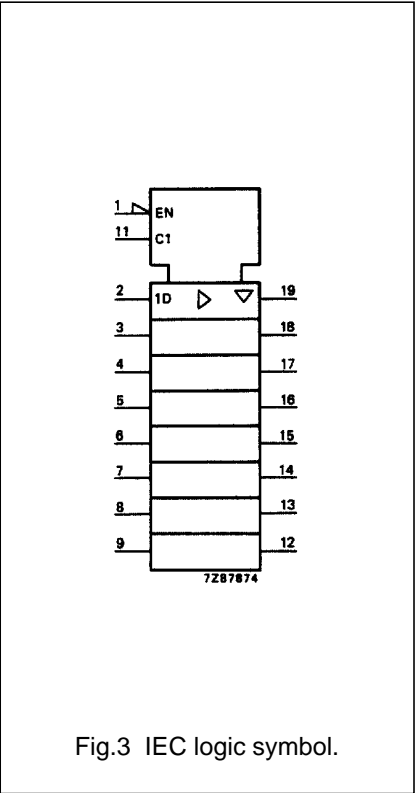
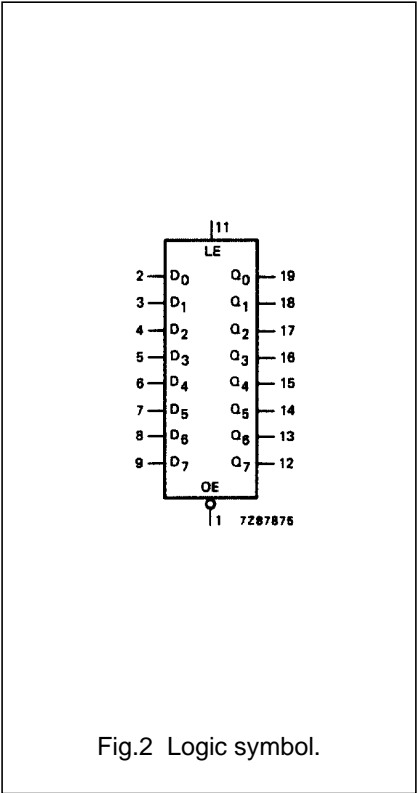
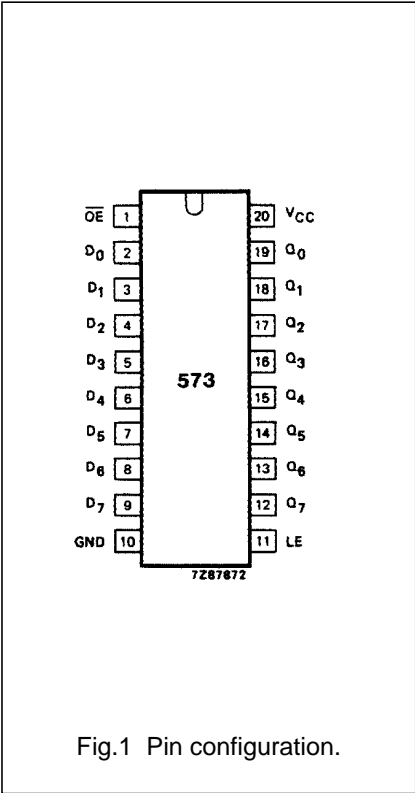
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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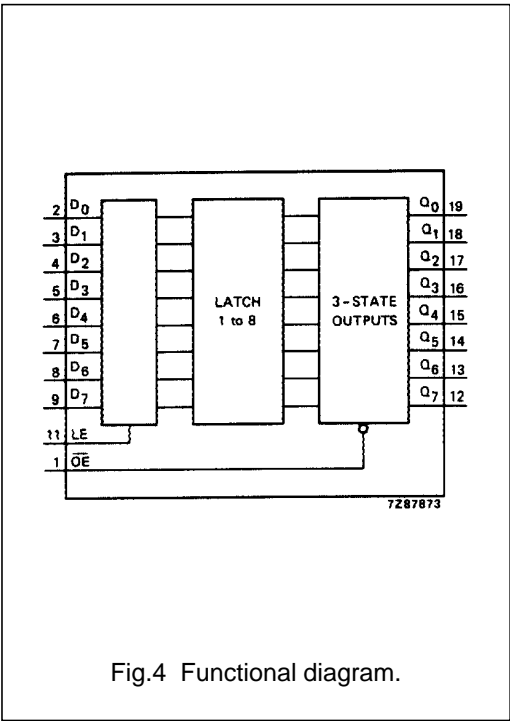
PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------------------------|----------------------------------|--|
| 2, 3, 4, 5, 6, 7, 8, 9 | D ₀ to D ₇ | data inputs |
| 11 | LE | latch enable input (active HIGH) |
| 1 | \overline{OE} | 3-state output enable input (active LOW) |
| 10 | GND | ground (0 V) |
| 19, 18, 17, 16, 15, 14, 13, 12 | Q ₀ to Q ₇ | 3-state latch outputs |
| 20 | V _{CC} | positive supply voltage |



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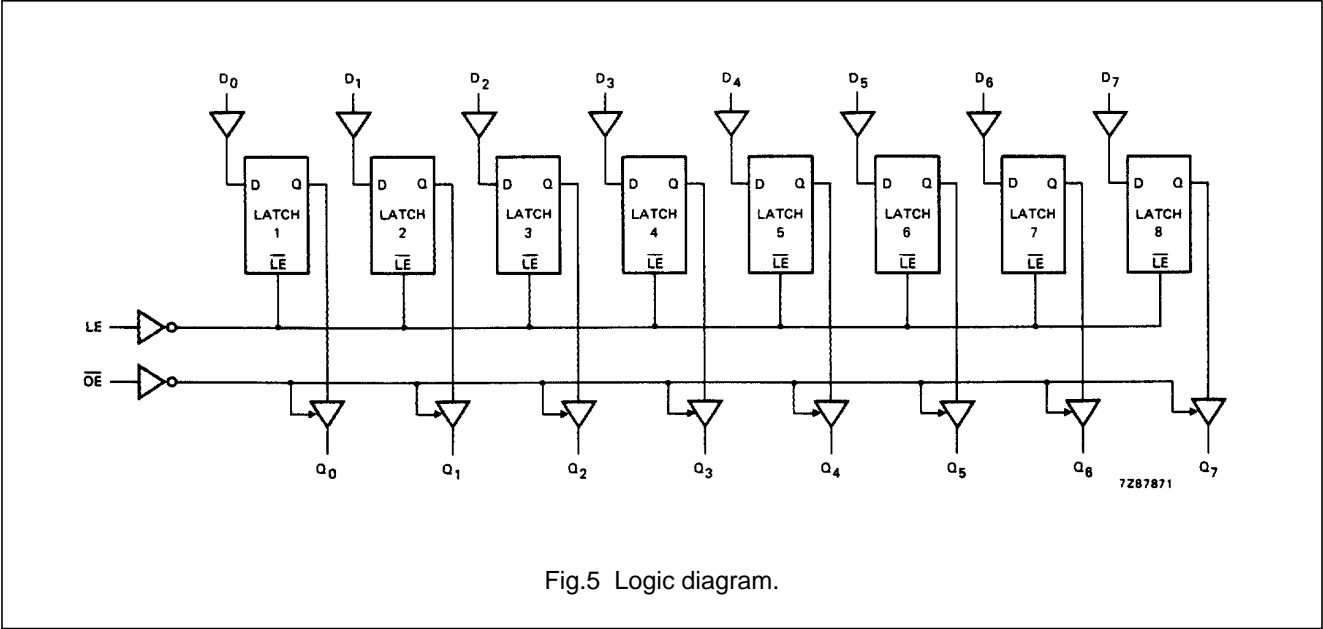


FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS |
|---|-----------------|----|----------------|------------------|----------------------------------|
| | \overline{OE} | LE | D _N | | Q ₀ to Q ₇ |
| enable and read register (transparent mode) | L | H | L | L | L |
| | L | H | H | H | H |
| latch and read register | L | L | L | L | L |
| | L | L | h | H | H |
| latch register and disable outputs | H | L | L | L | Z |
| | H | L | h | H | Z |

Notes

- 1. H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
- Z = high impedance OFF-state



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay D _n to Q _n | | 47 17 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay LE to Q _n | | 50 18 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PZH} / t _{PZL} | 3-state output enable time OE to Q _n | | 44 16 13 | 140 28 24 | | 175 35 30 | | 210 42 36 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time OE to Q _n | | 55 20 16 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _W | enable pulse width HIGH | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{su} | set-up time D _n to LE | 50 10 9 | 11 4 3 | | 65 13 11 | | 75 15 13 | | ns | 2.0 4.5 6.0 | Fig.9 |
| t _h | hold time D _n to LE | 5 5 5 | 3 1 1 | | 5 5 5 | | 5 5 5 | | ns | 2.0 4.5 6.0 | Fig.9 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| D _n | 0.35 |
| LE | 0.65 |
| \overline{OE} | 1.25 |

AC CHARACTERISTICS FOR 74HCT

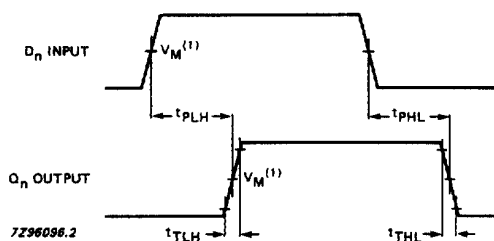
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
| | | 74HCT | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay D _n to Q _n | | 20 | 35 | | 44 | | 53 | ns | 4.5 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay LE to Q _n | | 18 | 35 | | 44 | | 53 | ns | 4.5 | Fig.7 |
| t _{PZH} / t _{PZL} | 3-state output enable time OE to Q _n | | 17 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time OE to Q _n | | 18 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.6 |
| t _W | enable pulse width HIGH | 16 | 5 | | 20 | | 24 | | ns | 4.5 | Fig.7 |
| t _{su} | set-up time D _n to LE | 13 | 7 | | 16 | | 20 | | ns | 4.5 | Fig.9 |
| t _h | hold time D _n to LE | 9 | 4 | | 11 | | 14 | | ns | 4.5 | Fig.9 |

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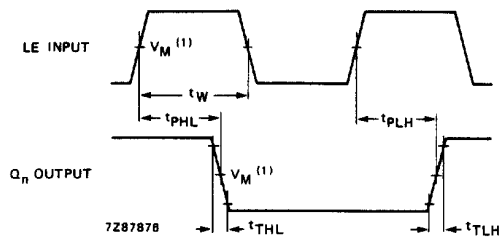
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AC WAVEFORMS



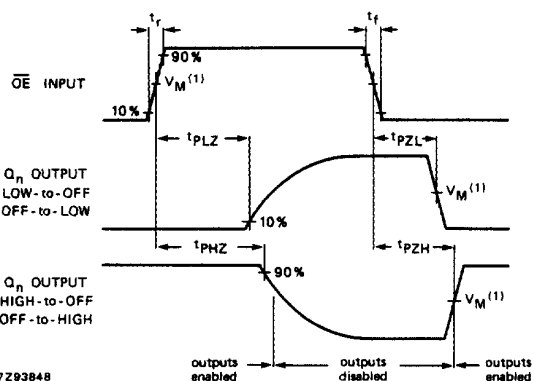
(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.



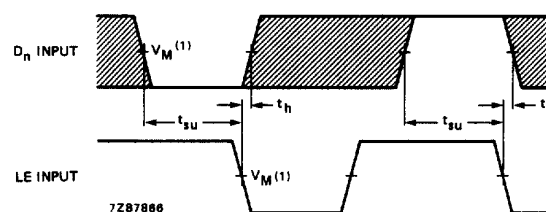
(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.8 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.9 Waveforms showing the data set-up and hold times for D_n input to LE input.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".