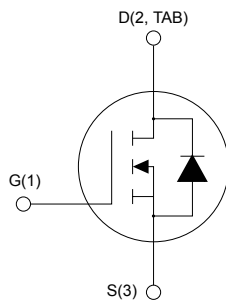
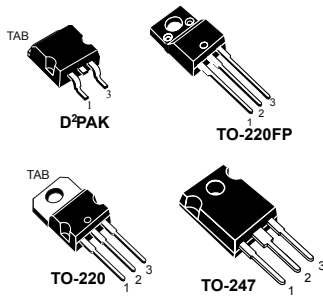


N-channel 650 V, 70 mΩ typ., 33 A, MDmesh M5 Power MOSFETs
in D²PAK, TO-220FP, TO-220 and TO-247 packages



AM01475v1_noZen



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STB42N65M5	650 V	79 mΩ	33 A
STF42N65M5			
STP42N65M5			
STW42N65M5			

- Extremely low R_{DS(on)}
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links

[STB42N65M5](#)

[STF42N65M5](#)

[STP42N65M5](#)

[STW42N65M5](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220, TO-247	TO-220FP	
V _{GS}	Gate-source voltage	±25		V
I _D	Drain current (continuous) at T _C = 25 °C	33	33 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	20.8	20.8 ⁽¹⁾	
I _{DM} ⁽²⁾	Drain current (pulsed)	132	132	A
P _{TOT}	Total power dissipation at T _C = 25 °C	190	40	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)		2500	V
T _J	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			°C

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- I_{SD} ≤ 33 A, di/dt ≤ 400 A/μs, V_{DD} = 400 V, V_{DS} (peak) < V_{(BR)DSS}.

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	TO-220	TO-247	TO-220FP	
R _{thJC}	Thermal resistance, junction-to-case	0.66			3.1	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	30 ⁽¹⁾	62.5	50	62.5	°C/W

- When mounted on an 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max.)	7	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	950	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 16.5\text{ A}$		70	79	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	4650	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse transfer capacitance		-	3.2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	285	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	100	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.1	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 33\text{ A}$,	-	98	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 19. Test circuit for gate charge behavior)	-	28	-	nC
Q_{gd}	Gate-drain charge		-	39	-	nC

- $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.
- $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 20. Test circuit for inductive load switching and diode recovery times and Figure 23. Switching time waveform)	-	52	-	ns
$t_{r(v)}$	Voltage rise time		-	8.4	-	ns
$t_{f(i)}$	Current fall time		-	8.7	-	ns
$t_{c(off)}$	Crossing time		-	14	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		33	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		132	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 33\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	400		ns
Q_{rr}	Reverse recovery charge		-	7		μC
I_{RRM}	Reverse recovery current		-	35		A
t_{rr}	Reverse recovery time	$I_{SD} = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	532		ns
Q_{rr}	Reverse recovery charge		-	10		μC
I_{RRM}	Reverse recovery current		-	38		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

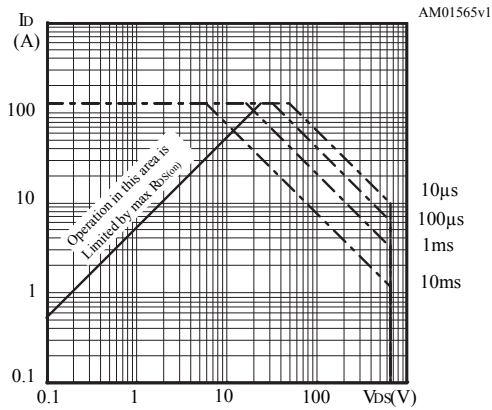
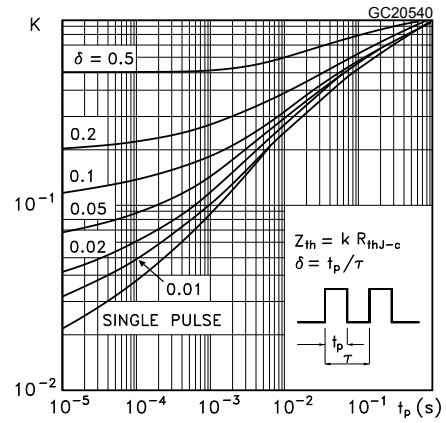
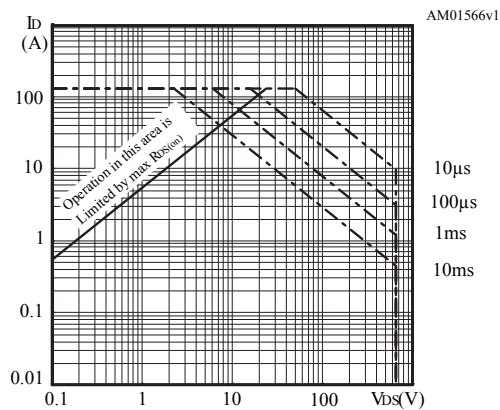
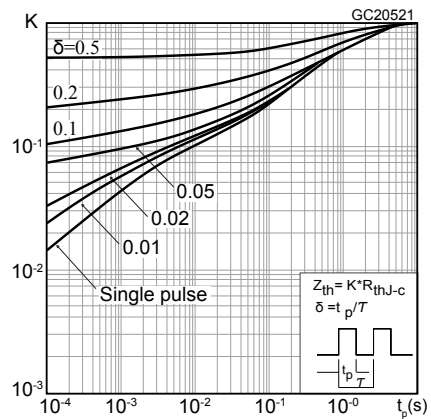
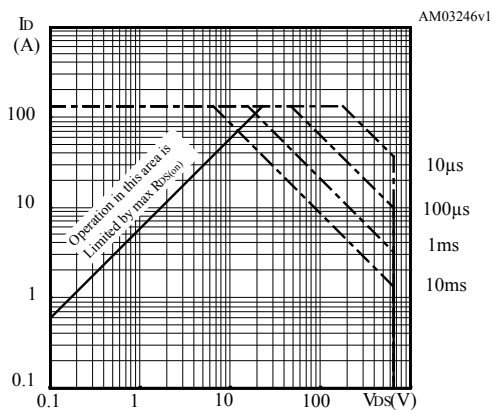
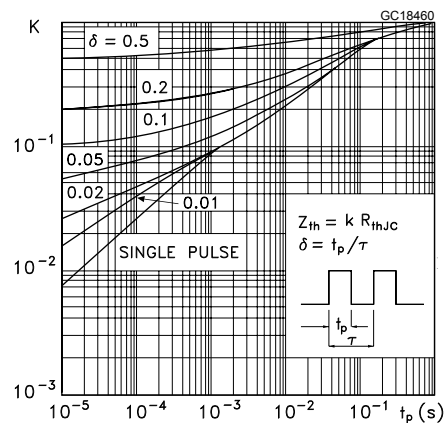
Figure 1. Safe operating area for D²PAK, TO-220

Figure 2. Normalized transient thermal impedance for D²PAK, TO-220

Figure 3. Safe operating area for TO-220FP

Figure 4. Normalized transient thermal impedance for TO-220FP

Figure 5. Safe operating area for TO-247

Figure 6. Normalized transient thermal impedance for TO-247


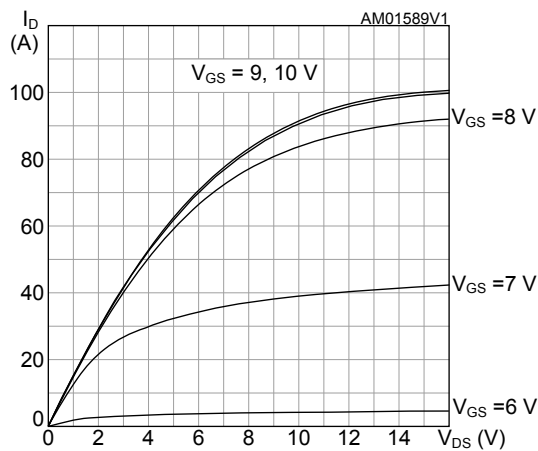
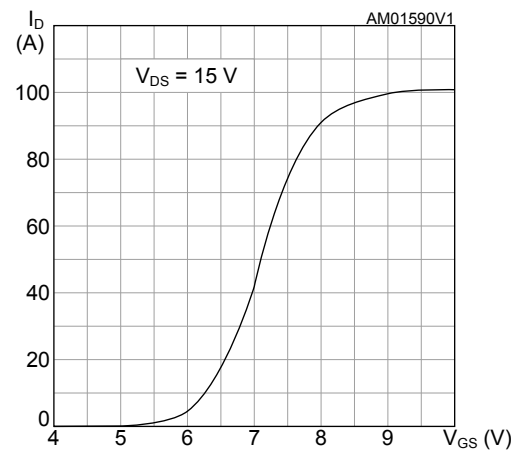
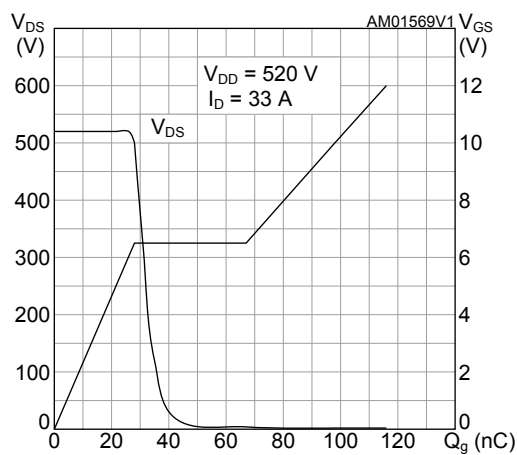
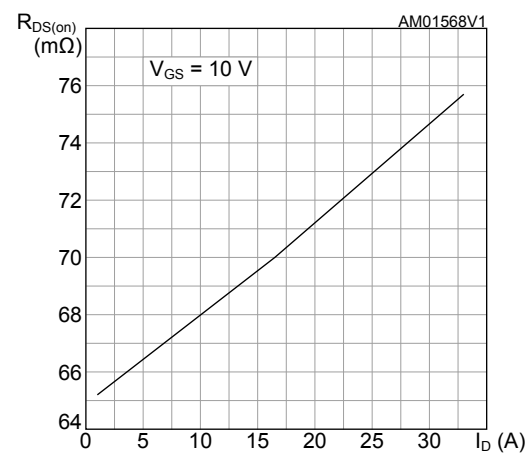
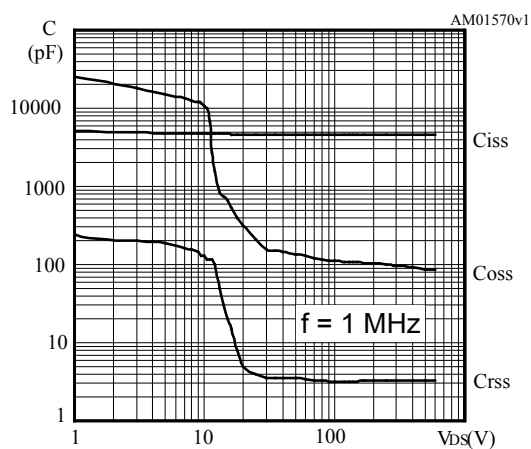
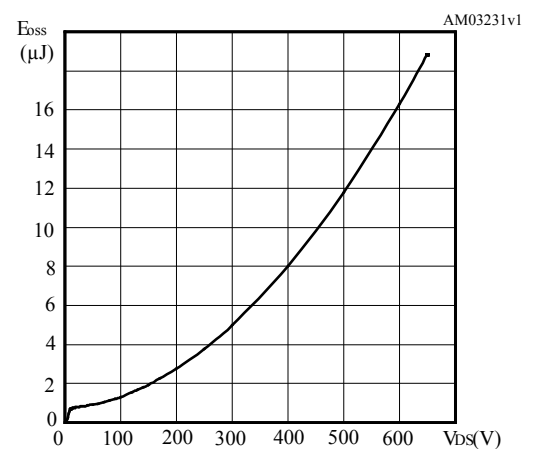
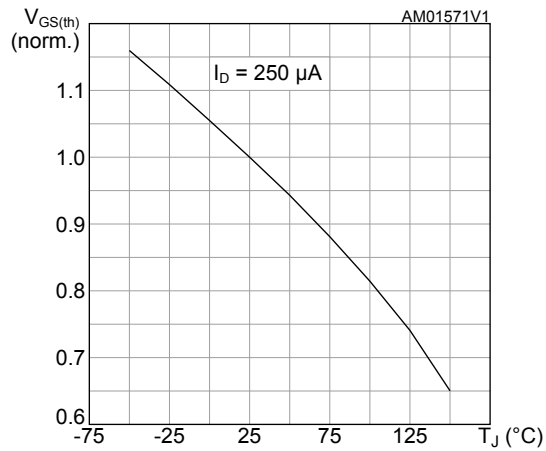
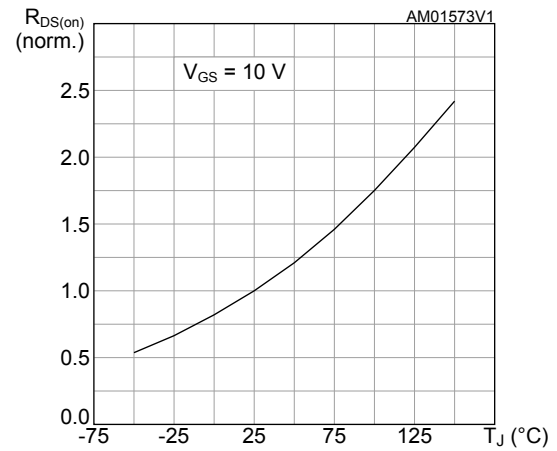
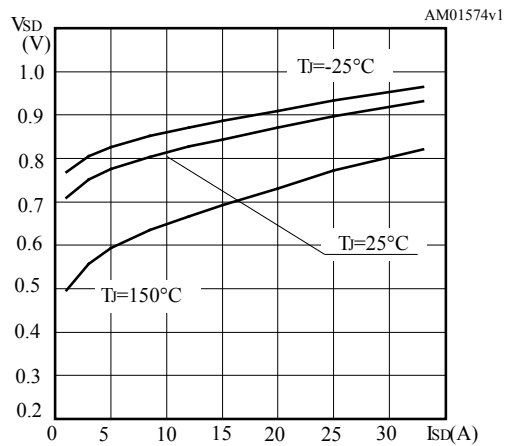
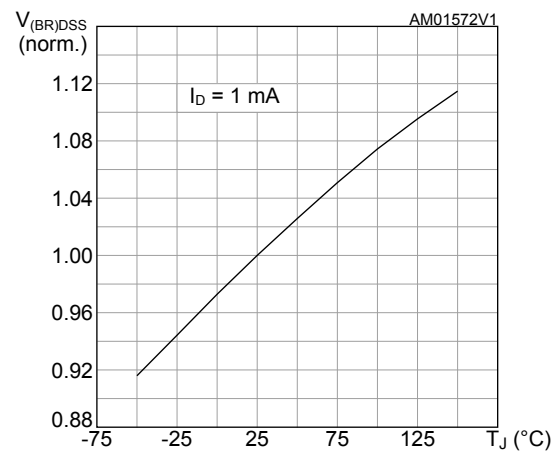
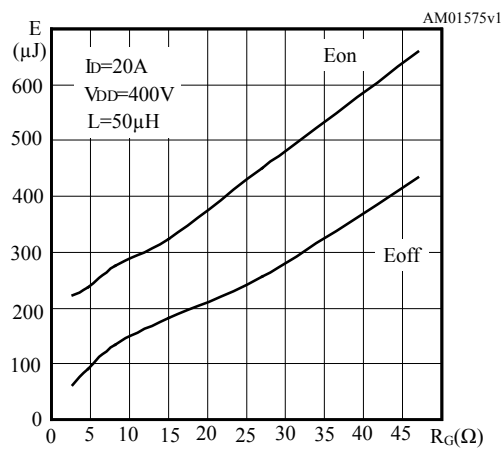
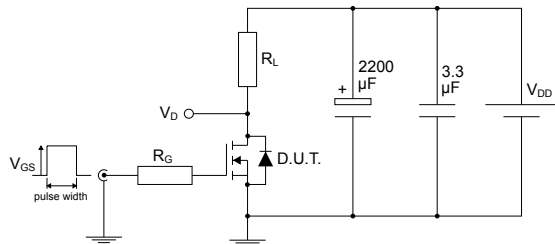
Figure 7. Typical output characteristics

Figure 8. Typical transfer characteristics

Figure 9. Typical gate charge characteristics

Figure 10. Typical drain-source on-resistance

Figure 11. Typical capacitance characteristics

Figure 12. Typical output capacitance stored energy


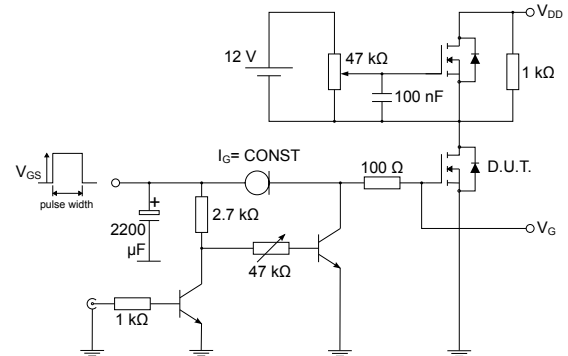
Figure 13. Normalized gate threshold vs temperature

Figure 14. Normalized on-resistance vs temperature

Figure 15. Typical reverse diode forward characteristics

Figure 16. Normalized breakdown voltage vs temperature

Figure 17. Typical inductive load switching energy vs gate resistance


Note: E_{on} including reverse recovery of a SiC diode.

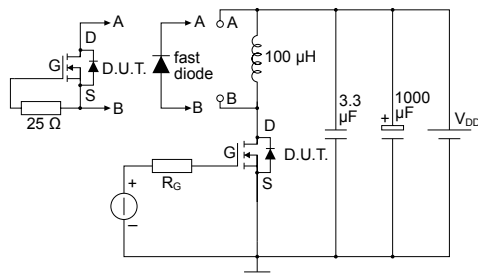
3 Test circuits

Figure 18. Test circuit for resistive load switching times


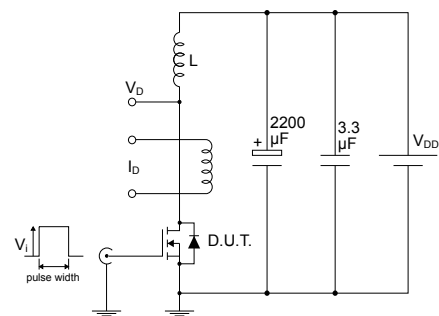
AM01468v1

Figure 19. Test circuit for gate charge behavior


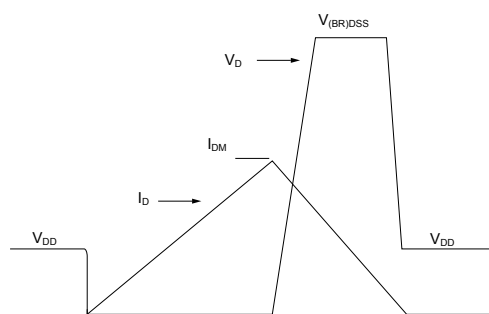
AM01469v1

Figure 20. Test circuit for inductive load switching and diode recovery times


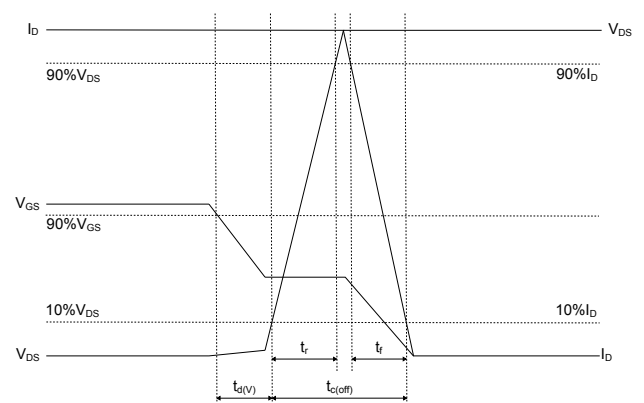
AM01470v1

Figure 21. Unclamped inductive load test circuit


AM01471v1

Figure 22. Unclamped inductive waveform


AM01472v1

Figure 23. Switching time waveform


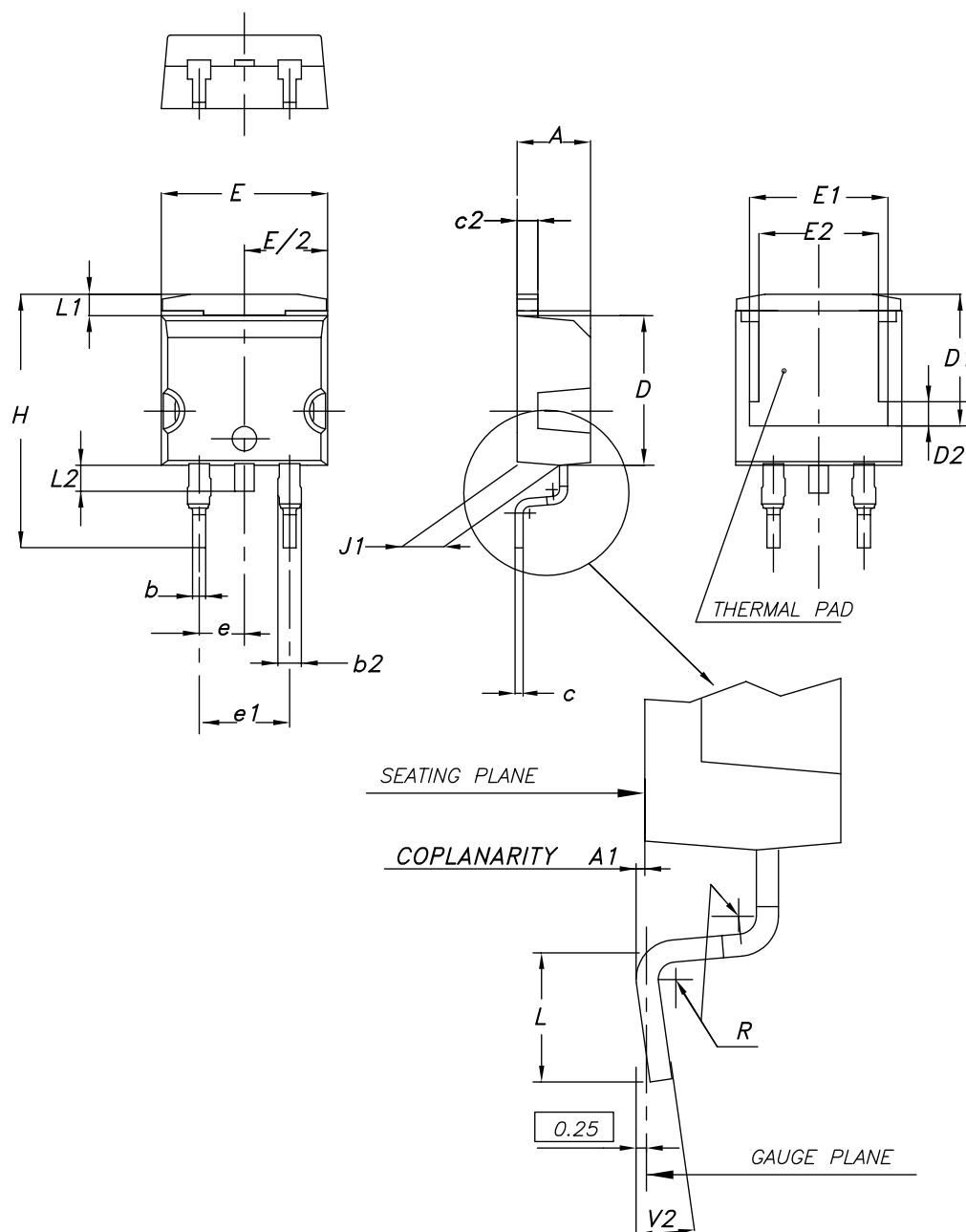
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 24. D²PAK (TO-263) type A2 package outline

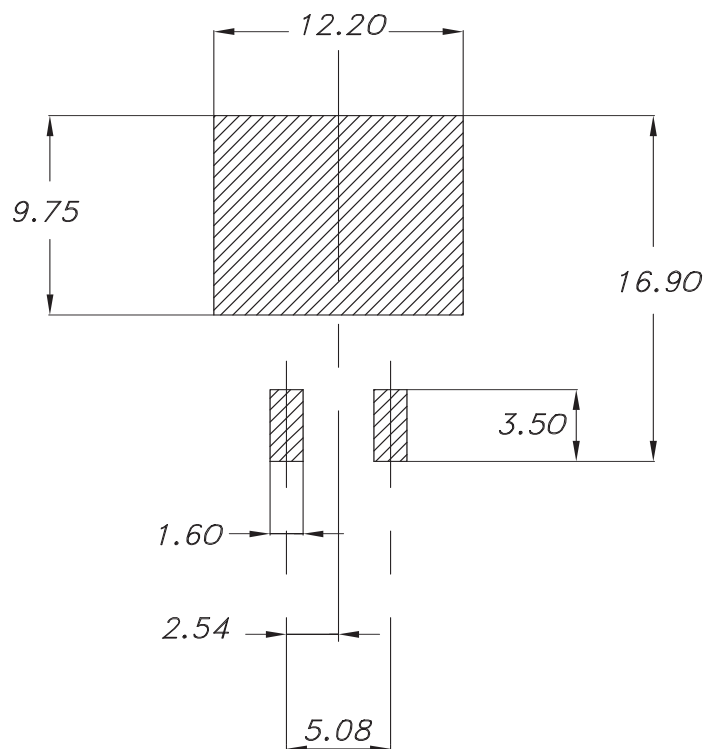


0079457_A2_27

Table 8. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

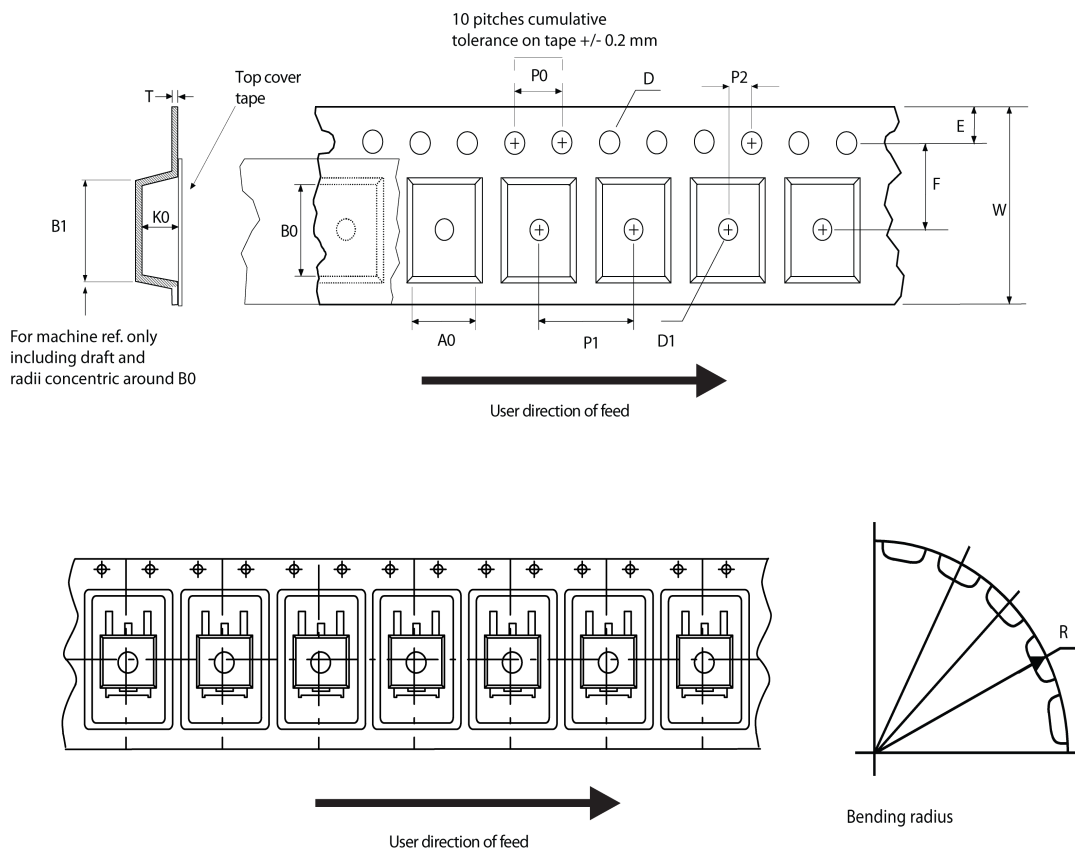
Figure 25. D²PAK (TO-263) recommended footprint (dimensions are in mm)



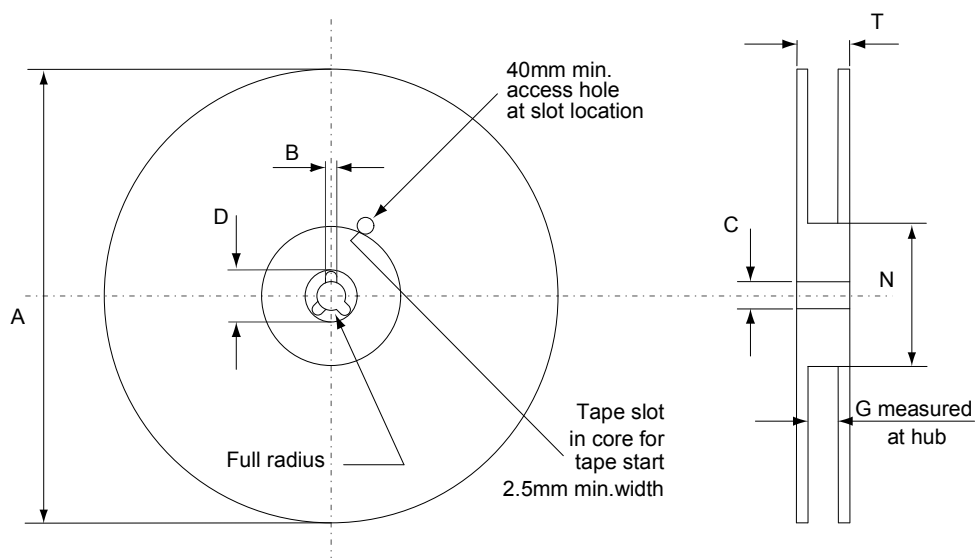
0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 26. D²PAK tape outline



AM08852v1

Figure 27. D²PAK reel outline


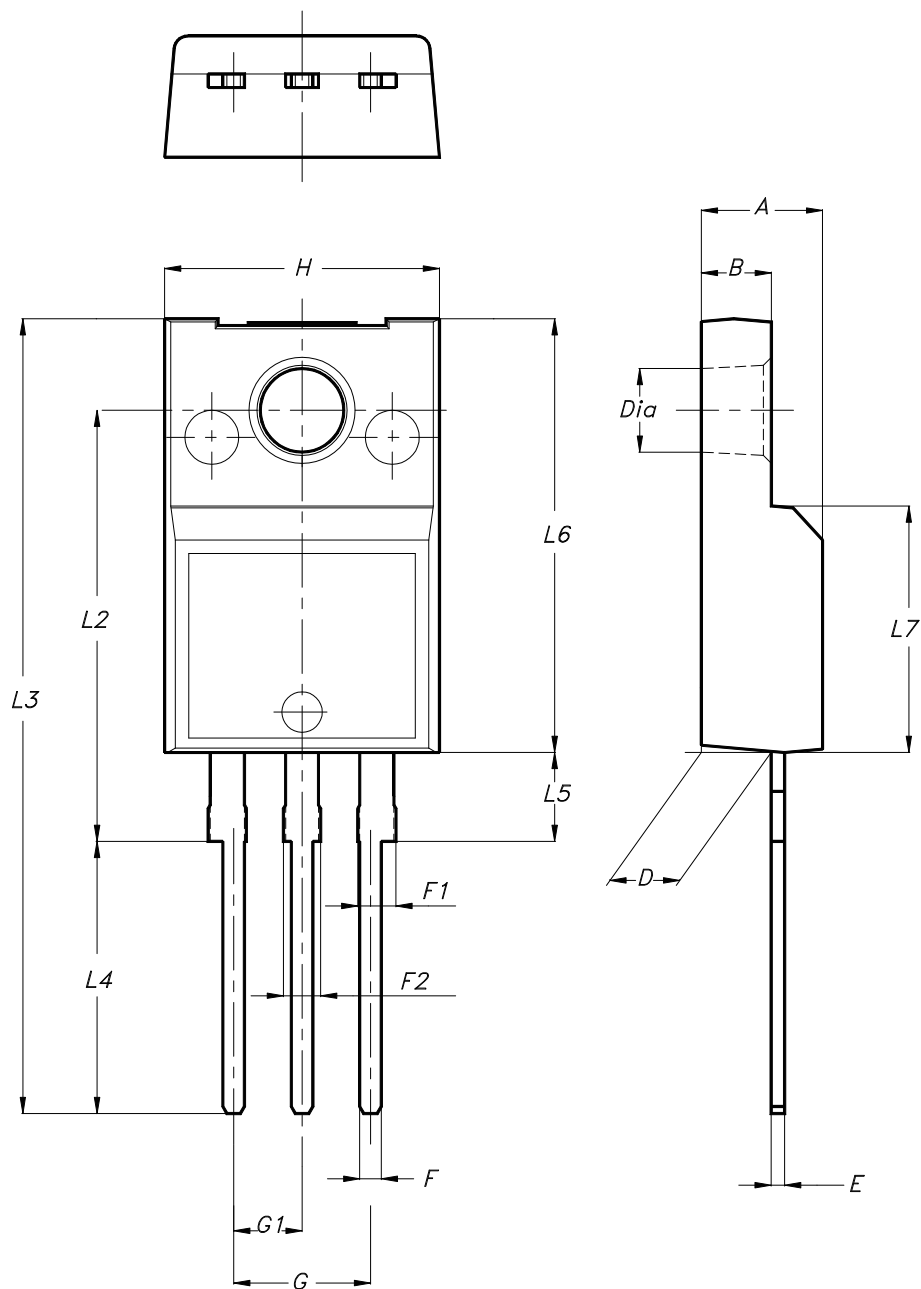
AM06038v1

Table 9. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 TO-220FP package information

Figure 28. TO-220FP type B package outline



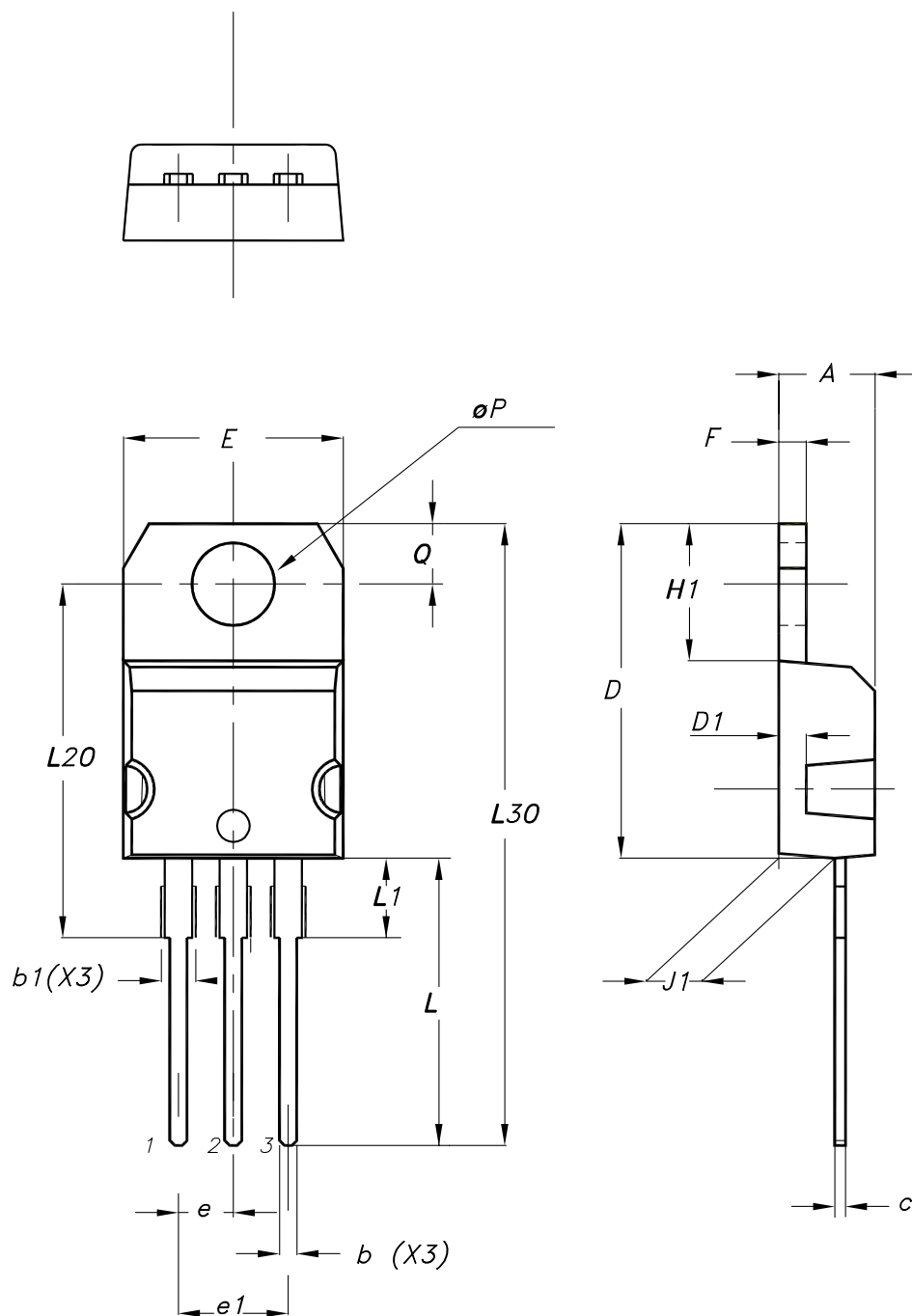
7012510_B_rev.14

Table 10. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.4 TO-220 type A package information

Figure 29. TO-220 type A package outline



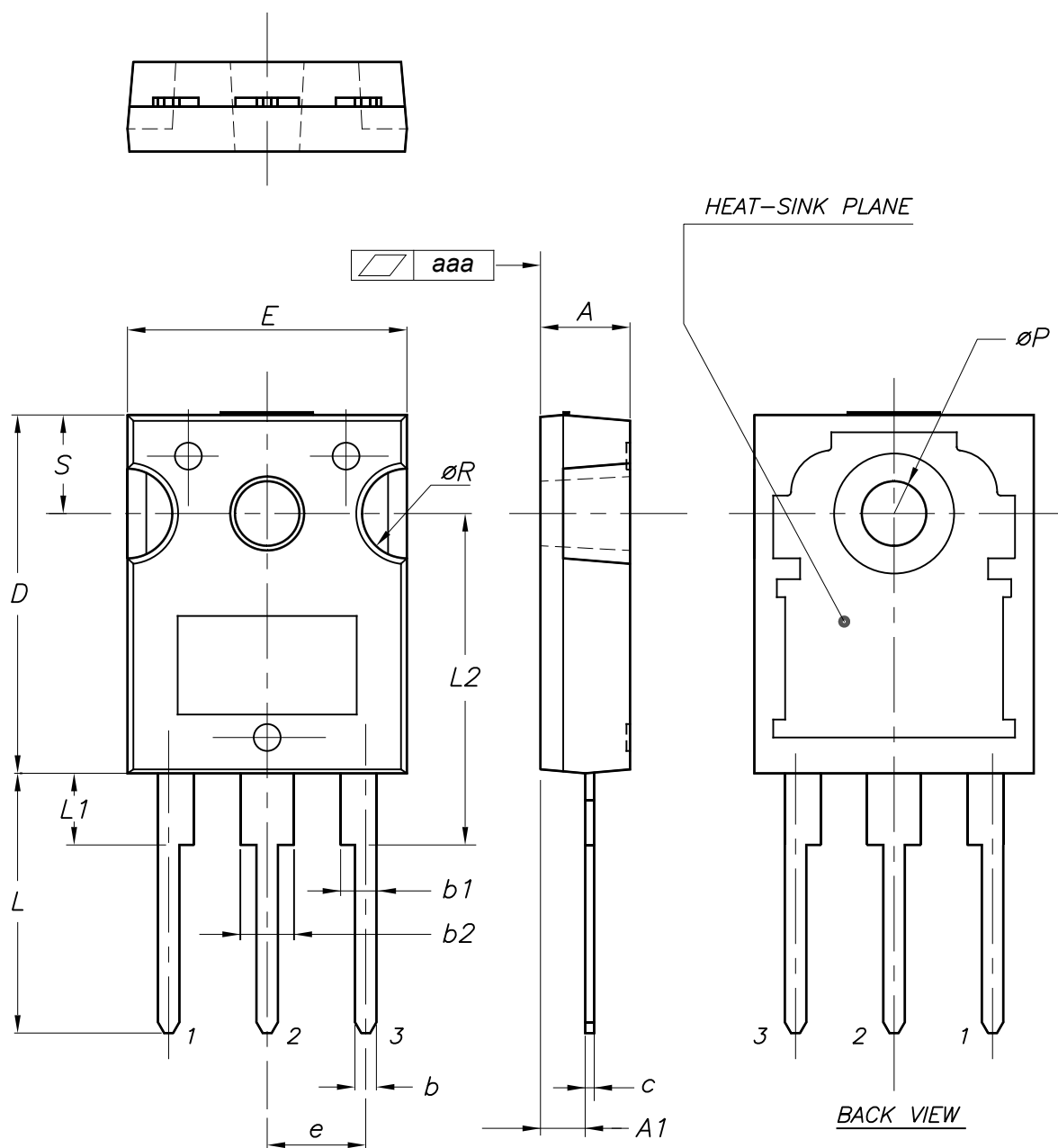
0015988_typeA_Rev_23

Table 11. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.5 TO-247 package information

Figure 30. TO-247 package outline



0075325_10

Table 12. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10



5 Ordering information

Table 13. Order codes

Order code	Marking	Package	Packing
STB42N65M5	42N65M5	D ² PAK	Tape and reel
STF42N65M5		TO-220FP	Tube
STP42N65M5		TO-220	
STW42N65M5		TO-247	

Revision history

Table 14. Document revision history

Date	Version	Changes
16-Jan-2009	1	First release.
15-May-2009	2	Updated <i>figures 9, 10, 11</i> and <i>17</i>
12-Jun-2009	3	<i>Figure 15</i> has been updated
02-May-2019	4	Modified features and description on cover page. Updated <i>Section 4 Package information</i> . Minor text changes.
01-Mar-2024	5	The part number STI42N65M5 has been moved to a separate datasheet and the document has been updated accordingly. Modified I_{AR} value in Table 3. Avalanche characteristics . Updated Section 4: Package information . Minor text changes.



Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	D ² PAK (TO-263) type A2 package information	9
4.2	D ² PAK packing information	12
4.3	TO-220FP package information	14
4.4	TO-220 type A package information	16
4.5	TO-247 package information	18
5	Ordering information	20
	Revision history	21



IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved