DATA SHEET

PCA9554/PCA9554A

8-bit I^2C and SMBus I/O port with interrupt

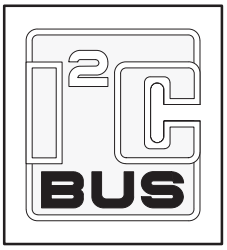
Product data sheet
Supersedes data of 2002 Jul 26

2004 Sep 30

Philips
Semiconductors

PHILIPS

8-bit I²C and SMBus I/O port with interrupt PCA9554/PCA9554A



FEATURES

- Operating power supply voltage range of 2.3 to 5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active-LOW interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Six packages offered: DIP16, SO16, SSOP16, SSOP20, TSSOP16, and HVQFN16

DESCRIPTION

The PCA9554 and PCA9554A are 16-pin CMOS devices that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C/SMBus applications and were developed to enhance the Philips family of I²C I/O expanders. The improvements include higher drive capability, 5V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc.

The PCA9554/54A consist of an 8-bit Configuration register (Input or Output selection); 8-bit Input register, 8-bit Output register and an 8-bit Polarity inversion register (Active-HIGH or Active-LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion Register. All registers can be read by the system master. Although pin to pin and I²C address compatible with the PCF8574 series, software changes are required due to the enhancements and are discussed in *Application Note AN469*.

The PCA9554/54A open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C address and allow up to eight devices to share the same I²C/SMBus. The PCA9554A is identical to the PCA9554 except that the fixed I²C address is different allowing up to sixteen of these devices (eight of each) on the same I²C/SMBus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-Pin Plastic DIP	–40 °C to +85 °C	PCA9554N	PCA9554N	SOT38-1
16-Pin Plastic SO (wide)	–40 °C to +85 °C	PCA9554D	PCA9554D	SOT162-1
16-Pin Plastic SSOP	–40 °C to +85 °C	PCA9554DB	9554DB	SOT338-1
20-Pin Plastic SSOP	–40 °C to +85 °C	PCA9554TS	PCA9554	SOT266-1
16-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9554PW	9554DH	SOT403-1
16-Pin Plastic HVQFN	–40 °C to +85 °C	PCA9554BS	9554	SOT629-1
16-Pin Plastic DIP	–40 °C to +85 °C	PCA9554AN	PCA9554AN	SOT38-1
16-Pin Plastic SO (wide)	–40 °C to +85 °C	PCA9554AD	PCA9554AD	SOT162-1
16-Pin Plastic SSOP	–40 °C to +85 °C	PCA9554ADB	9554A	SOT338-1
20-Pin Plastic SSOP	–40 °C to +85 °C	PCA9554ATS	PA9554A	SOT266-1
16-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9554APW	9554ADH	SOT403-1
16-Pin Plastic HVQFN	–40 °C to +85 °C	PCA9554ABS	554A	SOT629-1

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

PIN CONFIGURATION — 16-pin DIP, SO, SSOP, TSSOP

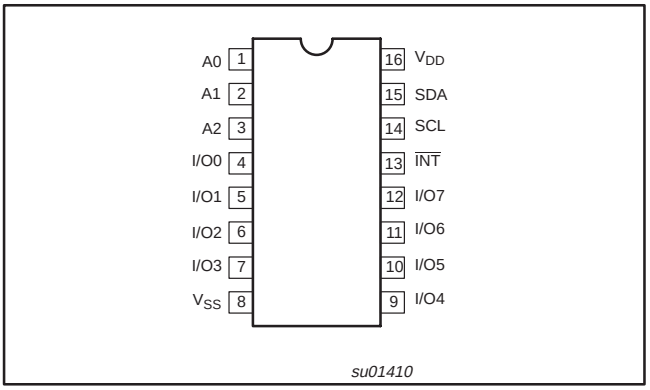


Figure 1. Pin configuration — 16-pin DIP, SO, SSOP, TSSOP

PIN CONFIGURATION — HVQFN

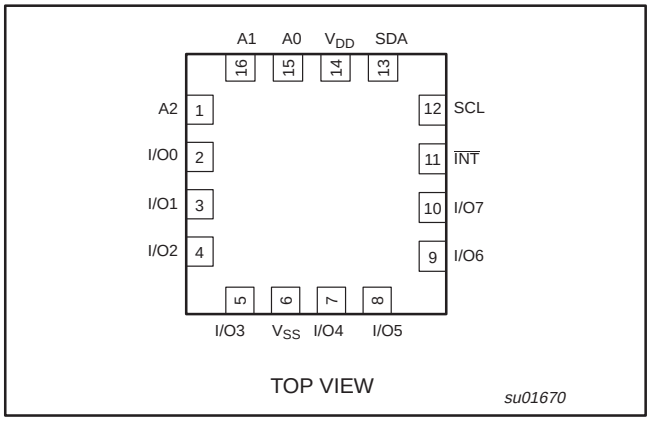


Figure 2. Pin Configuration — HVQFN

PIN CONFIGURATION — 20-pin SSOP

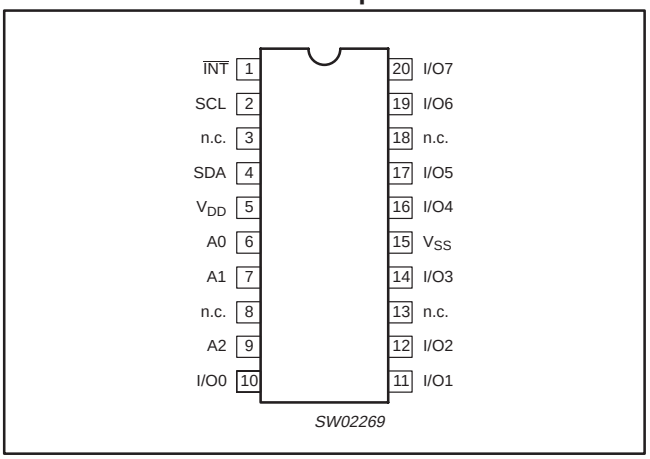


Figure 1. Pin configuration — 20-pin SSOP

PIN DESCRIPTION

DIP16, SO16, SSOP16, TSSOP16 PIN NUMBER	HVQFN16 PIN NUMBER	SSOP20 PIN NUMBER	SYMBOL	FUNCTION
1	15	6	A0	Address input 0
2	16	7	A1	Address input 1
3	1	9	A2	Address input 2
4–7	2–5	10–12, 14	I/O0 to I/O3	I/O0 to I/O3
8	6	15	V_{SS}	Supply ground
9	7–10	16, 17, 19, 20	I/O4 to I/O7	I/O4 to I/O7
13	11	1	$\overline{INT}$	Interrupt output (open drain)
14	12	2	SCL	Serial clock line
15	13	4	SDA	Serial data line
16	14	5	V_{DD}	Supply voltage
–	–	3, 8, 13, 18	n.c.	not connected

BLOCK DIAGRAM

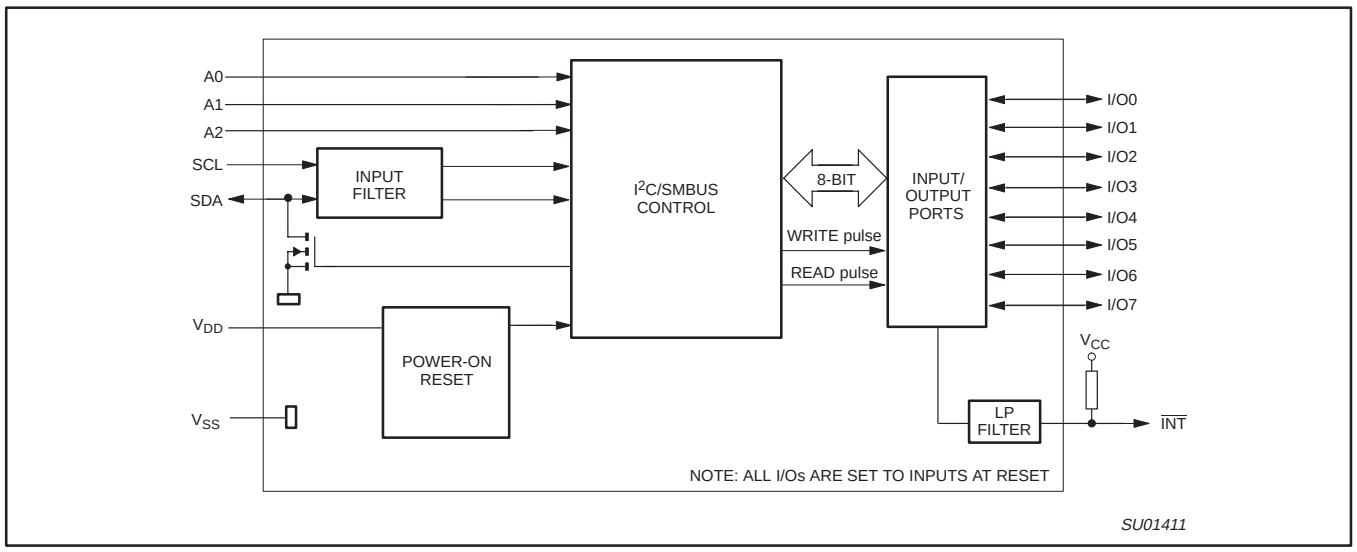


Figure 3. Block diagram

REGISTERS

Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0 – Input Port Register

bit	I7	I6	I5	I4	I3	I2	I1	I0
default	X	X	X	X	X	X	X	X

This register is a read only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level, normally '1' when no external signal externally applied because of the internal pull-up resistors.

Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	1	1	1	1	1	1	1	1

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port Register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Register 3 – Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

Power-on Reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9554 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9554 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

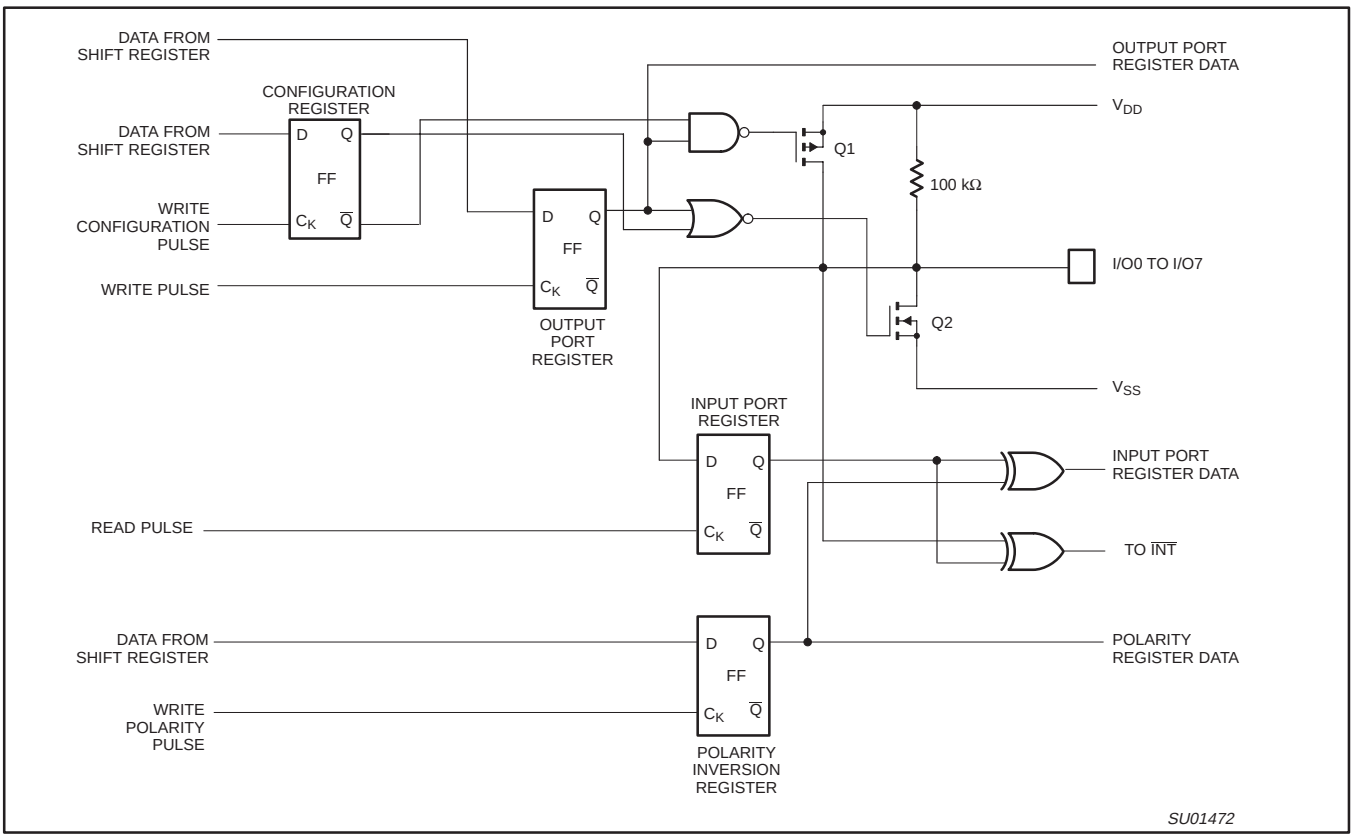
For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

Interrupt Output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

SIMPLIFIED SCHEMATIC OF I/O0 TO I/O7



NOTE: At Power-on Reset, all registers return to default values.

Figure 4. Simplified schematic of I/O0 to I/O7

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ.) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance paths that exist between the pin and either V_{DD} or V_{SS}.

Device address

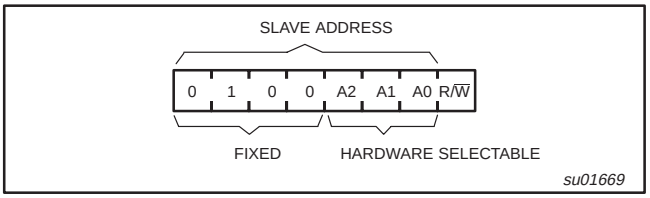


Figure 5. PCA9554 address

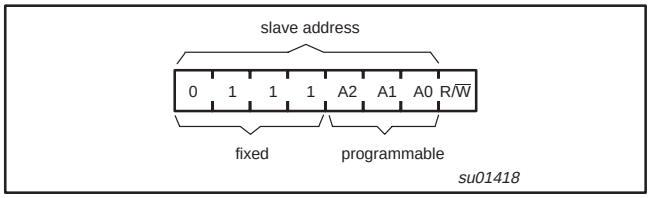


Figure 6. PCA9554A address

Bus transactions

Data is transmitted to the PCA9554/PCA9554A registers using the write mode as shown in Figures 7 and 8. Data is read from the PCA9554/PCA9554A registers using the read mode as shown in Figures 9 and 10. These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

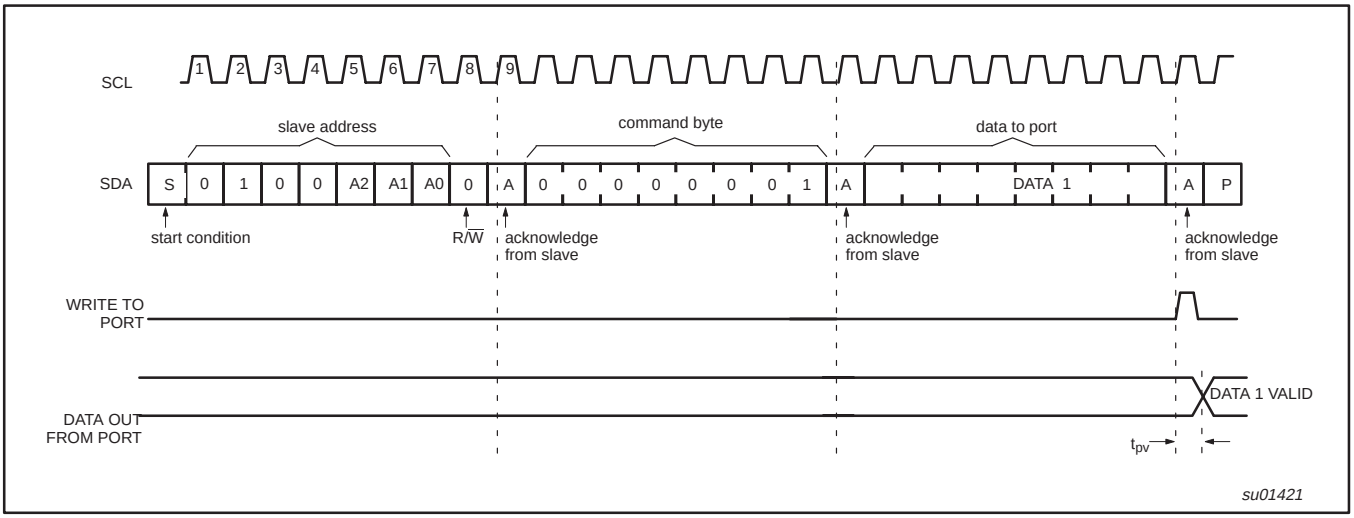


Figure 7. WRITE to output port register

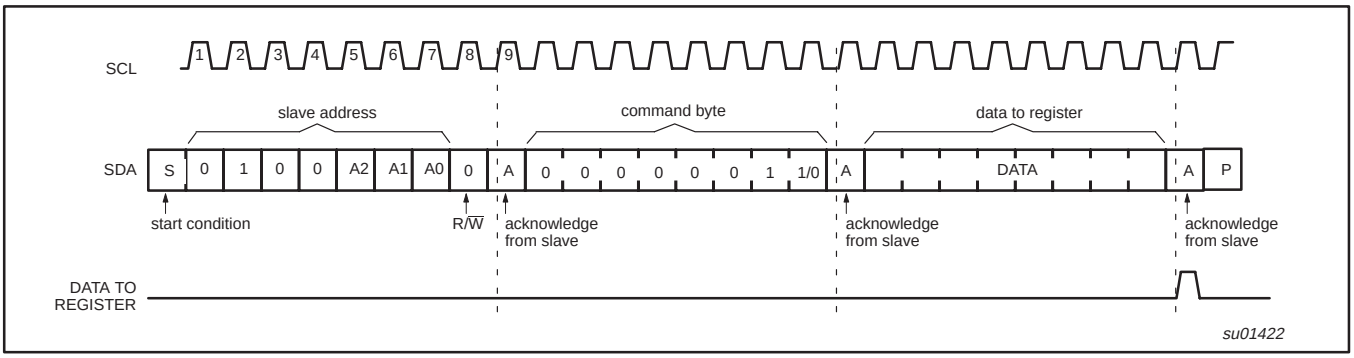


Figure 8. WRITE to configuration or polarity inversion registers

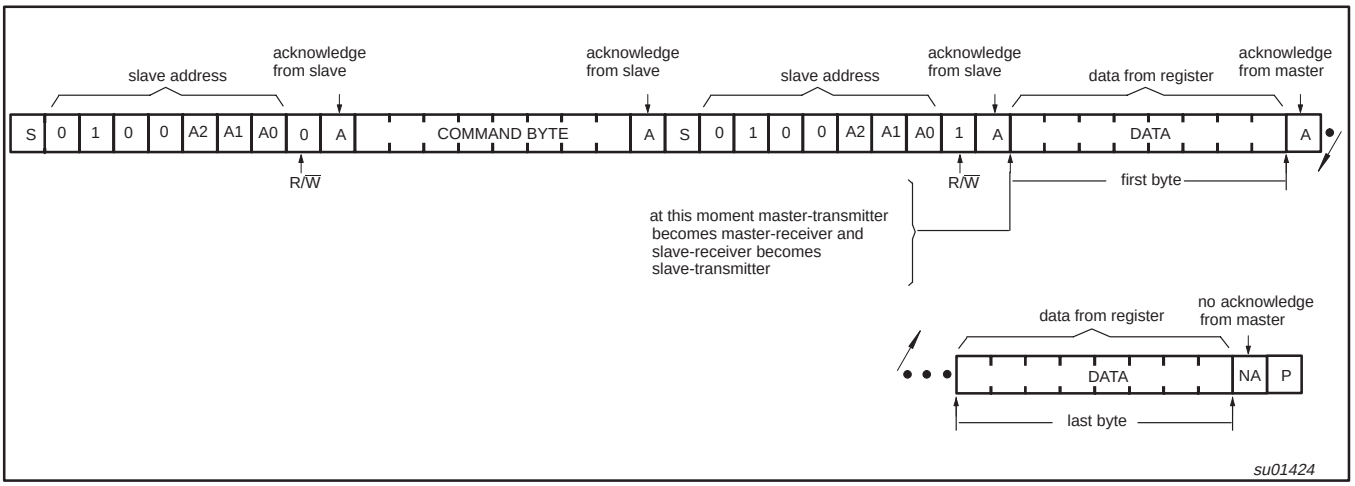
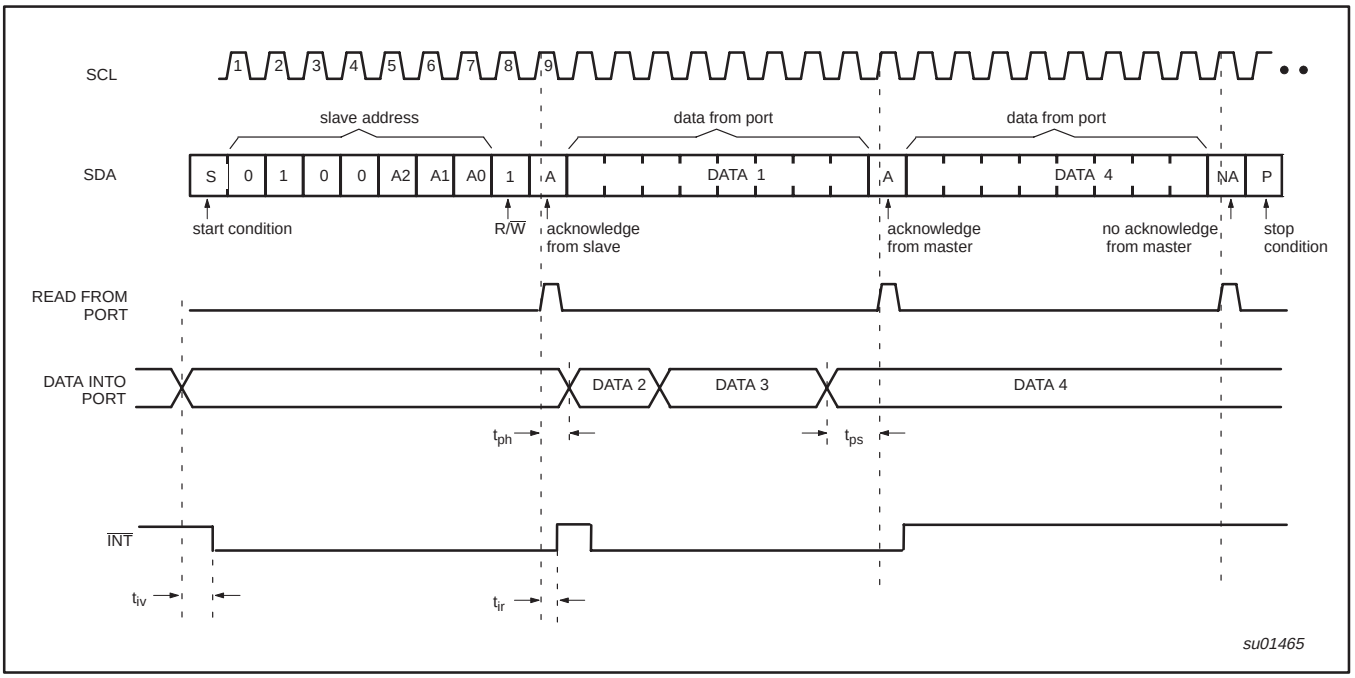


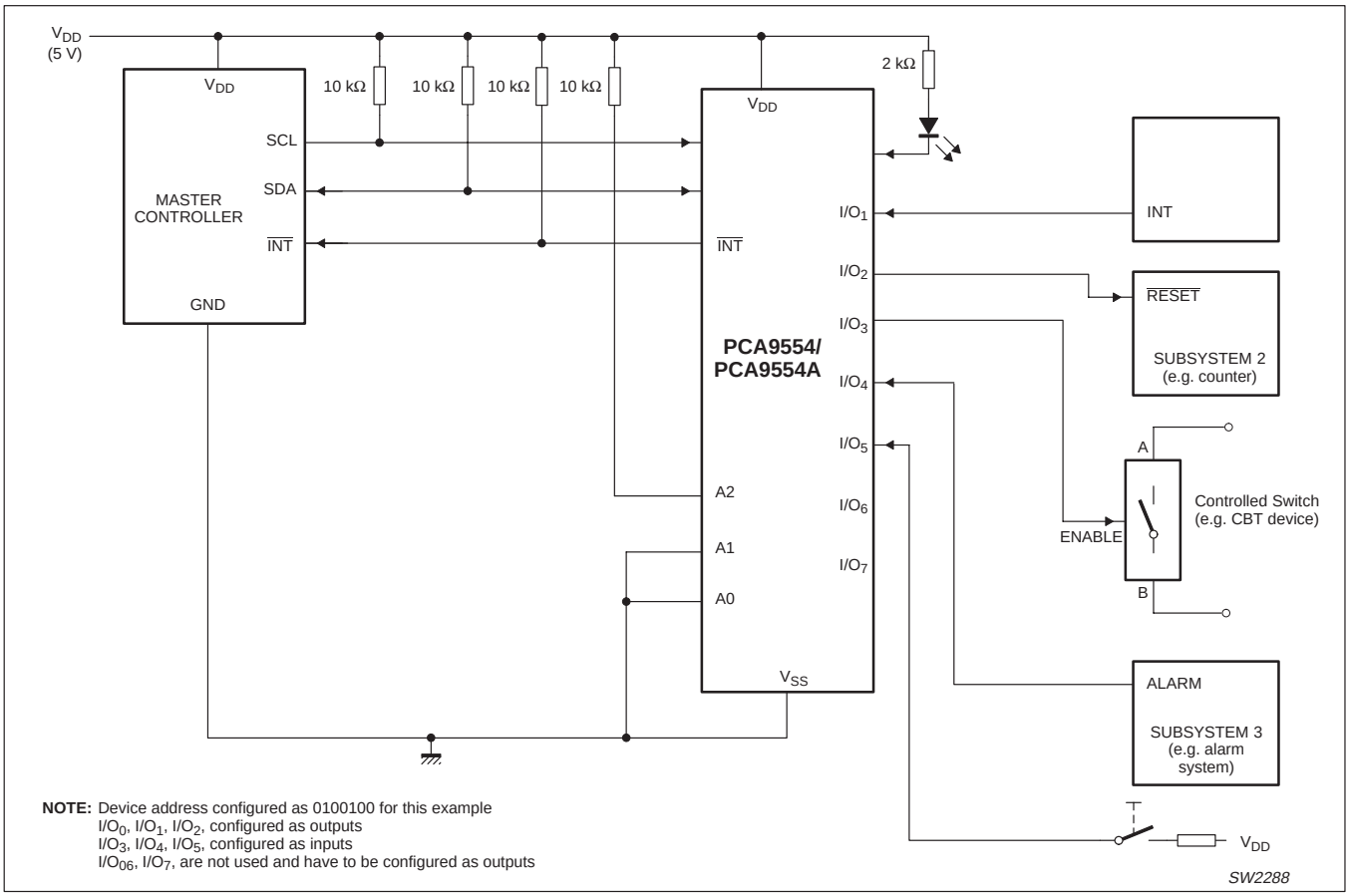
Figure 9. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition.

Figure 10. READ input port register

TYPICAL APPLICATION



NOTE: Device address configured as 0100100 for this example
I/O_0, I/O_1, I/O_2, configured as outputs
I/O_3, I/O_4, I/O_5, configured as inputs
I/O_{06}, I/O_7, are not used and have to be configured as outputs

Figure 11. Typcial application.

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
I_I	DC input current		—	±20	mA
$V_{I/O}$	DC voltage on an I/O		V_{SS} – 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±50	mA
I_{DD}	Supply current		—	85	mA
I_{SS}	Supply current		—	100	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz	—	104	175	µA
I_{stbl}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	550	700	µA
I_{stbh}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
V_{POR}	Power-on reset voltage (Note 1)	No load; $V_I = V_{DD}$ or V_{SS}	—	1.5	1.65	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
I/Os						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V; Note 2	8	10	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 2	10	13	—	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V; Note 2	8	17	—	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V; Note 2	10	24	—	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V; Note 2	8	14	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 2	10	19	—	mA
V_{OH}	HIGH level output voltage	I_{OH} = –8 mA; V_{DD} = 2.3 V; Note 3	1.8	—	—	V
		I_{OH} = –10 mA; V_{DD} = 2.3 V; Note 3	1.7	—	—	V
		I_{OH} = –8 mA; V_{DD} = 3.0 V; Note 3	2.6	—	—	V
		I_{OH} = –10 mA; V_{DD} = 3.0 V; Note 3	2.5	—	—	V
		I_{OH} = –8 mA; V_{DD} = 4.75 V; Note 3	4.1	—	—	V
		I_{OH} = –10 mA; V_{DD} = 4.75 V; Note 3	4.0	—	—	V
I_{IH}	Input leakage current	V_{DD} = 3.6 V; $V_I = V_{DD}$	—	—	1	µA
I_{IL}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	—	—	–100	µA
C_I	Input capacitance		—	3.7	5	pF
C_O	Output capacitance		—	3.7	5	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	—	—	mA
Select Inputs A0, A1, A2						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	µA

NOTES:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.
3. The total current sourced by all I/Os must be limited to 85 mA.

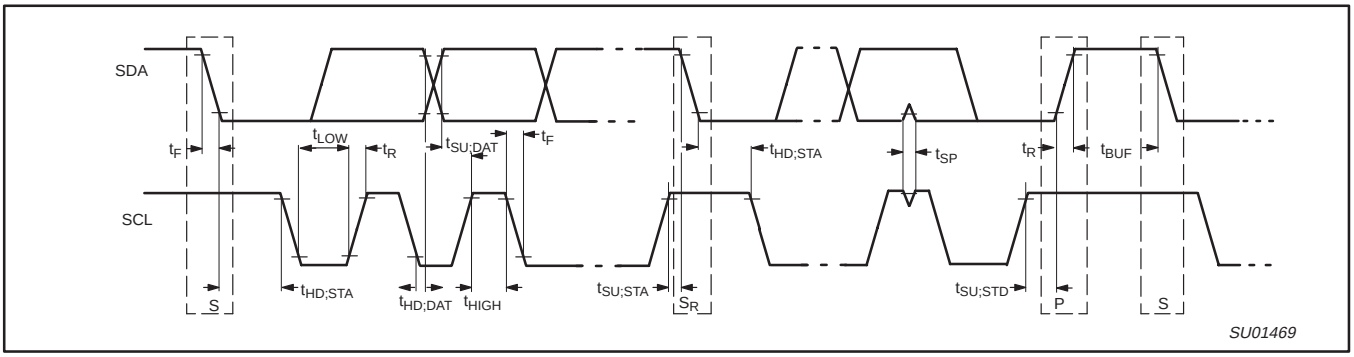


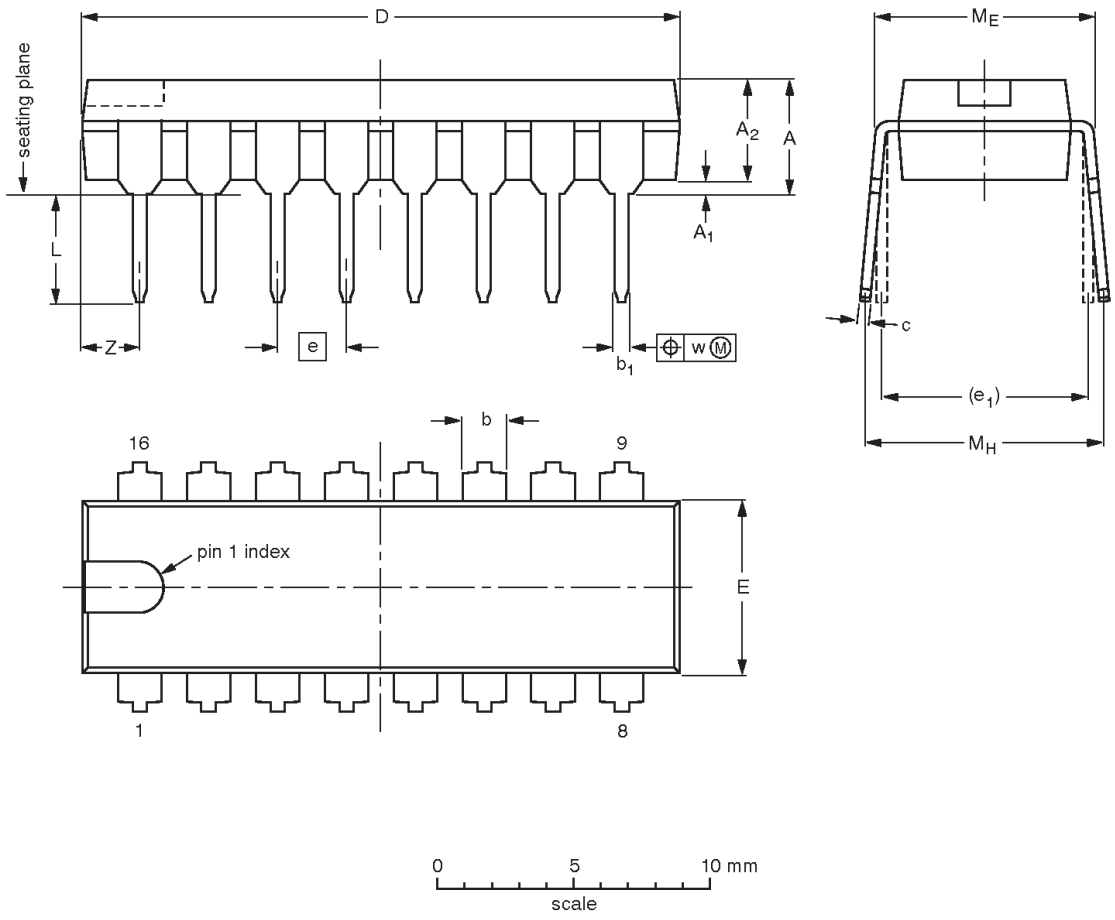
Figure 12. Definition of timing

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	Data out valid time[3]	300	—	50	—	ns
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data setup time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Interrupt Timing						
t_{IV}	Interrupt valid	—	4	—	4	µs
t_{IR}	Interrupt reset	—	4	—	4	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

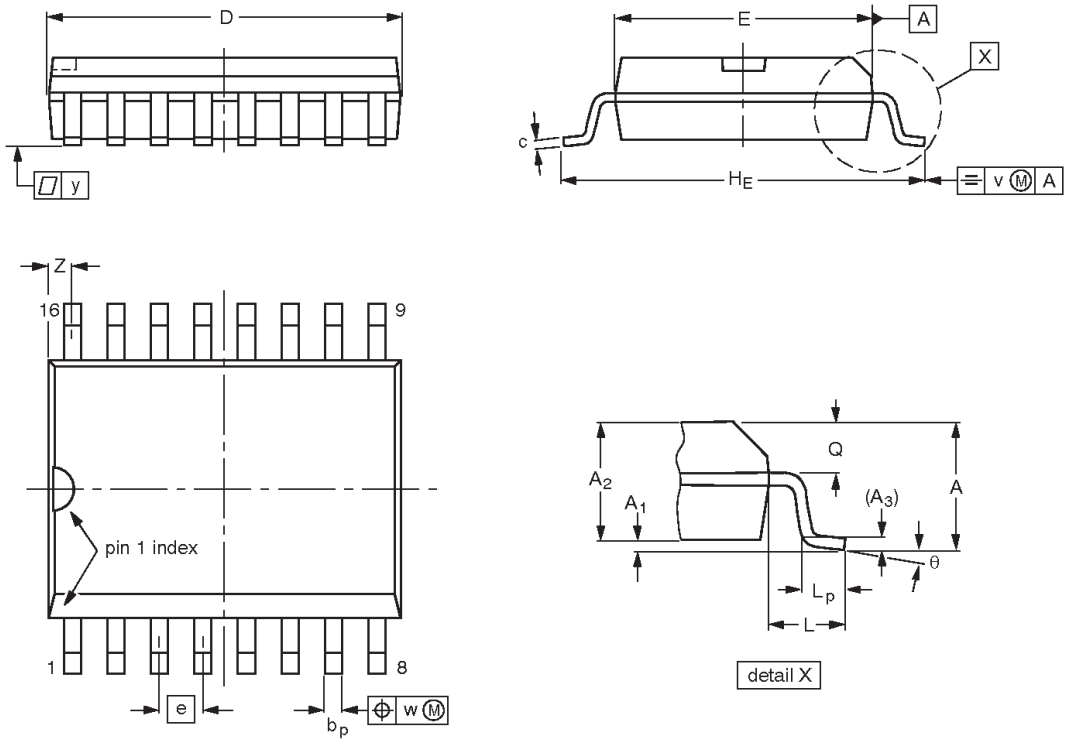
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

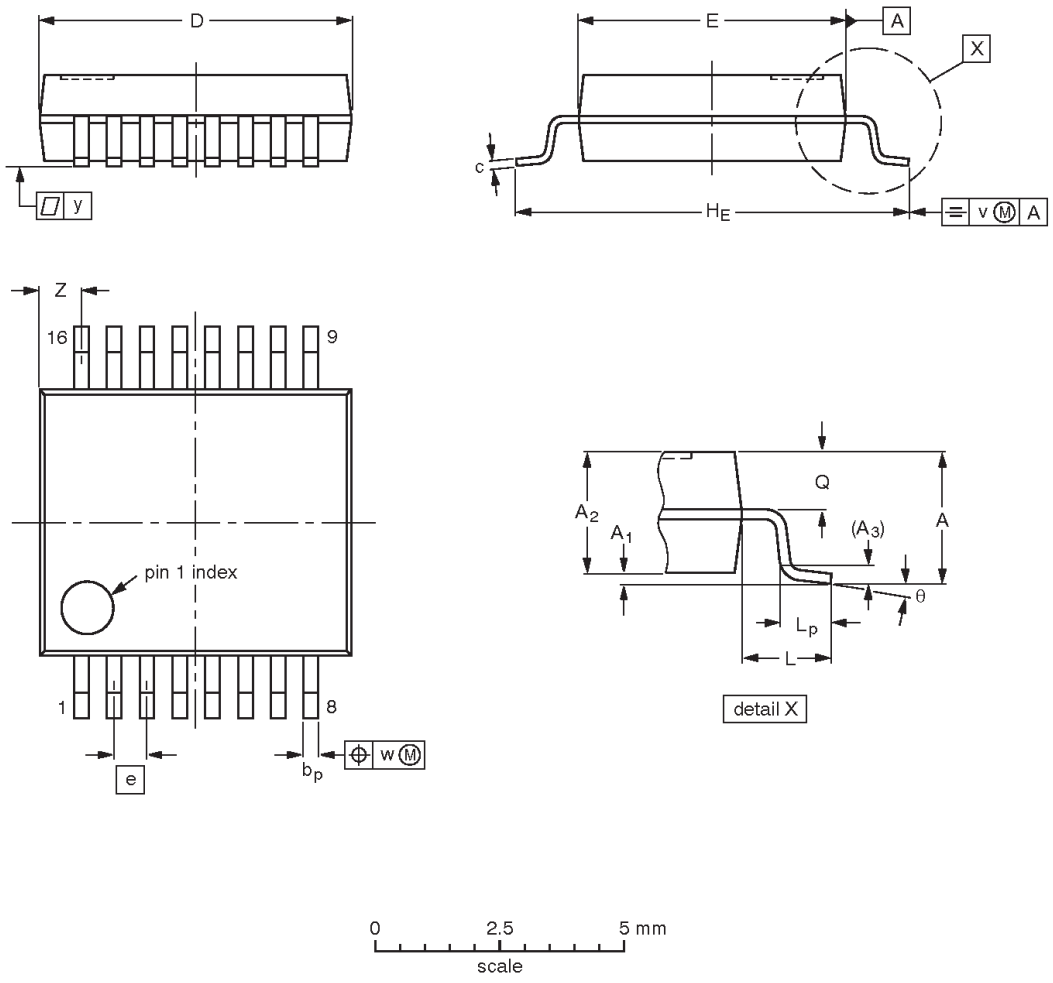
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

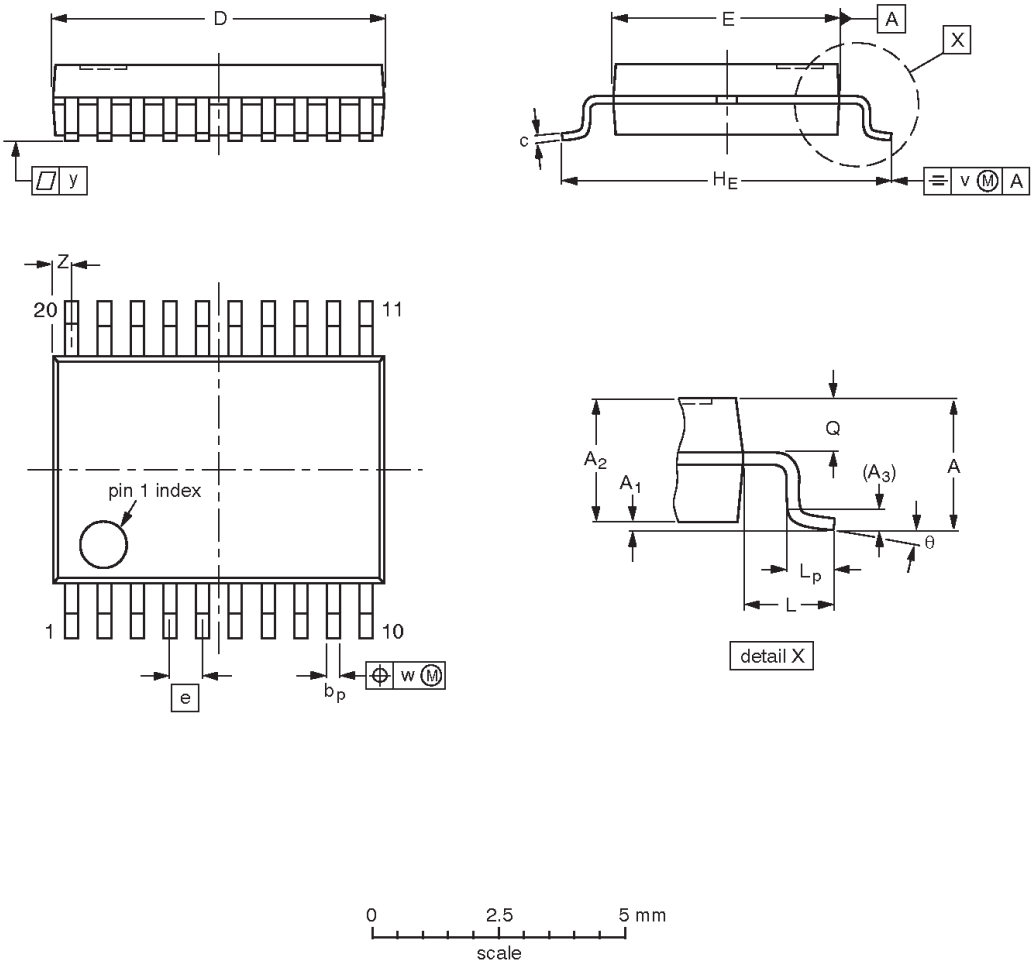
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

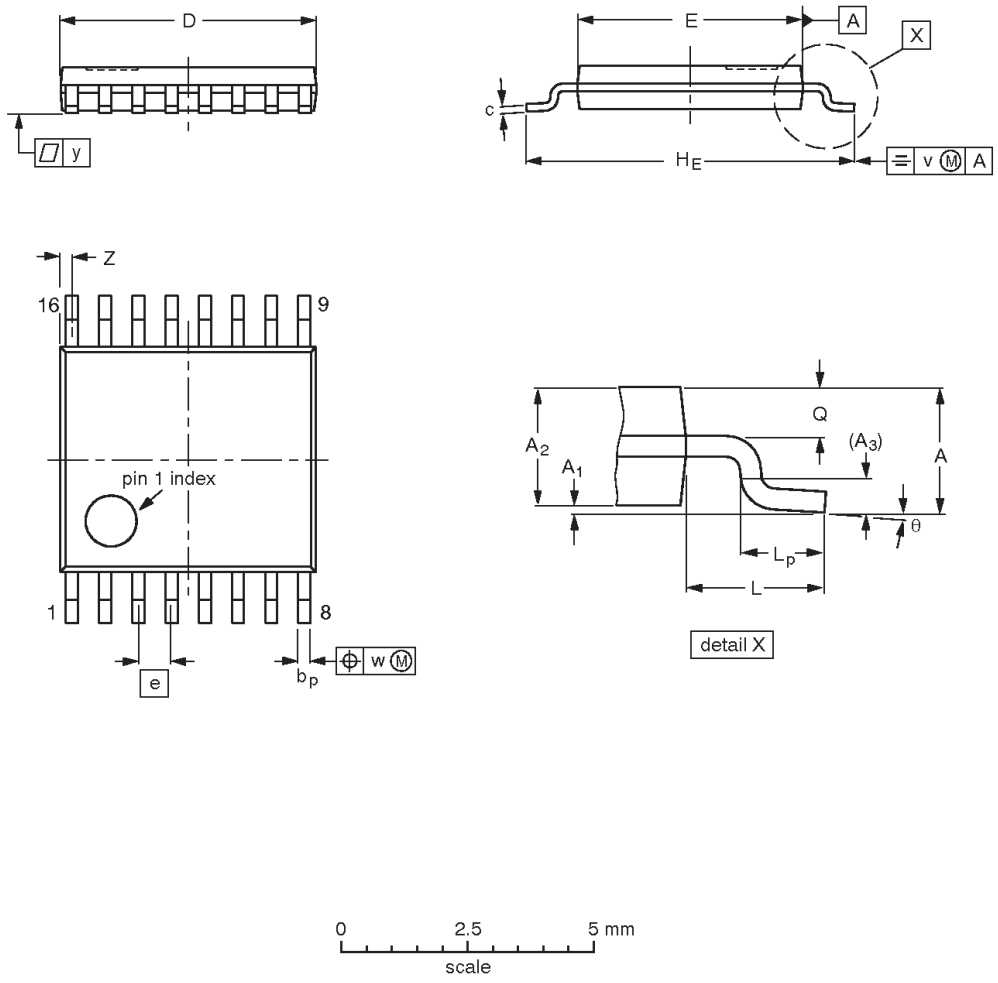
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT266-1		MO-152				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

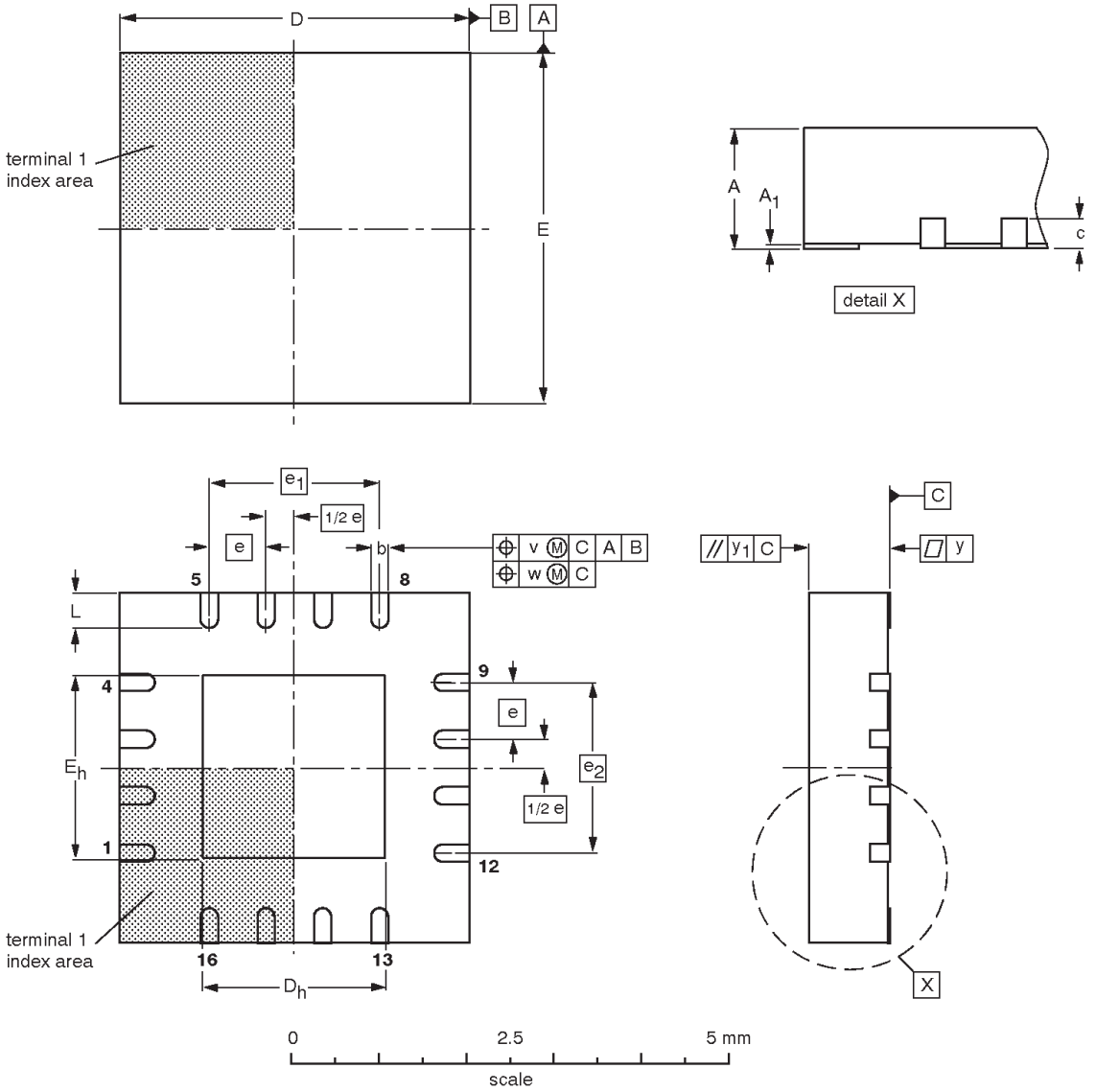
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_6	20040930	**Product data (9397 750 13289). Supersedes data of 2002 Jul 26 (9397 750 10163).** Modifications: ● Add DIP16 and SSOP20 packages to Features, Ordering information, Pin configuration, Pin description, and package outline drawings. ● Section “Register 0—Input Port Register” on page 4: change default values to ‘XXXXXXXX’ and add second paragraph. ● “Power-on Reset” section on page 5 modified. ● Add new “Typical application” section on page 9. ● DC Characteristics table on page 11: – add (new) Note 1, and its reference at V_{POR}. – Note 2 re-written.
_5	20020726	**Product data (9397 750 10163). ECN 853-2243 28672 of 26 July 2002. Supersedes data of 2002 May 13 (9397 750 09817).**
_4	20020513	Product specification (9397 750 09817)
_3		Product specification (9397 750 08342)
_2		Product specification (9397 750 08209)
_1		Product specification (9397 750 08159)

8-bit I²C and SMBus I/O port with interrupt PCA9554/PCA9554A

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Level	Data sheet status [1]	Product status [2] [3]	Definitions
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