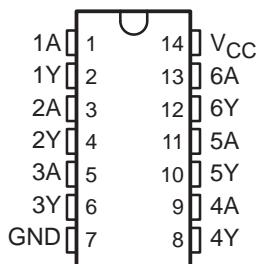


SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

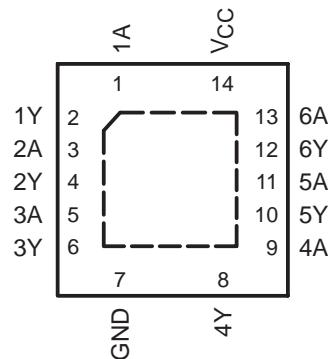
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- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max t_{pd} of 3.7 ns at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

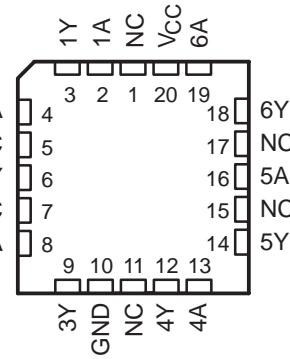
SN54LVC06A . . . J OR W PACKAGE
SN74LVC06A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC06A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC06A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These hex inverter buffers/drivers are designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the 'LVC06A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

TA	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC06ARGYR
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC06AD
		Reel of 2500	SN74LVC06ADR
		Reel of 250	SN74LVC06ADT
	SOP – NS	Reel of 2000	SN74LVC06ANSR
	SSOP – DB	Reel of 2000	SN74LVC06ADBR
	TSSOP – PW	Tube of 90	SN74LVC06APW
		Reel of 2000	SN74LVC06APWR
		Reel of 250	SN74LVC06APWT
-55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LVC06ADGVR
	CDIP – J	Tube of 25	SNJ54LVC06AJ
	CFP – W	Tube of 150	SNJ54LVC06AW
	LCCC – FK	Tube of 55	SNJ54LVC06AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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description/ordering information (continued)

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.
4. For the D package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
5. For the DB, DGV, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

recommended operating conditions (see Note 6)

			SN54LVC06A	UNIT		
			-55 TO 125°C			
			MIN	MAX		
V_{CC}	Supply voltage		Operating	1.65	3.6	V
			Data retention only	1.5		
V_{IH}	High-level input voltage		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
			V_{CC} = 2.3 V to 2.7 V	1.7		
			V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage		V_{CC} = 1.65 V to 1.95 V	0.35 × V_{CC}		V
			V_{CC} = 2.3 V to 2.7 V	0.7		
			V_{CC} = 2.7 V to 3.6 V	0.8		
V_I	Input voltage			0	5.5	V
V_O	Output voltage			0	5.5	V
I_{OL}	Low-level output current		V_{CC} = 1.65 V	4		mA
			V_{CC} = 2.3 V	8		
			V_{CC} = 2.7 V	12		
			V_{CC} = 3 V	24		

NOTE 6: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Note 6)

		SN74LVC06A						UNIT	
		T_A = 25°C		-40 TO 85°C		-40 TO 125°C			
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	1.65	3.6	1.65	3.6	1.65	3.6	V	
	Data retention only	1.5		1.5		1.5			
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	0.65 × V_{CC}	0.65 × V_{CC}			V	
		V_{CC} = 2.3 V to 2.7 V	1.7	1.7	1.7				
		V_{CC} = 2.7 V to 3.6 V	2	2	2				
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.35 × V_{CC}	0.35 × V_{CC}	0.35 × V_{CC}			V	
		V_{CC} = 2.3 V to 2.7 V	0.7	0.7	0.7				
		V_{CC} = 2.7 V to 3.6 V	0.8	0.8	0.8				
V_I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V_O	Output voltage	0	5.5	0	5.5	0	5.5	V	
I_{OL}	Low-level output current	V_{CC} = 1.65 V	4	4	4			mA	
		V_{CC} = 2.3 V	8	8	8				
		V_{CC} = 2.7 V	12	12	12				
		V_{CC} = 3 V	24	24	24				

NOTE 6: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**SN54LVC06A, SN74LVC06A
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC06A			UNIT	
			-55 TO 125°C				
			MIN	TYP	MAX		
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V		0.2		V	
	I _{OL} = 4 mA	1.65 V		0.45			
	I _{OL} = 8 mA	2.3 V		0.7			
	I _{OL} = 12 mA	2.7 V		0.4			
	I _{OL} = 24 mA	3 V		0.55			
I _I	V _I = 5.5 V or GND	3.6 V		±5	µA		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		10	µA		
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	µA		
C _i	V _I = V _{CC} or GND	3.3 V		5†	pF		

† T_A = 25°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC06A						UNIT	
			T _A = 25°C			-40 TO 85°C		-40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V		0.1	0.2		0.3			V
	I _{OL} = 4 mA	1.65 V		0.24	0.45		0.6			
	I _{OL} = 8 mA	2.3 V		0.3	0.7		0.75			
	I _{OL} = 12 mA	2.7 V		0.4	0.4		0.6			
	I _{OL} = 24 mA	3 V		0.55	0.55		0.8			
I _I	V _I = 5.5 V or GND	3.6 V		±1	±5		±20	µA		
I _{off}	V _I or V _O = 5.5 V	0		±1	±10		±20	µA		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		1	10		40	µA		
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	500		5000	µA		
C _i	V _I = V _{CC} or GND	3.3 V		5					pF	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC06A		UNIT	
				-55 TO 125°C			
				MIN	MAX		
t _{pd}	A	Y	1.8 V ± 0.15 V	1.4	5.6	ns	
				2.5 V ± 0.2 V	1		
				2.7 V	3.9		
				3.3 V ± 0.3 V	1		

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SN54LVC06A, SN74LVC06A
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC06A						UNIT	
				T _A = 25°C			-40 TO 85°C		-40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	1.4	3	5.1	1.4	5.6	1.4	7.6	ns
			2.5 V ± 0.2 V	1	1.9	2.8	1	3.1	1	4	
			2.7 V	1	2.4	3.7	1	3.9	1	5	
			3.3 V ± 0.3 V	1	2.2	3.5	1	3.7	1	5	

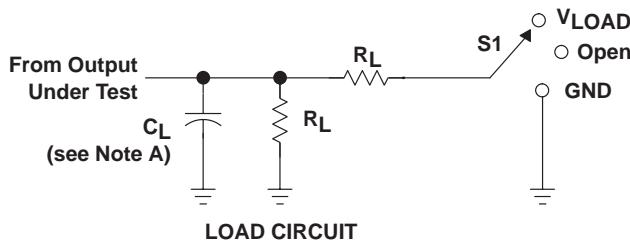
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT	
C _{pd} Power dissipation capacitance per buffer/driver			f = 10 MHz	1.8 V 2.5 V 3.3 V	2.1 2.3 2.5	pF

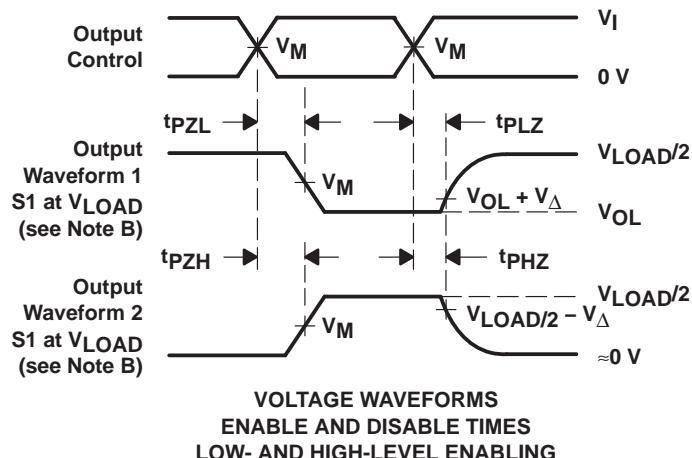
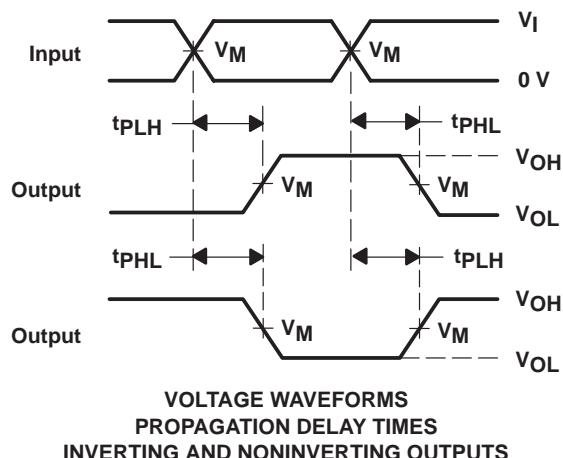
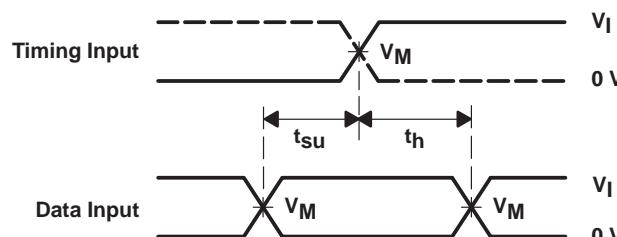
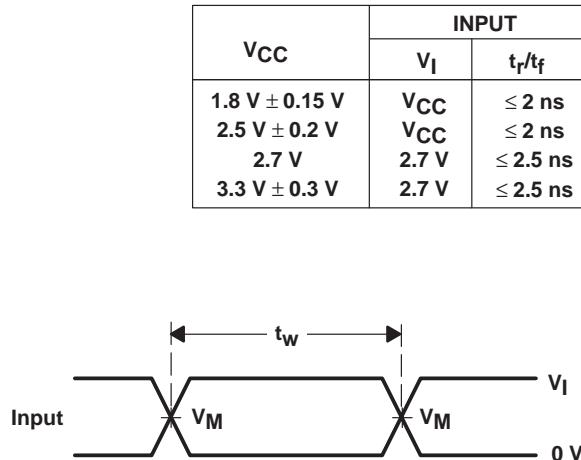
**SN54LVC06A, SN74LVC06A
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION
(OPEN DRAIN)**



TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- t_{PZL} is measured at V_M .
- t_{PLZ} is measured at $V_{OL} + V_\Delta$.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC06AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LVC06ADBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LVC06ADGVR	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC06ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LVC06ADT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LVC06ANSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LVC06APW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC06APWLE	OBsolete	TSSOP	PW	14		None	Call TI	Call TI
SN74LVC06APWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC06APWT	ACTIVE	TSSOP	PW	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC06ARGYR	ACTIVE	QFN	RGY	14	1000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

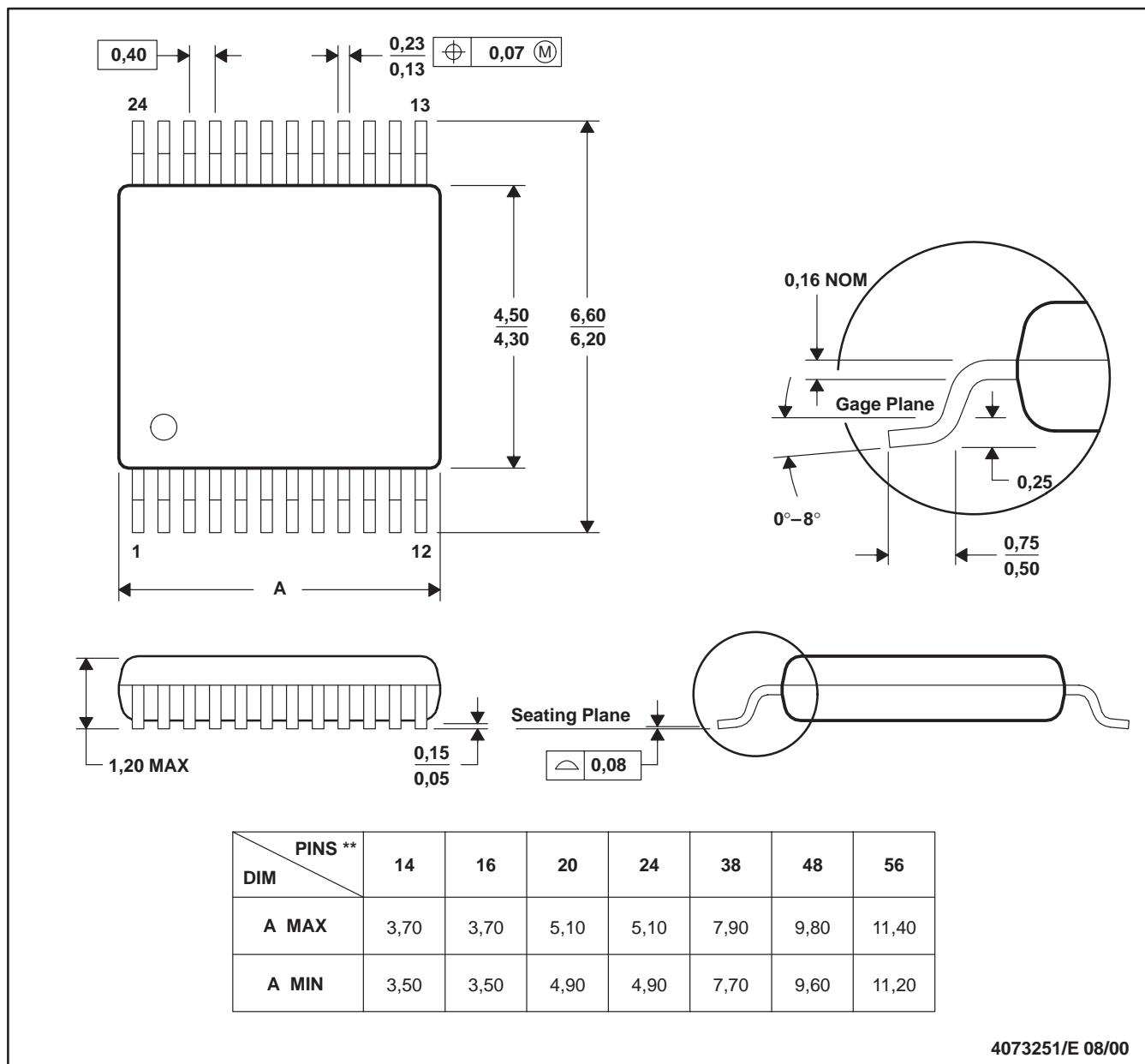
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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

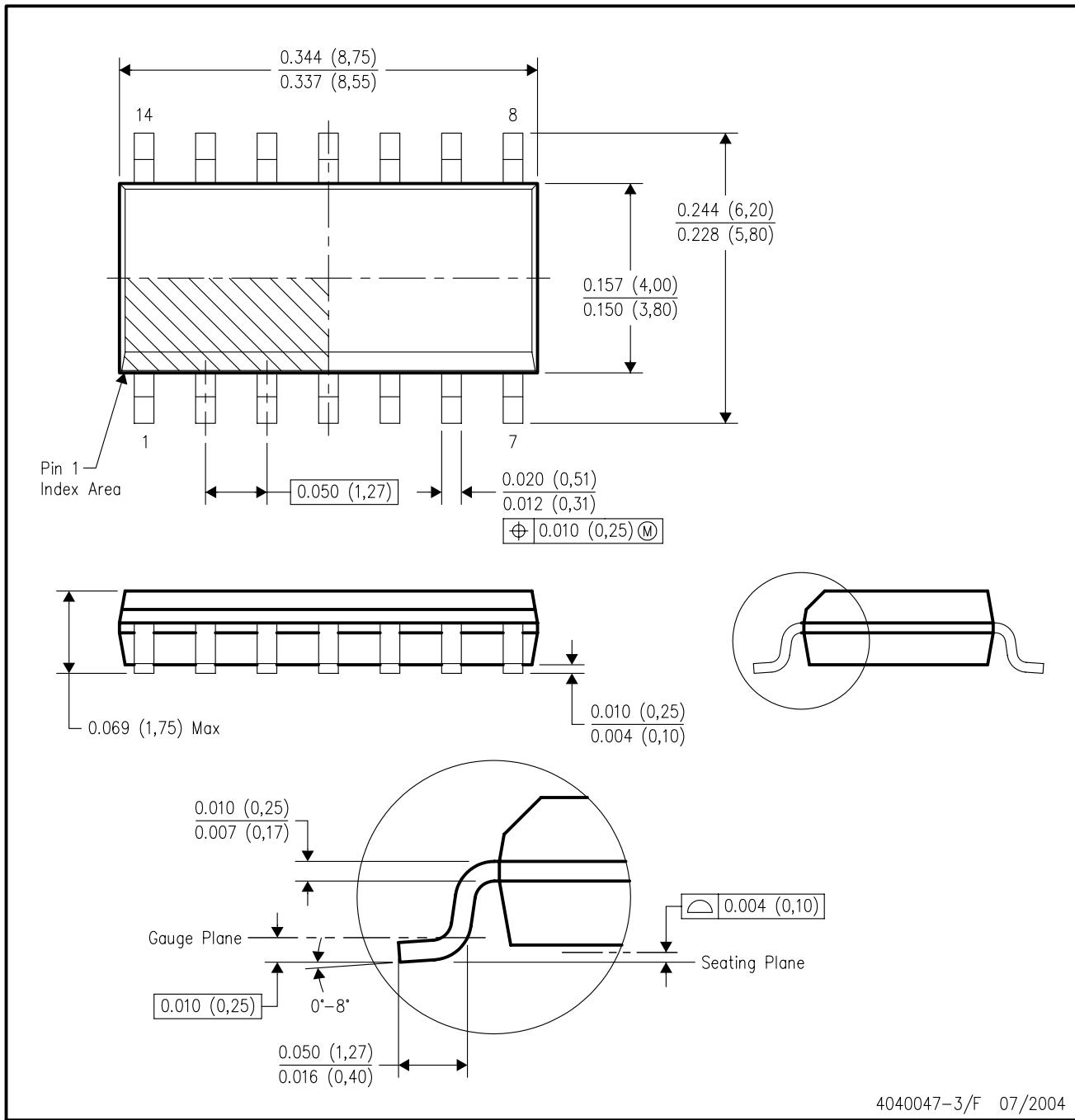
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

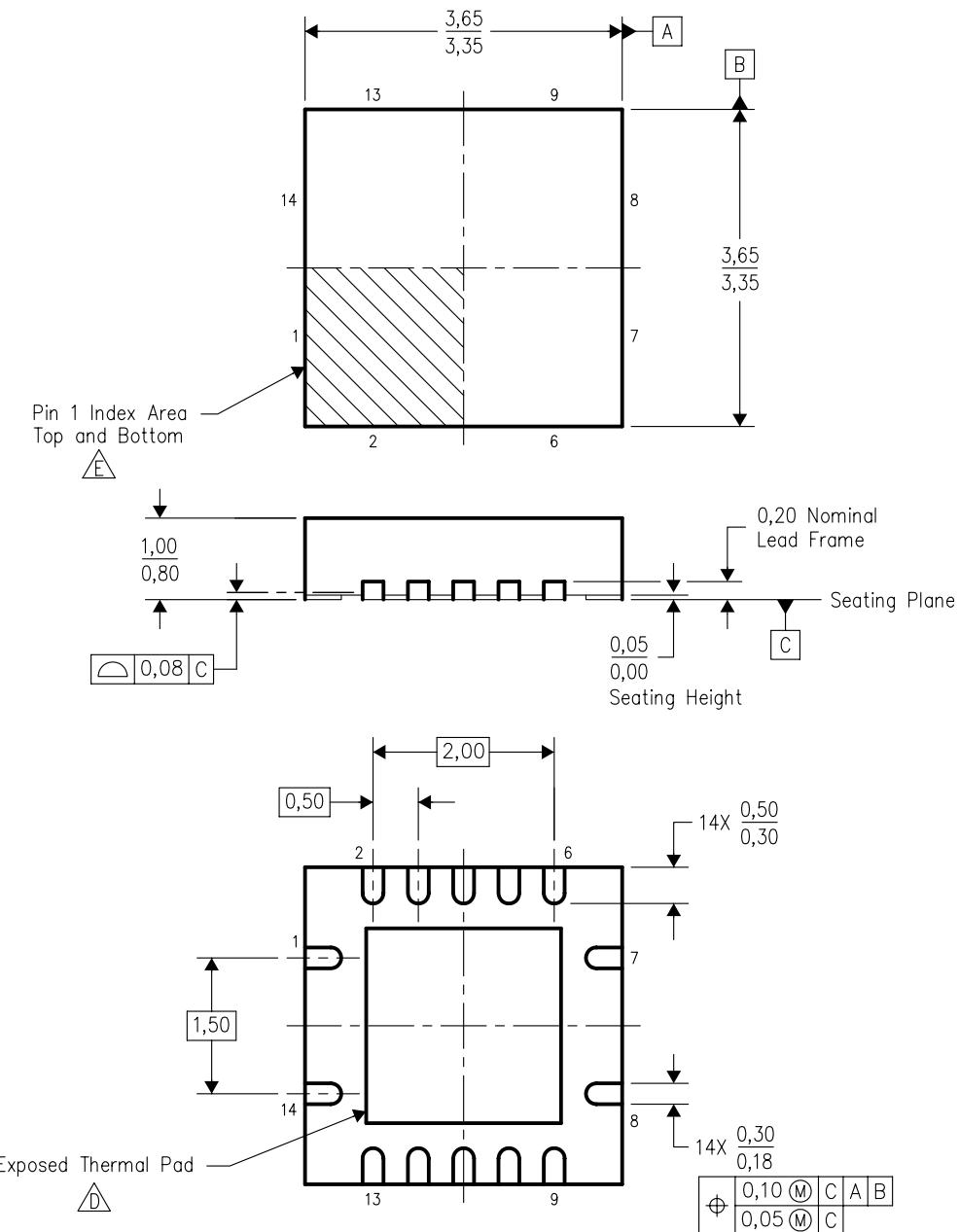


NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

4203539-2/F 02/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

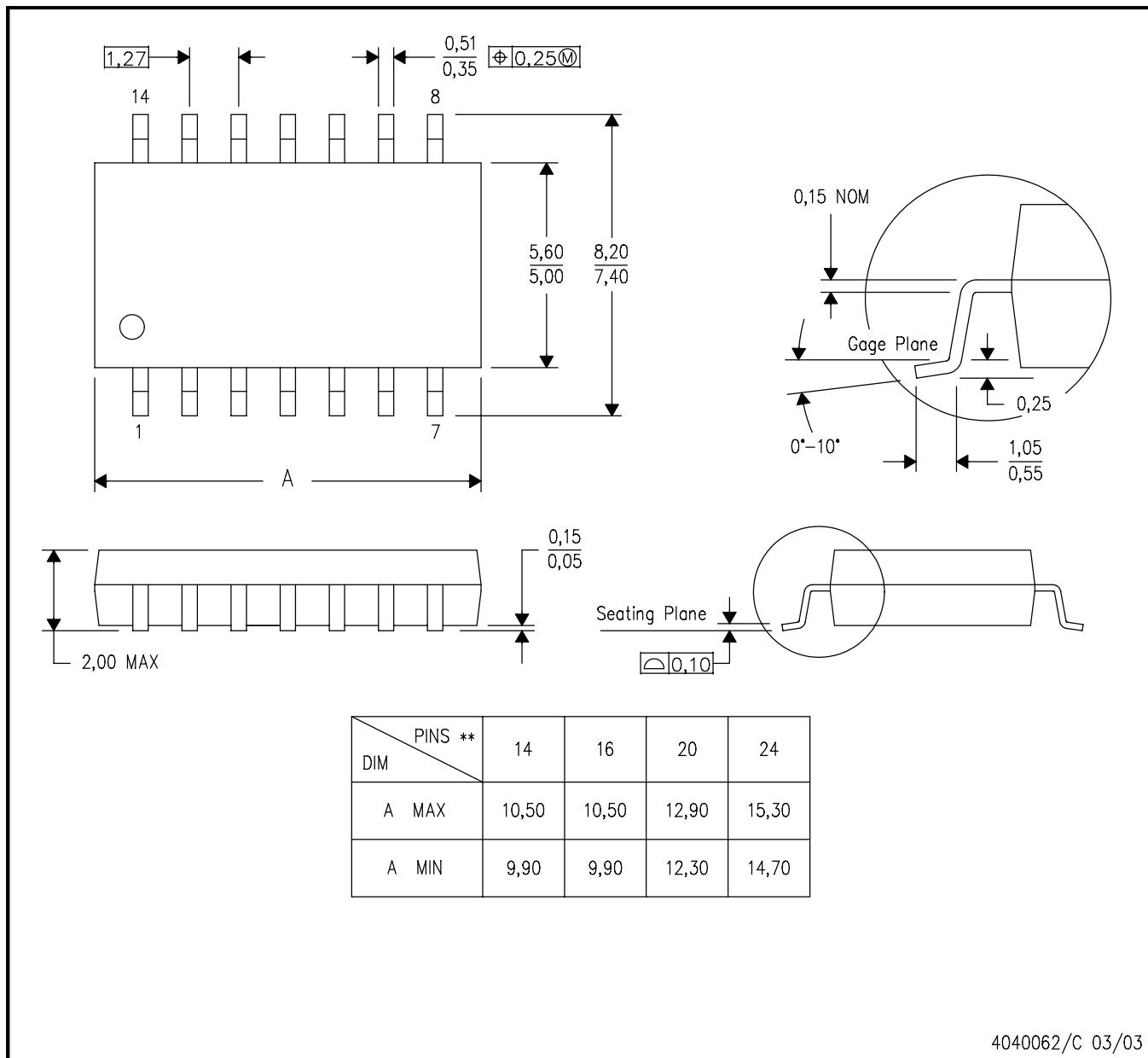
F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



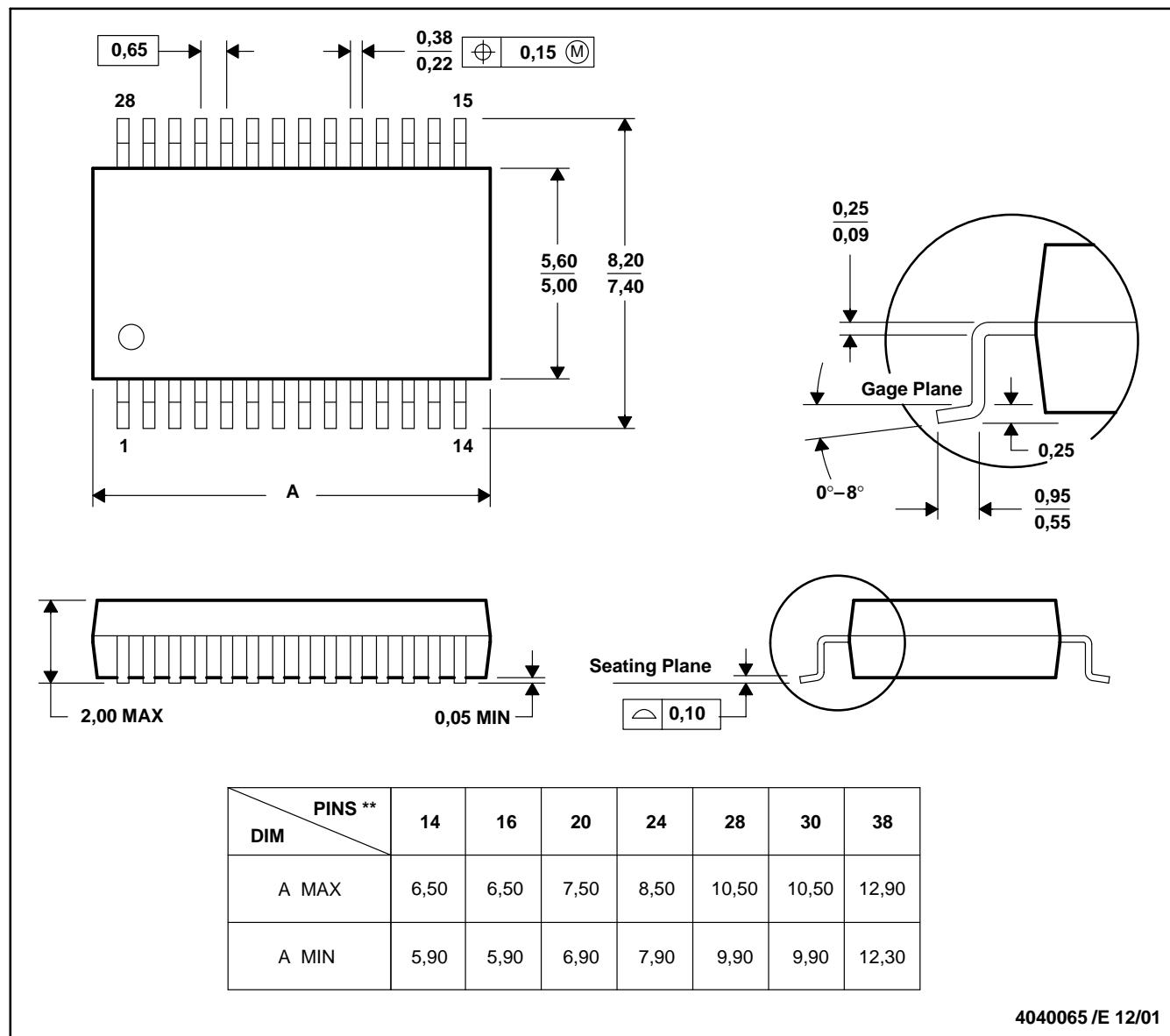
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
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DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

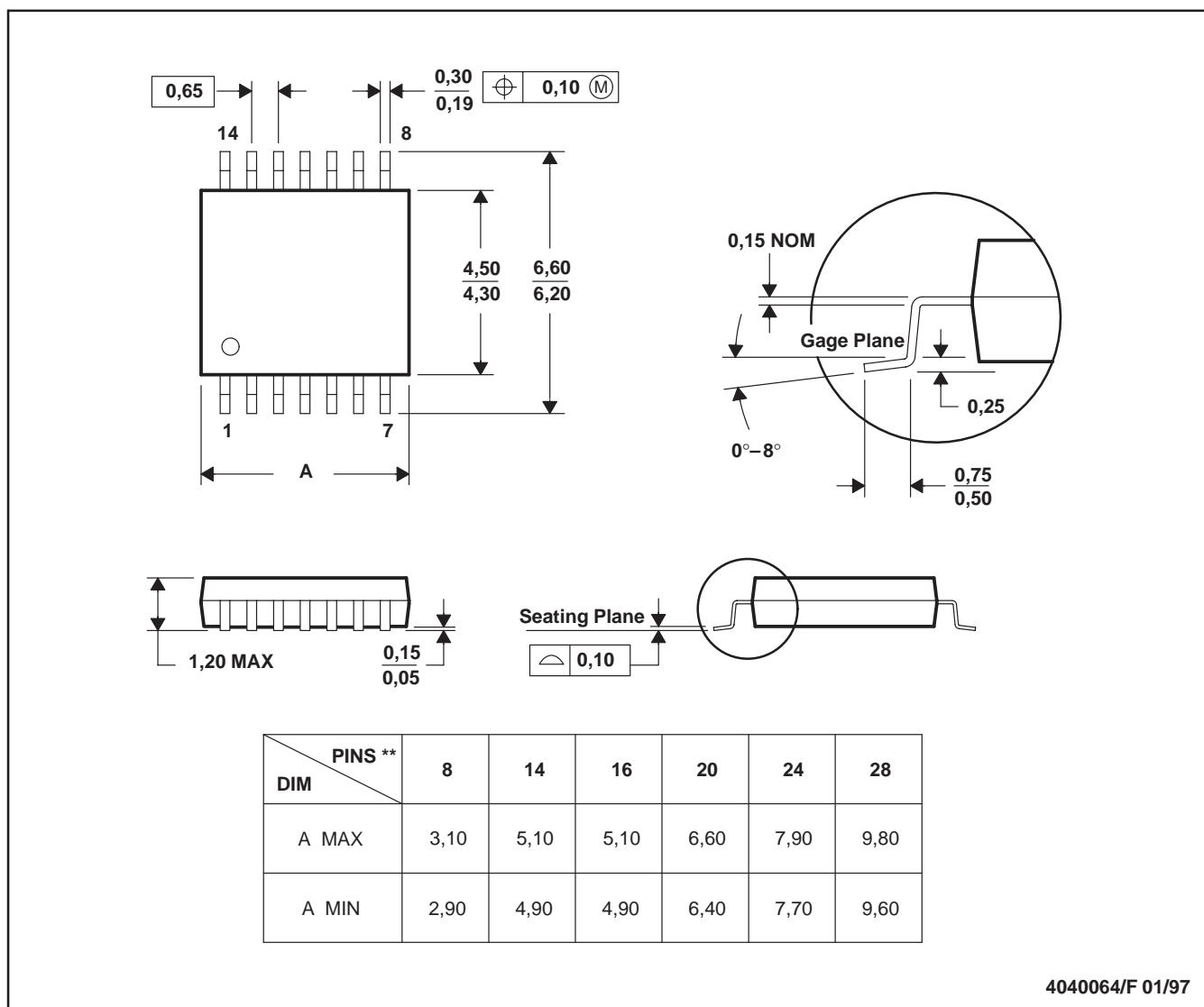


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

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