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February 2008

# 74LVT373, 74LVTH373 Low Voltage Octal Transparent Latch with 3-STATE Outputs

### **Features**

- Input and output interface capability to systems at 5V V<sub>CC</sub>
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH373), also available without bushold feature (74LVT373)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 373
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

### **General Description**

The LVT373 and LVTH373 consist of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent in the latches appear transparent in the latchestable (LE) is HIGH. When 'E is own to data satisfying the input timing requirement is atched bath appears on the bus very notice of the latent appears on the bus very notice of the latent appears of the laten

The LVT. '73 'ta in its include bushold, eliminating the adit ext pull-up resistors to hold unused but

The contractions are designed for low-voltage (3.3V) V<sub>CC</sub> applications but with the copability to provide a TTL interface to a 5V environment. The LVT373 and LVTH373 are fabricated with an advanced BiCMOS technology to achieve high space operation similar to 5V ABT while managining to vipower dissipation.

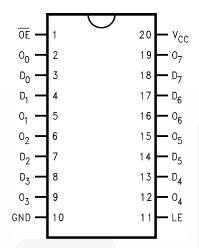
# Ordering Information

Order N mber	Jack-Je	Package Description			
7 _vic 3W.	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide			
, VT37, J	M29D	J-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide			
74L TO JMTC	MTC20	20-Lead 1 hin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide			
74LVTH?73WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide			
74LVT1373SJ	M207	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide			
74LVTH373MTC	.47 620	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide			

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

## **Connection Diagram**



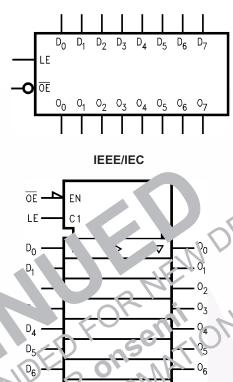
# **Pin Description**

Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
ŌĒ	Output Enable Input
O <sub>0</sub> –O <sub>7</sub>	3-STATE Latch O ,uts

# Functional Pascintion

The LVT373 a 4.1 and 373 contain eight D-type latches with 3-STz. E standard utputs. When the Latch Enable (LE) at it. HIC at a on the Dn inputs enters the ches. This position the latches are Lansparent, Do., a tch or but will change state each time its D input changes when LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

# **Logic Symbols**



### Truth Table

10 C	inputs	Outputs	
LE	ŌĒ	D <sub>n</sub>	O <sub>n</sub>
X	Н	Х	Z
Н	L	L	L
Н	L	Н	Н
L	L	Х	O <sub>0</sub>

H = HIGH Voltage Level

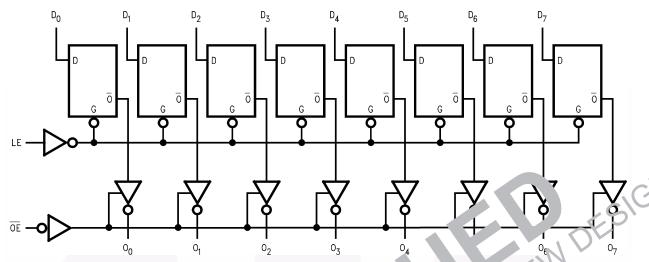
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

 ${\rm O_0} = {\rm Previous} \; {\rm O_0} \; {\rm before} \; {\rm HIGH\text{-}to\text{-}LOW} \; {\rm transition}$  of Latch Enable

# **Logic Diagram**



Please note that this diagram is provided only for the understanding of gic peratic and should not be used to estimate propagation delays.

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	-0.5V to +4.6V
VI	DC Input Voltage	-0.5V to +7.0V
Vo	DC Output Voltage	
	Output in 3-STATE	-0.5V to +7.0V
	Output in HIGH or LOW State <sup>(1)</sup>	-0.5V to +7.0V
I <sub>IK</sub>	DC Input Diode Current, V <sub>I</sub> < GND	-50mA
I <sub>OK</sub>	DC Output Diode Current, V <sub>O</sub> < GND	-50mA
Io	DC Output Current, V <sub>O</sub> > V <sub>CC</sub>	
	Output at HIGH State	64mA
	Output at LOW State	128mA
I <sub>cc</sub>	DC Supply Current per Supply Pin	±64mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±128mA
T <sub>STG</sub>	Storage Temperature	-65° C tc → 150° C

#### Note:

1. In Absolute Maximum Rating must be of a ved.

# Recommended Operation Corditions

The Recommended Oproving Conditions able defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend excretely a more signing to assolute maximum ratings.

Symb	Parantever	Min	Max	Units
	Sinal oltage	2.7	3.6	V
VI	nput Voltage	0	5.5	V
Тон	HIGH Level Output Current		-32	mA
JL	LOV/-Leve! Output Current		64	mA
T <sub>A</sub> Free-Air Operating 1 mperature		-40	85	°C
Δ+/ ΔV	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

### **DC Electrical Characteristics**

		T <sub>A</sub> =-40°C to +85°C				
Parameter	V <sub>CC</sub> (V)	Conditions	Min.	Typ. <sup>(2)</sup>	Max.	Units
Input Clamp Diode Voltage	2.7	I <sub>I</sub> = -18mA			-1.2	V
Input HIGH Voltage	2.7–3.6	$V_0 \le 0.1V$ or	2.0			V
Input LOW Voltage	2.7–3.6	$V_O \ge V_{CC} - 0.1V$			0.8	V
Output HIGH Voltage	2.7–3.6	$I_{OH} = -100 \mu A$	V <sub>CC</sub> -0.2			V
	2.7	$I_{OH} = -8mA$	2.4			
	3.0	$I_{OH} = -32mA$	2.0			
Output LOW Voltage	2.7	$I_{OL} = 100 \mu A$			0.2	V
		I <sub>OL</sub> = 24mA			0.5	
	3.0	I <sub>OL</sub> = 16mA			0.4	5
		$I_{OL} = 32mA$			0.5	
		I <sub>OL</sub> = 64mA			0.55	1
Bushold Input Minimum	3.0	V <sub>I</sub> = 0.8V	75		1	μA
Drive		V <sub>I</sub> = 2.0V	-75	190		
Bushold Input Over-Drive	3.0	(4)	500			μA
Current to Change State		Tr -	-50ú	3(1)		7
Input Current	3.6	\ -5.5V		5 1	10	μA
Control Pins	3.0	V <sub>I</sub> = V or V <sub>CC</sub>	0/	. 12	±1	
Data Pins		V <sub>I</sub> = 0V	2	5/4	<b>–</b> 5	
		$V_1 = V_{CC}$	10		1	
Power Off Leakage Irrent	U	$vV \le V_1 \text{ or } V_0 \le 5.5V$	71		±100	μA
Power up/ Jwn 3-STA	0-1.50	$V_0 = 0.5 \text{V to } 3.0 \text{V},$			±100	μA
STATE Och Hill akage	3.6	$V_0 = 0.5V$			<b>–</b> 5	μA
0.07475	(0)	144				
	3.6	V <sub>C</sub> = 3.0V			5	μA
	3.6	$V_{CC} < V_O \le 5.5V$			10	μA
Chirent	S. W.	100 10 = 3121				
Power Supply Current	3.6	Outputs HIGH			0.19	mA
Power Supply Cur ent	3.6	Outputs LOW			5	mA
Power Suprly Current	3.6	Outputs Disabled			0.19	mA
Power Surply Current	3.6	$V_{CC} \le V_O \le 5.5V$ ,			0.19	mA
		Outputs Disabled				
Increase in Power Supply	3.6	One Input at V <sub>CC</sub> – 0.6V,			0.2	mA
Current		Other Inputs at V <sub>CC</sub> or GND				
	Input Clamp Diode Voltage Input HIGH Voltage Input LOW Voltage Output HIGH Voltage  Output LOW Voltage  Output LOW Voltage  Bushold Input Minimum Drive  Bushold Input Over-Drive Current to Change State  Input Current  Control Pins Data Pins  Power Off Leakage urrent Power up own 3-STA Output C ent STATE Output Leakage Current  3-STATE Output Leakage Current Power Supply Current	Input Clamp Diode Voltage Input HIGH Voltage Input LOW Voltage Output HIGH Voltage  2.7–3.6  Output HIGH Voltage 2.7–3.6  2.7  3.0  Output LOW Voltage 2.7  3.0  Output LOW Voltage 2.7  3.0  Bushold Input Minimum Drive  Bushold Input Over-Drive Current to Change State  Input Current  Control Pins Data Pins  Power Up Own 3-STA Output C rent  STATE Output Leakage Trent  STATE Output Leakage Current  STATE Output Leakage Current  STATE Output Leakage Current  Power Supply Current 3.6  Power Supply Current 3.6  Power Supply Current 3.6  Power Supply Current 3.6  Increase in Power Supply 3.6  Increase in Power Supply 3.6	Input Clamp Diode Voltage	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Parameter   V <sub>CC</sub> (V)   Conditions   Min.   Typ. (2)   Max.

### Notes:

- 2. All typical values are at  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$ .
- 3. Applies to bushold versions only (74LVTH373).
- 4. An external driver must source at least the specified current to switch from LOW-to-HIGH.
- 5. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- 6. This is the increase in supply current for each input that is at the specified voltage level rather than  $V_{CC}$  or GND.

# Dynamic Switching Characteristics<sup>(7)</sup>

			Conditions T <sub>A</sub> = 25°C		2		
Symbol	Parameter	V <sub>CC</sub> (V)	$C_L = 50 pF, R_L = 500 \Omega$	Min.	Тур.	Max.	Units
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	(8)		0.8		V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	(8)		-0.8		V

### Notes:

- 7. Characterized in SOIC package. Guaranteed parameter, but not tested.
- 8. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

### **AC Electrical Characteristics**

			$T_A = -40$ °C + $C_L = 50$ °F, $R_L$	5L 2	N	0
		$V_{CC} = 3$	3.3V 0.3	√ <sub>CC</sub> =	2.71	
Symbol	Parameter	Min. 1	(9) Ma	Min.	Max.	Units
t <sub>PHL</sub>	Propagation Delay,	1.5	1.5	.5	5.0	าร
t <sub>PLH</sub>	$D_n$ to $O_n$		1.5	1.5	4.9	
t <sub>PHL</sub>	Propagation Delay,	1.7	4.5	1.7	4.9	ns
t <sub>PLH</sub>	LE to O <sub>n</sub>	1.7	4.52	1.7	5.0	
t <sub>PZL</sub>	Output Enable Tim	.3	4.8		5.9	ns
t <sub>PZH</sub>		1.3	4.8	1.3	5.5	
t <sub>PLZ</sub>	Output F Dakie Til	19	4.6	1.9	4.9	ns
t <sub>PHZ</sub>		1.9	4.6	1.9	4.9	
t <sub>W</sub>	LE Pulse Vid+1	3.0	60	3.0		ns
t <sub>S</sub>	cup me, D <sub>n</sub> to LE	1.1		1.0		ns
	i ime, D <sub>it</sub> to LE	1.4		1.4		ns

/ 'e:

9. Typi I values 2 e at  $V_{CC} = 3.3V$ ,  $T_A = 25.5$ 

# Capacitance<sup>(10)</sup>

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC} = OPEN, V_I = 0V \text{ or } V_{CC}$	3	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 3.0V$ , $V_{O} = 0V$ or $V_{CC}$	5	pF

### Note:

10. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

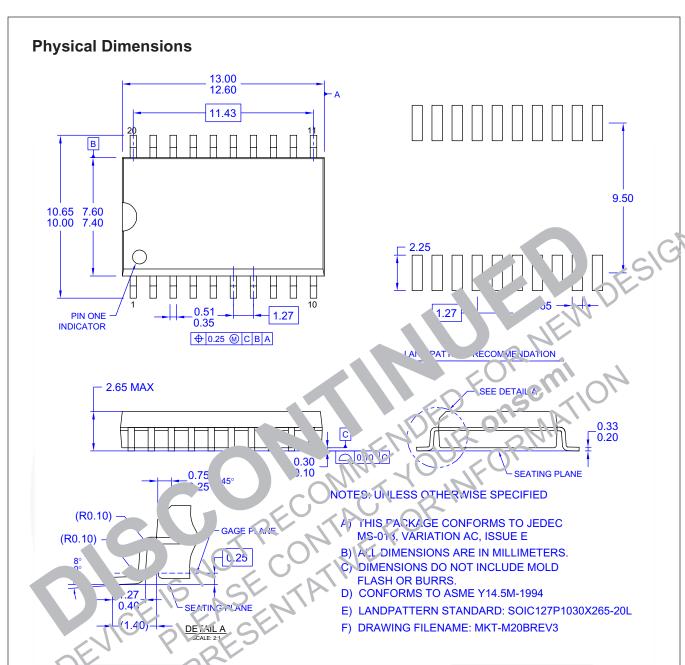


Figure 1. 20-Levi Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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# Physical Dimensions (Continued) 12.6±0.10 0.40 TYP -A-20 11 12 11 5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-3.9 (2.13)△ 0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT. J.6 TYP 1.27 ALL LEAD TIPS △ 0.1 C 2.1 MAX.--C-0.15 - 0.255.35-0.51 1.27 TYP 7° TYP ARE IN MILLIMATER GAGE PLANE 0°-8° TYP CONFORMS TO LIAU EDG-7320 REGISTRATION ESTABLISHED IN DECEMBER, 1998. D.Y.L.NSIONS ARE EXCLUSIVE OF TURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. $0.60\pm0.15$ SEATING PLANE 1.25 -DETAIL A

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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# Physical Dimensions (Continued) 5.5±0.1 -A--0.20 02ا 4.16 6,4 4.4±0.1 -B-3,2 0.2 C B A 0.65 ALL LEAD PIN #1 IDENT. O.1 C -0.90 1.2 -C-0.09-0.20 0.05 0.65 -12.00° GAGE PLANE 0.25 SEATING PLANE CONFORMS TO JEDEC RESISTRATION MIL-133 REF NOTE 6, DATE 7/33. VARIATION AC, -0.6±0.1-

DIMENSIONS ARE IN MILLIMETERS.

- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONS AND TO ERANCES PER ANSI Y14.5M, 1982.

R0.09min

DETAIL A

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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