16-CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The **NJU6631A** is a 1 Chip Dot Matrix LCD controller driver for up to 16-character 1-line or 8-character 2-line display.

It contains microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM and common and segment drivers.

The bleeder resistance generates for LCD Bias voltage internally.

The CR oscillator incorporates C and R, therefore no external components for oscillation are required.

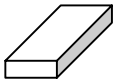
The microprocessor interface circuits which operate 2MHz frequency, can be connected directly to 4bit/8bit microprocessor.

The character generator consists of 9,600 bits ROM and 32 x 5 bits RAM. The standard version ROM is coded with 192 characters including capital and small letter fonts.

The 16-common and 40-segment drives up to 16-character 1-line LCD panels which divided two common electrode blocks.

The rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE



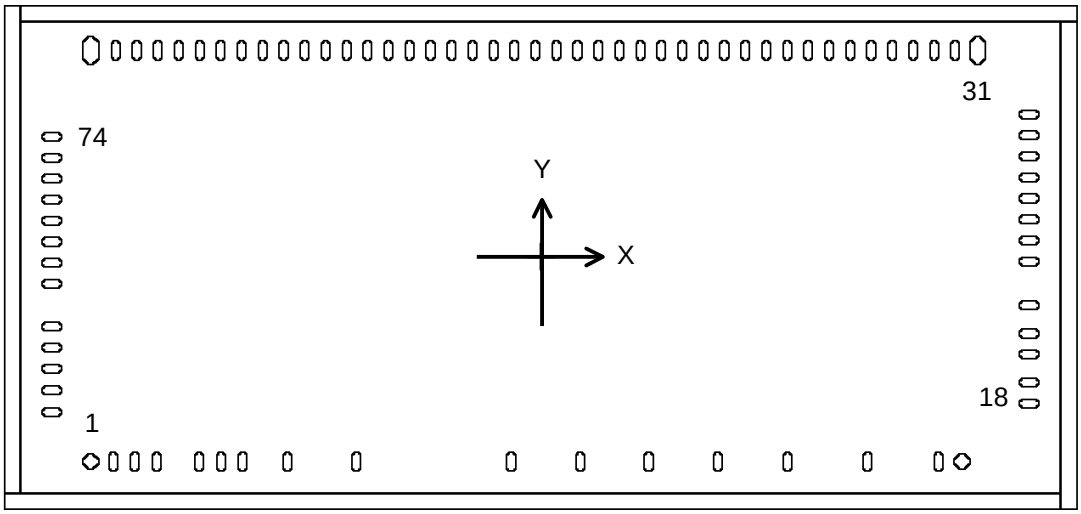
NJU6631ACH

■ FEATURES

- 16-character 1-line Dot Matrix LCD Controller Driver
- 4/8 Bit Microprocessor Direct Interface
- Display Data RAM - 16 x 8 bits : Maximum 16-character 1-line Display
- Character Generator ROM - 9,600 bits : 240 Characters for 5 x 8 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 8 Dots)
- Microprocessor can access to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver : 16-common / 40-segment
- Duty Ratio : 1/16 Duty
- Number of Maximum Display Characters : 16-character
- Useful Instruction Set
  Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift,
- Common and Segment driver Location order Select Function(Pin configuration mode A / mode B)
- Power On Initialize / Hardware Reset Function
- Bleeder Resistance On-chip
- Oscillation Circuit On-chip
- Low Power Consumption
- Operating Voltage --- +5V
- Package Outline --- Bumped Chip
- C-MOS Technology

31.Mar,2000
Ver.1

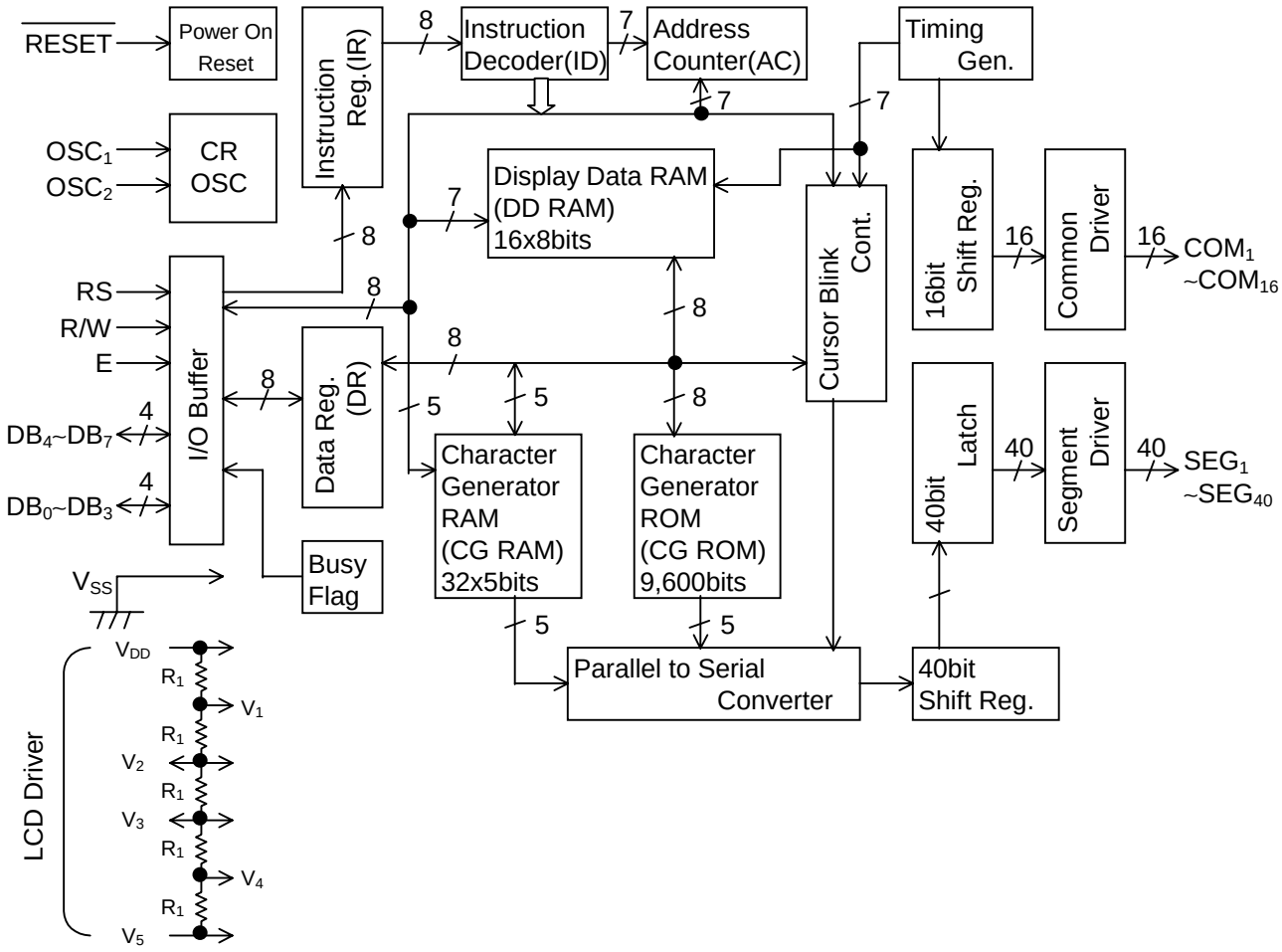
■ PAD LOCATION



Chip Size : 3.58mm x 1.68mm
Chip Center : X=0um, Y=0um
Bump Material : Au

Bump Size : 90um x 55um
Bump Height : 17.5um TYP.

■ BLOCK DIAGRAM



■ PAD COORDINATES

Chip Size 3.58 × 1.68mm(Chip Center X=0um,Y=0um)

PAD No.	PAD Name Pin Configuration Mode A	PAD Name Pin Configuration Mode B	Center X=(um)	Center Y=(um)	PAD No.	PAD Name Pin Configuration Mode A	PAD Name Pin Configuration Mode B	Center X=(um)	Center Y=(um)
1	Dummy1	Dummy1	-1501	-680	44	SEG_{12}	SEG_{29}	543	690
2	V_{DD}	V_{DD}	-1426	-680	45	SEG_{13}	SEG_{28}	473	690
3	V_{DD}	V_{DD}	-1353	-680	46	SEG_{14}	SEG_{27}	403	690
4	V_{DD}	V_{DD}	-1281	-680	47	SEG_{15}	SEG_{26}	333	690
5	V_5	V_5	-1138	-680	48	SEG_{16}	SEG_{25}	263	690
6	V_5	V_5	-1066	-680	49	SEG_{17}	SEG_{24}	193	690
7	V_5	V_5	-993	-680	50	SEG_{18}	SEG_{23}	123	690
8	V_3	V_3	-844	-680	51	SEG_{19}	SEG_{22}	53	690
9	V_2	V_2	-614	-680	52	SEG_{20}	SEG_{21}	-17	690
10	$\overline{RESET}$	$\overline{RESET}$	-98	-680	53	SEG_{21}	SEG_{20}	-87	690
11	RS	RS	132	-680	54	SEG_{22}	SEG_{19}	-157	690
12	R/W	R/W	361	-680	55	SEG_{23}	SEG_{18}	-227	690
13	E	E	591	-680	56	SEG_{24}	SEG_{17}	-297	690
14	DB_0	DB_0	824	-680	57	SEG_{25}	SEG_{16}	-367	690
15	DB_1	DB_1	1091	-680	58	SEG_{26}	SEG_{15}	-437	690
16	DB_2	DB_2	1328	-680	59	SEG_{27}	SEG_{14}	-507	690
17	Dummy2	Dummy2	1406	-680	60	SEG_{28}	SEG_{13}	-577	690
18	DB_3	DB_3	1630	-486	61	SEG_{29}	SEG_{12}	-647	690
19	DB_4	DB_4	1630	-416	62	SEG_{30}	SEG_{11}	-717	690
20	DB_5	DB_5	1630	-322	63	SEG_{31}	SEG_{10}	-787	690
21	DB_6	DB_6	1630	-253	64	SEG_{32}	SEG_9	-857	690
22	DB_7	DB_7	1630	-160	65	SEG_{33}	SEG_8	-927	690
23	COM_1	COM_9	1630	-13	66	SEG_{34}	SEG_7	-997	690
24	COM_2	COM_{10}	1630	57	67	SEG_{35}	SEG_6	-1067	690
25	COM_3	COM_{11}	1630	127	68	SEG_{36}	SEG_5	-1137	690
26	COM_4	COM_{12}	1630	197	69	SEG_{37}	SEG_4	-1207	690
27	COM_5	COM_{13}	1630	267	70	SEG_{38}	SEG_3	-1277	690
28	COM_6	COM_{14}	1630	337	71	SEG_{39}	SEG_2	-1347	690
29	COM_7	COM_{15}	1630	407	72	SEG_{40}	SEG_1	-1417	690
30	COM_8	COM_{16}	1630	477	73	Dummy5	Dummy5	-1501	690
31	Dummy3	Dummy3	1459	690	74	COM_{16}	COM_8	-1630	402
32	Dummy4	Dummy4	1383	690	75	COM_{15}	COM_7	-1630	332
33	SEG_1	SEG_{40}	1313	690	76	COM_{14}	COM_6	-1630	262
34	SEG_2	SEG_{39}	1243	690	77	COM_{13}	COM_5	-1630	192
35	SEG_3	SEG_{38}	1173	690	78	COM_{12}	COM_4	-1630	122
36	SEG_4	SEG_{37}	1103	690	79	COM_{11}	COM_3	-1630	52
37	SEG_5	SEG_{36}	1033	690	80	COM_{10}	COM_2	-1630	-18
38	SEG_6	SEG_{35}	963	690	81	COM_9	COM_1	-1630	-88
39	SEG_7	SEG_{34}	893	690	82	OSC_1	OSC_1	-1630	-230
40	SEG_8	SEG_{33}	823	690	83	OSC_2	OSC_2	-1630	-300
41	SEG_9	SEG_{32}	753	690	84	V_{SS}	V_{SS}	-1630	-370
42	SEG_{10}	SEG_{31}	683	690	85	V_{SS}	V_{SS}	-1630	-443
43	SEG_{11}	SEG_{30}	613	690	86	V_{SS}	V_{SS}	-1630	-515

Note) Dummy1~ Dummy5 are Dummy Pad.

■ TERMINAL DESCRIPTION

PAD No.		SYMBOL	FUNCTION
Pin Configuration			
Mode A	Mode B		
2,3,4	2,3,4	V_{DD}	Power Source (+5V)
84,85,86	84,85,86	V_{SS}	Power Source (0V)
9,8, 7,6,5	9,8, 7,6,5	V_2,V_3, V_5	LCD Driving Power Source
82 83	82 83	OSC_1 OSC_2	Oscillation Frequency Adjust Terminals. Normally Open. (Oscillation C and R are incorporated, OSC Freq.=270kHz) For external clock operation, the clock should be input on OSC1.
11	11	RS	Register selection signal input "0" : Instruction Register (Writing) Busy Flag (Reading) "1" : Data Register (Writing/Reading)
12	12	R/W	Read/Write selection signal input "0" : Write, "1" : Read
13	13	E	Read/Write activation signal input
22~19	22~19	DB_7~DB_4	3-state Data Bus (Upper) to transfer the data between MPU and NJU6631A DB_7 is also used for the Busy flag reading.
18~14	18~14	DB_3~DB_0	3-state Data Bus (Lower) to transfer the data between MPU and NJU6631A These bus are not used in the 4-bit operation.
23~30 81~74	81~74 23~30	COM_1~COM_8 COM_9~COM_{16}	LCD Common driving signal Terminals Common driver Location order Select as Shown in Table 4. Pin configuration mode A : M0=0 / mode B : M0=1.
33~72	72~33	SEG_1~SEG_{40}	LCD Segment driving signal Terminals Segment driver Location order Select as Shown in Table 4. Pin configuration mode A : M0=0 / mode B : M0=1.
10	10	$\overline{RESET}$	Reset Terminal. When the "L" level input over than 1.2ms to this terminal the system will be reset. (f_{OSC}=270kHz)

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Register

The **NJU6631A** incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR).

The Register (IR) stores instruction codes such as “Clear Display” and “Return Home”, and address data for Display Data RAM (DD RAM) and Character Generator RAM (CG RAM). The MPU can write the instruction code and address data to the Register (IR), but it cannot read out from the Register (IR).

The Register (DR) is a temporary stored register, the data stored in the Register (DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register (DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.

When the address data for the DD RAM or CG RAM is written into the Register (IR), the addressed data in the DD RAM or CG RAM is transferred to the Register (DR). By the MPU read out the data in the Register (DR), the data transmitting process is performed completely.

After reading the data in the Register (DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register (DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below :

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag (DB_7) and address counter (DB_0~DB_6)
1	0	DR	Write (DR to DD RAM or CG RAM)
1	1		Read (DD RAM or CG RAM to DR)

(1-2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in table 1.

The next instruction should be written after busy flag (BF) goes to "0".

(1-3) Address Counter (AC)

The address Counter (AC) addressing the DD RAM and CG RAM.

When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to counter (AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

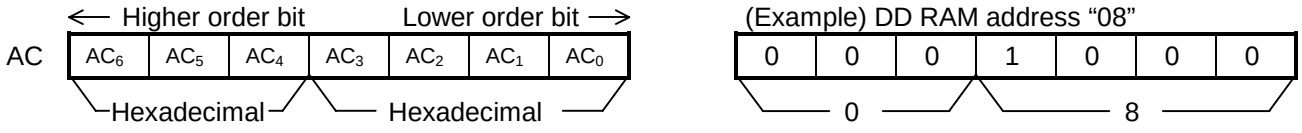
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.

The address data in the Counter (AC) is output from DB_6~DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1-4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 16 x 8 bits, stores up to 16-character display data represented in 8-bit code.

The DD RAM address data set in the address Counter (AC) is represented in Hexadecimal.



(1-4-1) 16-character 1-line Display

The **NJU6631A** has two kinds of addressing mode called "Addressing mode 1" and "Addressing mode 2" which is determined by the Function Set Instruction (A= 0 and 1).

"Addressing mode 1" is using consecutive address of $(00)_H$ through $(0F)_H$ for front half 8-character and last half 8-character. "Addressing mode 2" is not using consecutive address likes as $(00)_H$ through $(07)_H$ and $(40)_H$ through $(47)_H$ for front half 8-character and last half 8-character respectively.

16-character 1-line and 8 character 2-line are also determined by the Function Set Instruction (M1= 0 and 1).

<Addressing mode 1: A=0, M1=0>

-The relation between DD RAM address and display position on the LCD is shown below.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display position
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM address (Hexadecimal)
COM_1~COM_8								COM_9~COM_{16}								

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00	

(Right Shift Display)

0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→(0F)

<Addressing mode 2: A=1, M1=0>

-The relation between DD RAM address and display position on the LCD is shown below.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display position
00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47	←DD RAM address (Hexadecimal)
COM_1~COM_8								COM_9~COM_{16}								

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47	00	

(Right Shift Display)

47	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	→(47)

(1-4-2) 8-character 2-line

<Addressing mode 1: A=0, M1=1>

-The relation between DD RAM address and display position on the LCD is shown below.

	1	2	3	4	5	6	7	8	←Display Position
	COM_1~COM_8								
1st Line	00	01	02	03	04	05	06	07	←DD RAM Address
2nd Line	08	09	0A	0B	0C	0D	0E	0F	←
	COM_9~COM_{16}								(Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:

(Left Display Shift)

1st Line(00)←	01	02	03	04	05	06	07	08
2nd Line(08)←	09	0A	0B	0C	0D	0E	0F	00

(Right Display Shift)

1st Line	0F	00	01	02	03	04	05	06	→(07)
2nd Line	07	08	09	0A	0B	0C	0D	0E	→(0F)

<Addressing mode 2: A=1, M1=1>

-The relation between DD RAM address and display position on the LCD is shown below.

	1	2	3	4	5	6	7	8	← Display Position
	COM_1~COM_8								
1st Line	00	01	02	03	04	05	06	07	←DD RAM Address
2nd Line	40	41	42	43	44	45	46	47	←
	COM_9~COM_{16}								(Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:

(Left Display Shift)

1st Line(00)←	01	02	03	04	05	06	07	08
2nd Line(40)←	41	42	43	44	45	46	47	00

(Right Display Shift)

1st Line	47	00	01	02	03	04	05	06	→(07)
2nd Line	07	40	41	42	43	44	45	46	→(47)

(1-5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 8 dots character pattern represented in 8-bit character codes.

The storage capacity is up to 240 kinds of 5 x 8 dots character pattern. The correspondence between character code and standard character pattern of NJU6631A is shown in Table 2.

User-defined character pattern (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version -02)

Lower 4bit (Hexadecimal) \ Upper 4bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

(1-6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kinds of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 4 kinds of character in 5 x 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ ~ $(03)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. shows the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 7 dots).

Character Code (DD RAM Data)	CG RAM Address	Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0	4 3 2 1 0	4 3 2 1 0	
← Upper bit Lower bit →	← Upper bit Lower bit →	← Upper bit Lower bit →	
0 0 0 0 * * 0 0	0 0 0 0 0	1 1 1 1 0	
	0 0 1	1 0 0 0 1	
	0 1 0	1 0 0 0 1	
	0 1 1	1 1 1 1 0	
	1 0 0	1 0 1 0 0	Character Pattern Example (1)
	1 0 1	1 0 0 1 0	
	1 1 0	1 0 0 0 1	
	1 1 1	0 0 0 0 0	←Cursor Position
0 0 0 0 * * 0 1	0 1 0 0 0	1 0 0 0 1	
	0 0 1	0 1 0 1 0	
	0 1 0	1 1 1 1 1	
	0 1 1	0 0 1 0 0	
	1 0 0	1 1 1 1 1	Character Pattern Example (2)
	1 0 1	0 0 1 0 0	
	1 1 0	0 0 1 0 0	
	1 1 1	0 0 0 0 0	←Cursor Position
	0 0 0		
	0 0 1		
			* : Don't Care
0 0 0 0 * * 1 1	1 1		
	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1		

Notes : 1.Character code bits 0 to 1 correspond to the CG RAM address 3 and 4 (2 bits : 4 patterns)

2.CG RAM address 0, 1 and 2 designate character pattern Line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.

3.Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above. The bits 5 to 7 of the CG RAM do not exist.

4.CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 to 1. Therefore, the address $(00)_H$, $(04)_H$, $(08)_H$ and $(0C)_H$, select the same character pattern as shown in Table 2 and Table 3.

5."1" for CG RAM data corresponds to display On and "0" to display Off.

(1-7) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-8) LCD Driver

LCD driver circuits consist of 16-common driver and 40-segment driver.

The 40 bits of character pattern data are shifted in the shift-register and latched when the 40 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1-9) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(04)_H$, a cursor position is shown as follows :

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	0	1	0	0

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display Position
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM Address (Hexadecimal)

Cursor Position

Note) The cursor or blinks appear when the address counter (AC) selects the CG RAM.
But the displayed the cursor and blink are meaningless.
If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

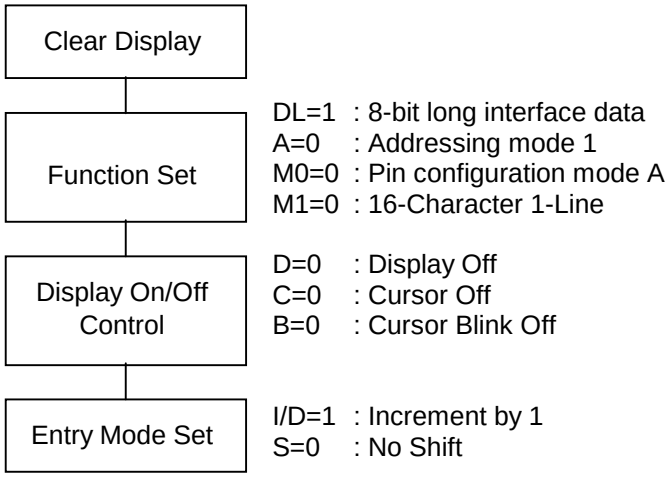
(2) Power on Initialization by internal circuits

(2-1) Initialization by Internal Reset circuits

The NJU6631A is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.

During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 4.5V.

Initialization flow is shown below :



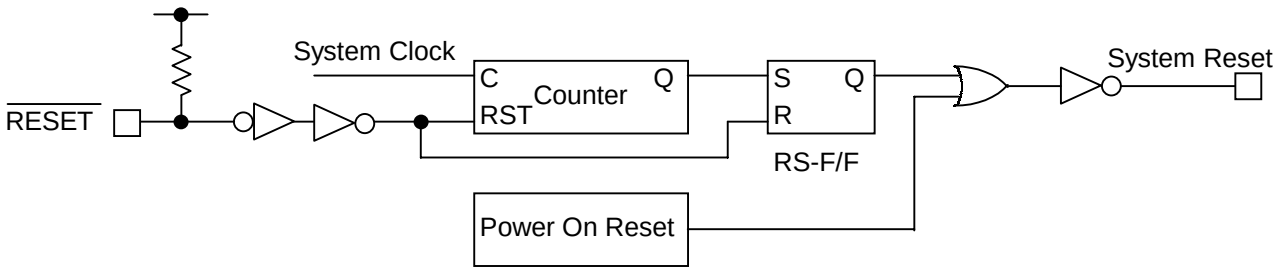
NOTE

If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operate and initialization will not be performed.
In this case the initialization by MPU software is required.

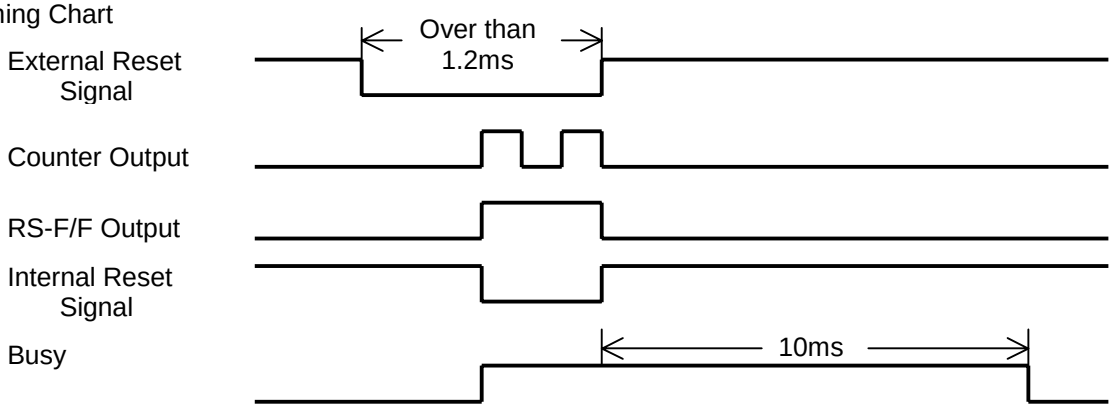
(2-2) Initialization by Hardware

The **NJU6631A** incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

- Reset Circuit



- Timing Chart



(3) Instruction

The **NJU6631A** incorporates two registers, an Instruction Register (IR) and a Data Register (DR).

These two registers store control information temporarily to allow interface between NJU6631A and MPU or peripheral ICs operating different cycles. The operation of NJU6631A is determined by this control signal from MPU.

The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).

Table 4. shows each instruction and its operating time.

Note) The execution time mentioned in Table 4. based on fcp or fosc=270kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

Instructions	Code										Description	Exec Time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Maker Test	0	0	0	0	0	0	0	0	0	0	All “0” code is using for maker testing.	-
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged.	37us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift.	37us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	37us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	56us
Function Set	0	0	0	0	1	DL	A	*	M1	M0	Sets interface data length(DL), Display address mode(A). DL=1 : 8 bits, DL=0 : 4 bits A=0 : Addressing mode 1 A=1 : Addressing mode 2 M1=0: 16-Character 1-Line M1=1: 8-Character 2-Line M0=0: Pin configuration mode A M0=1: Pin configuration mode B	37us
Set CG RAM address	0	0	0	1	*	A_{CG}					Sets CG RAM address. After this instruction, the data is transferred on CG RAM.	37us
Set DD RAM address	0	0	1	A_{DD}							Sets DD RAM address. After this instruction, the data is transferred on DD RAM.	37us
Read Busy Flag & Address	0	1	BF	AC_{DD}							Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
				*	*	AC_{CG}						
Write Data to CG or DD RAM	1	0	Write Data(DD RAM)								Writes data into CG or DD RAMs.	37us
			*	*	*	Write Data(CG RAM)						
Read Data to CG or DD RAM	1	1	Read Data(DD RAM)								Reads data from CG or DD RAMs.	56us
			*	*	*	Read Data(CG RAM)						
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM A_{CG} : CG RAM address, A_{DD} : DD RAM address, Corresponds to cursor address AC : Address counter used for both of DD and CG RAMs											

* = Don’t Care

(3-1) Description of each instructions

(a) Maker Test

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please pay attention the output condition of Enable signal when the power turns on.)
All "0" code in 8-bit length is usable for NOP (Not Operating instruction).

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment. If the cursor or blink are displayed, they are returned to the left end of the LCD.

The S of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	0	0	0	1	*	* = Don't Care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD, if the cursor or blink are on the display.

The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment : The address of the DD or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement : The address of the DD or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D : shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

(e)Display On/Off Control

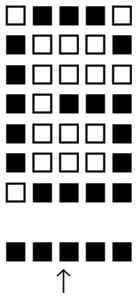
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

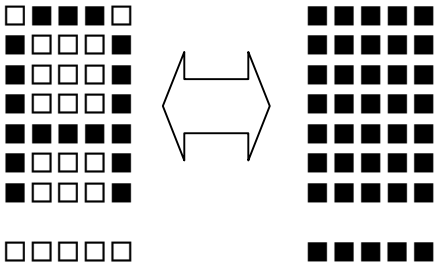
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 303.4ms at or f_{OSC}=270kHz. The blink is displayed alternatively with all on (it means all black) and characters display. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Cursor

Character Font 5 x 7 dots
(1) Cursor display example



Alternating display
(2) Blink display example

(f) Cursor / Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* = Don't Care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display.

The contents of address counter (AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left. ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right. ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	1	DL	A	*	M1	M0	* = Don't Care

Function set instruction which sets the interface data length, the addressing Mode for the DD RAM, 1-line or 2-line display, and Pin configuration mode, is executed when the code "1" is written into DB_5 and the codes of (DL), (A), (M1) and (M0) are written into DB_4(DL), DB_3(A), DB_1(M1) and DB_0(M0), as shown below (character font is fixed 5 x 7 dots).

(DL) sets the interface data length, (A) sets the DD RAM address mode $(00)_H$ through $(0F)_H$ or $(00)_H$ through $(07)_H$ and $(40)_H$ through $(47)_H$, (M1) sets the number of display line either the 1-line or 2-line display, and (M0) sets the Pin configuration for Common and Segment drivers as shown in coordinates.

NOTE

This function set instruction must be performed at the head of the program prior to all other existing instructions (except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length to 8 bits (DB_7 to DB_0).
0	Set the interface data length to 4 bits (DB_7 to DB_4). The data must be sent or received twice.

A	Function
0	Set the Addressing Mode 1 for the DD RAM.
1	Set the Addressing Mode 2 for the DD RAM.

M1	Function
0	Set the 16-Character 1-Line Display.
1	Set the 8-Character 2-Line Display.

M0	Function	
0	Set the Pin configuration mode A for Common and Segment Driver.	Refer to coordinates
1	Set the Pin configuration mode B for Common and Segment Driver.	

(h) Set CG RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	1	*	A	A	A	A	A	* = Don't Care
			← Higher order bit →			← Lower order bit →					

Set CG RAM address instruction is executed when the code "1" is written into DB_6 and the address is written into DB_4 to DB_0 as shown above.

The address data mentioned by binary code "AAAAA" is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM.

(i) Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
			← Higher order bit →			← Lower order bit →				

Set DD RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data mentioned by binary code "AAAAAAA" is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction, the data writing/reading is performed into/from the DD RAM.

Note : When the "Addressing mode 1" selection, $(00)_H$ through $(0F)_H$ are available but $(10)_H$ through $(7F)_H$ are ignored. When the "Addressing mode 2" selection, $(00)_H$ through $(07)_H$ and $(40)_H$ through $(47)_H$ are available but $(08)_H$ through $(3F)_H$ and $(48)_H$ through $(7F)_H$ are ignored.

(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher order bit →← Lower order bit →

This instruction reads out the internal status of the NJU6631A. When this instruction is executed, the busy flag (BF) which indicate internal operation is read out from DB_7 and the address of CG RAM or DD RAM is read out from DB_6 to DB_0 (the address for CG RAM or DD RAM is determined by the previous instruction).

(BF)=1 indicates that internal operation is in progress. The next instruction is inhibited when (BF)=1. Check the (BF) status before the next write operation.

(k) Write Data to CG or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	0	D	D	D	D	D	D	D	D	(DD RAM)

← Higher order bit →← Lower order bit →

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	0	*	*	*	D	D	D	D	D	(CG RAM)

← Higher order bit →← Lower order bit →

Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 5-bit data "DDDDD" are written into the CG RAM, and the binary 8-bit data "DDDDDDDD" are written into the DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

After this instruction execution, the address increment (+1) or decrement (-1) performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(l) Read Data from CG or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	1	D	D	D	D	D	D	D	D	(DD RAM)

← Higher order bit →← Lower order bit →

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	1	*	*	*	D	D	D	D	D	(CG RAM)

← Higher order bit →← Lower order bit →

Read Data from CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 5 bit data "DDDDD" are read out from CG RAM, and the binary 8 bit data "DDDDDDDD" are read out from DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

Note : The address counter(AC) is automatically incremented or decremented by 1 after write instructions to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(3-2) Initialization using the internal reset circuits

(a) 16-character 1-line in 8-bit operation Addressing Mode 1 (Using internal reset circuits).

At the 16-character 1-line display, the Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Power On											Initialized. No display appears.
↓											
Function Set	0	0	0	0	1	1	0	*	0	0	Set the 8-bit operation, 16-Character 1-line display, Pin configuration mode A, Addressing Mode 1.
↓											
Disp. On/Off Control	0	0	0	0	0	0	1	1	1	0	Turns on display and cursor. Entire display is in space mode by the initialization.
↓											
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data write to the DD or CG RAM.
↓											
Write data to the DD/CG RAM and set the Instruction											

(b) 8-character 2-line in 4-bit operation Addressing Mode 2 (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

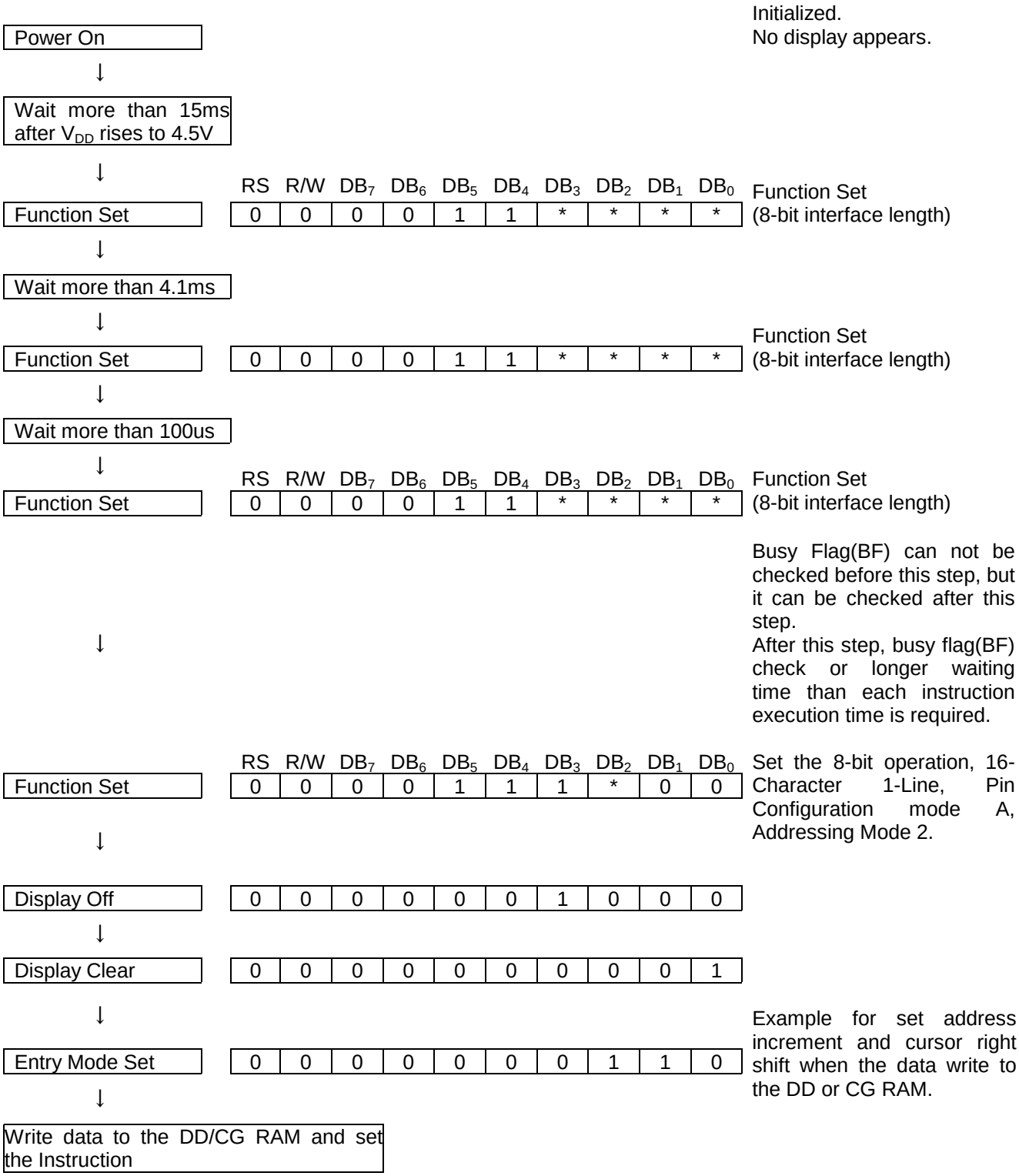
When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full. 8-character 2-line in 4-bit operation is shown as follows:

	RS	R/W	DB_7	DB_6	DB_5	DB_4	
Power On							Initialized. No display appears.
↓							
Function Set	0	0	0	0	1	0	Set the 4-bit operation. This step is executed in 8-bit mode set by the initialization.
↓							
Function Set	0 0	0 0	0 1	0 *	1 1	0 1	Set the 4-bit operation / 2-line 8-Character display / Pin configuration mode B / Addressing Mode 2. The 4-bitoperation starts from this step.
↓							
Disp. On/Off Control	0 0	0 0	0 1	0 1	0 1	0 0	Turn on display and cursor. Entire display is in space mode by the initialization.
↓							
Entry Mode Set	0 0	0 0	0 0	0 1	0 1	0 0	Example for set address increment and cursor right shift when the data write to the DD or CG RAM.
↓							
Write data to the DD/CG RAM and set the Instruction							

(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6631A must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface



(b) Initialization by Instruction in 4-bit interface

	RS	R/W	DB_7	DB_6	DB_5	DB_4	
Power On							Initialized. No display appears.
↓							
Wait more than 15ms after V_{DD} rises to 4.5V							
↓							
Function Set	0	0	0	0	1	1	Function Set (8-bit interface length)
↓							
Wait more than 4.1ms							
↓							
Function Set	0	0	0	0	1	1	Function Set (8-bit interface length)
↓							
Wait more than 100us							
↓							
Function Set	0	0	0	0	1	1	Function Set (8-bit interface length)
↓							Busy Flag (BF) can not be checked before this step, but it can be checked after this step. After this step, busy flag (BF) check or longer waiting time than each instruction execution time is required.
Function Set	0	0	0	0	1	1	Function Set in 8-bit interface length. (Set 4-bit interface length)
↓	0 0	0 0	0 0	0 *	1 0	0 0	Set the 4-bit operation, 16-Character 1-Line, Pin Configuration mode A, Addressing Mode 1.
Display Off	0 0	0 0	0 1	0 0	0 0	0 0	
↓							
Display Clear	0 0	0 0	0 0	0 0	0 0	0 1	
↓							
Entry Mode Set	0 0	0 0	0 0	0 1	0 1	0 0	Example for set address increment and cursor right shift when the data write to the DD or CG RAM.
↓							
Write data to the DD/CG RAM and set the Instruction							

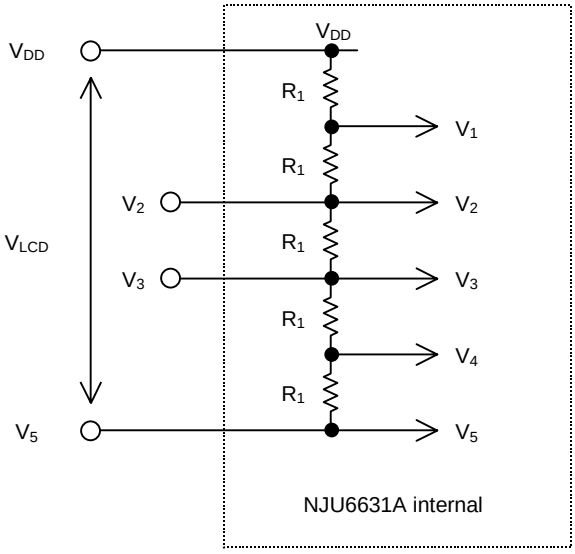
(4) LCD Display

(4-1) Power Supply for LCD Driving

NJU6631A incorporates bleeder resistance to generate the LCD display driving waveform.
The bleeder resistance is set 1/5 bias suitable for 1/18 duty ratio and 1.5kΩ per resistance.
Furthermore, the bias level can be changed by connecting external resistance between the V_2, V_3 terminals, if needed.

Table 5. LCD Driving Voltage vs Duty Ratio

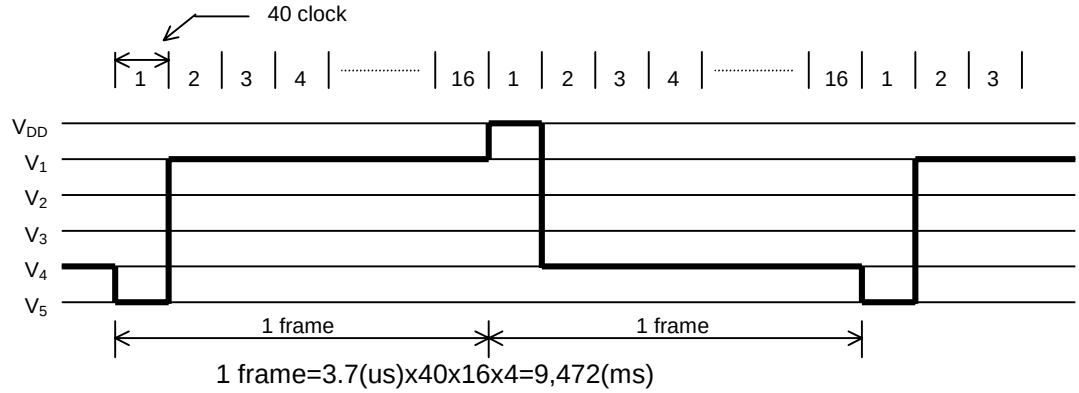
Power Supply	Duty Ratio	1/16
	Bias	1/5
	V_2	V_{DD}-2/5V_{LCD}
	V_3	V_{DD}-3/5V_{LCD}
	V_5	V_{DD}-V_{LCD}



Note) Power ON or power OFF is in the following order.
Power ON : V_5 should be turned on after the V_{DD} turned on or at the same time.
Power OFF : V_5 should be turned off before the V_{DD} turned off or at the same time.

(4-2) Relation between oscillation frequency and LCD frame frequency.

LCD frame frequency example mentioned below is based on 270kHz oscillation.
The clock for the LCD Driving is using 270kHz (1 clock=3.7us).
1/16 Duty



1 frame=3.7(us)x40x16x4=9,472(ms)
Frame frequency=1/9,472(ms)=105.6(Hz)

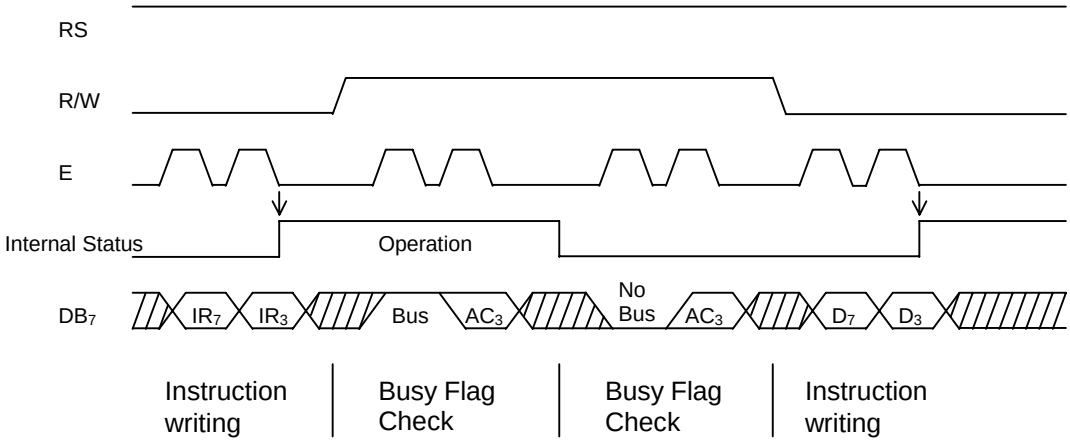
■ Interface with MPU

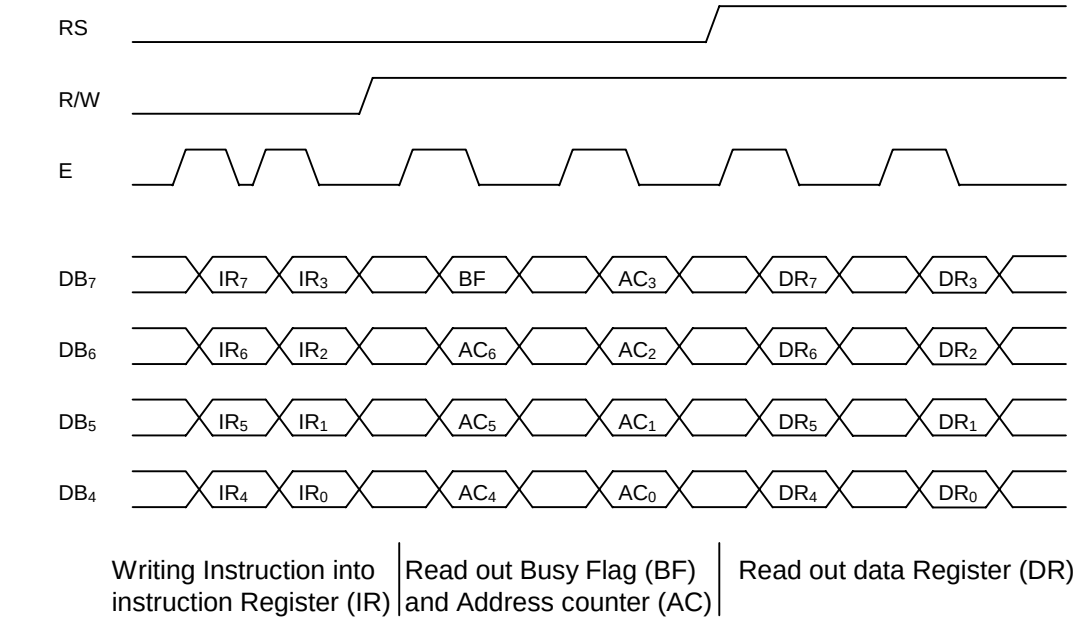
NJU6631A can be interfaced with both of 4/8 bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(1) When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

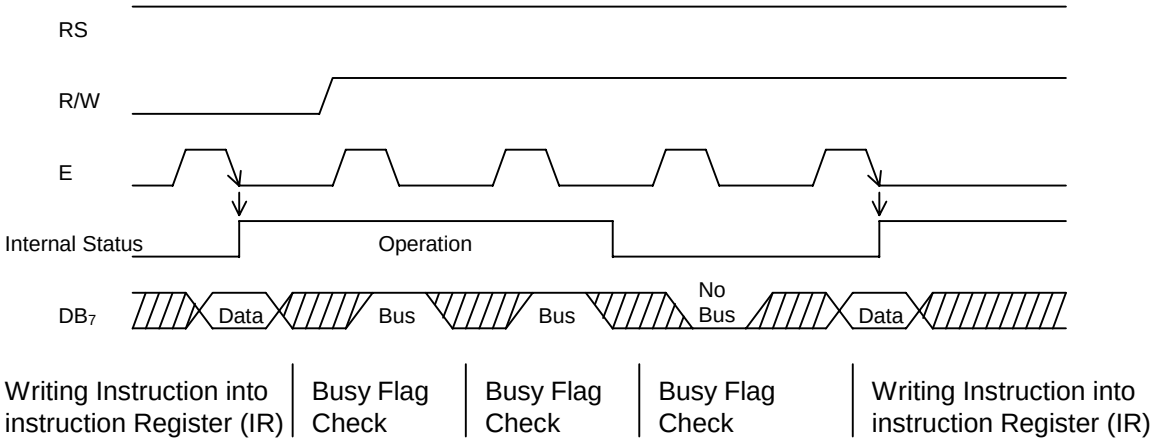
The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check must be executed after two-time 4-bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.





(2) 8-bit MPU interface



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_{opr}	-30 ~ +80	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2) All voltage values are specified as V_{SS}=0V.
Note 3) The relation : $V_{DD}>V_5\geq V_{5OUT}$, V_{SS}=0V must be maintained.
Turn on V_{DD} first then turn on V_5 must be required.
Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the LSI.

■ ELECTRICAL CHARACTERISTICS

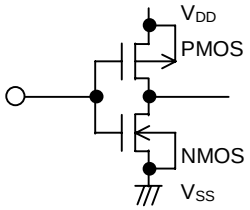
(V_{DD}=5.0V±10%, V_{SS}=0V, Ta= -20~75°C)

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit	Note
Operating Voltage		V_{DD}		4.5	5.0	5.5	V	
Input Voltage	1	V_{IH1}	All Input/Output Terminals except OSC and E Terminals	2.3	-	V_{DD}	V	5
		V_{IL1}		-	-	0.8		
	2	V_{IH2}	Only OSC Terminal	V_{DD}-1.0	-	V_{DD}		
		V_{IL2}		-	-	1.0		
	3	V_{IH3}	Only E Terminal	0.8V_{DD}		V_{DD}		
		V_{IL3}		-	-	0.2V_{DD}		
Output Voltage		V_{OH}	-I_{OH}=0.205mA	2.4	-	-	V	6
		V_{OL}	I_{OL}=1.6mA	-	-	0.4		
Driver On-resist.(COM)		R_{COM}	±Id=50uA(All COM term.)	-	-	20	kΩ	9
Driver On-resist.(SEG)		R_{SEG}	±Id=50uA(All SEG term.)	-	-	30	kΩ	9
Input Leakage Current		I_{LI}	V_{IN}=0cV_{DD}	-1	-	1	uA	7
Pull-up Resist. Current		-Ip	V_{DD}=5V	50	125	250	uA	
Operating Current		I_{DD}	CR Oscillation V_{DD}=5V, f_{OSC}=270kHz	-	1.0	1.8	mA	8
LCD Driving Voltage		V_2	Ta=25°C, V_{DD}=5V, V_5=0V Measurement Terminal is SEG.	2.7	3.0	3.3	V	
		V_3		1.7	2.0	2.3		
Bleeder Resistance		R_B	V_{DD}-V_5=5V Ta=25°C	6.65	9.5	12.35	kΩ	
Oscillation Frequency		f_{OSC}	V_{DD}=5V, Ta=25°C	135	270	405	KHz	
LCD Driving Voltage		V_{LCD}	V_5 Terminal, V_{DD}=5V	V_{DD}-3	-	V_{DD}-5	V	10

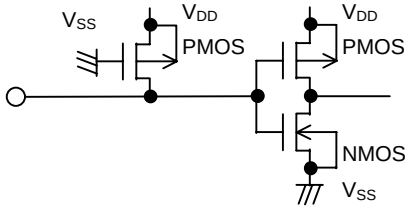
Note 5) Input / Output structure except LCD driver are shown below :

-Input Terminal Structure

E Terminal

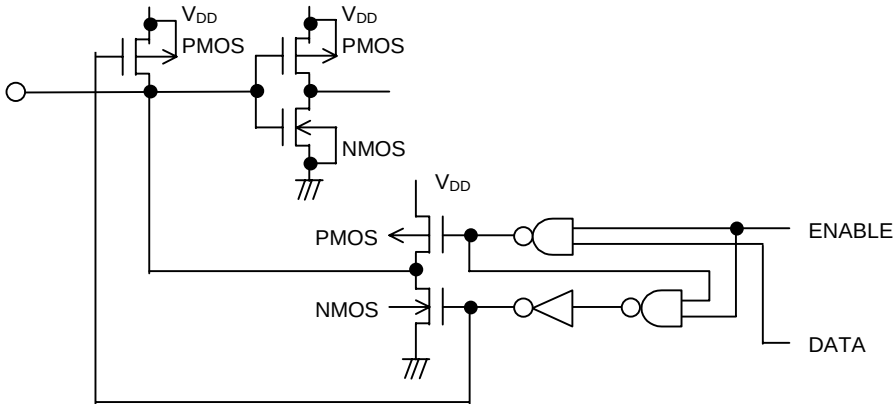


RS, R/W, $\overline{\text{RESET}}$ Terminals



-Input / Output Terminal Structure

DB_0 ~ DB_7



Note 6) Apply to the Input / Output Terminal.

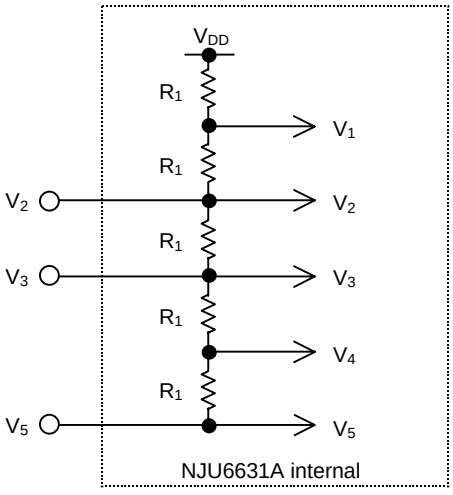
Note 7) Except pull-up resistance current and output driver current.

Note 8) Except Input/output current but including the current flow on bleeder resistance.

Note 9) R_{COM} and R_{SEG} are the resistance values between power supply terminals(V_{DD},V_2,V_3,V_5) and each common terminal (COM_1~COM_{16}), and supply voltage (V_{DD},V_2,V_3,V_5) and each segment terminal (SEG_1~SEG_{40}) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.

Note 10) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD Driving constant voltage(V_{DD}, V_5) at no load condition.

-Bleeder Resistance



■ Bus timing characteristics

-Write operation sequence (Write from MPU to NJU6631A)

(V_{DD}=5.0V±10%, V_{SS}=0V, Ta=-20~75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Enable Cycle Time		tCYCE	500	-	fig.1	ns
Enable Pulse Width	"High" level	PWEH	220	-		ns
	"Low" level	PWEL	280	-		ns
Enable Rise Time, Fall Time		tEr, tEf	-	20		ns
Set up Time	RS, R/W-E	tAS	40	-		ns
Address Hold Time		tAH	10	-		ns
Data Set up Time		tDSW	60	-		ns
Data Hold Time		tH	10	-		ns

Timing Characteristics (Write operation)

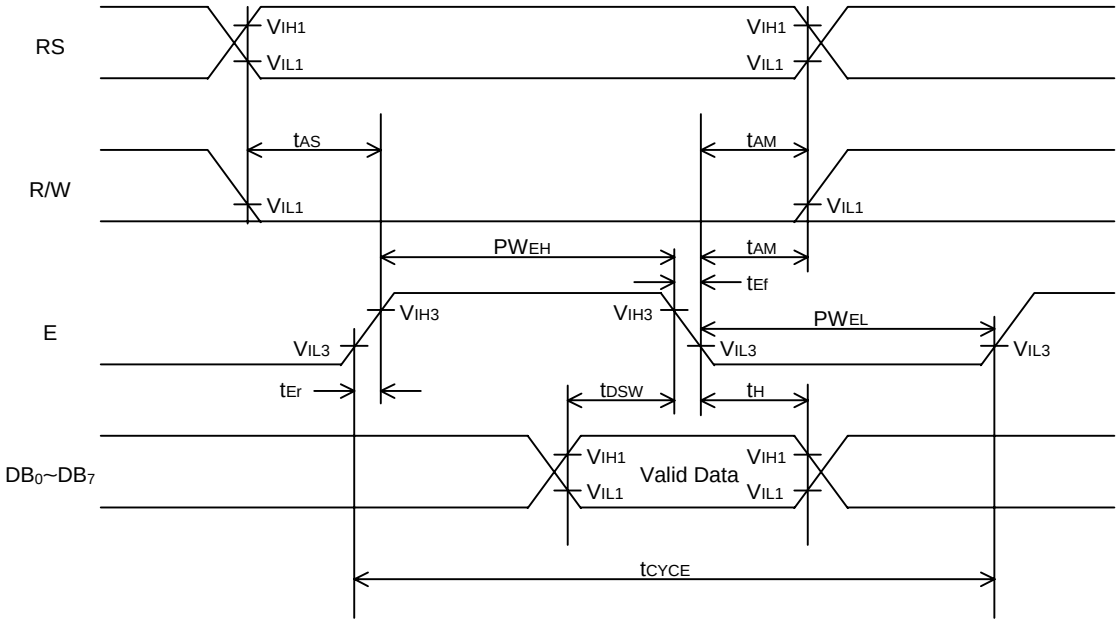


fig. 1 The timing characteristics of the bus write operating sequence.
(Write from MPU to NJU6631A)

-Read operation sequence (Read from NJU6631A to MPU)

(V_{DD}=5.0V±10%, V_{SS}=0V, Ta=-20~75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Enable Cycle Time		tCYCE	500	-	fig.2	ns
Enable Pulse Width	"High" level	PWEH	220	-		ns
	"Low" level	PWEL	280	-		ns
Enable Rise Time, Fall Time		tEr, tEf	-	20		ns
Set up Time	RS, R/W-E	tAS	40	-		ns
Address Hold Time		tAH	10	-		ns
Data Delay Time		tDDR	-	240		ns
Data Hold Time		tDHR	20	-		ns

-DB_0~DB_7 Load Condition : CL=100pF

Timing Characteristics (Read operation)

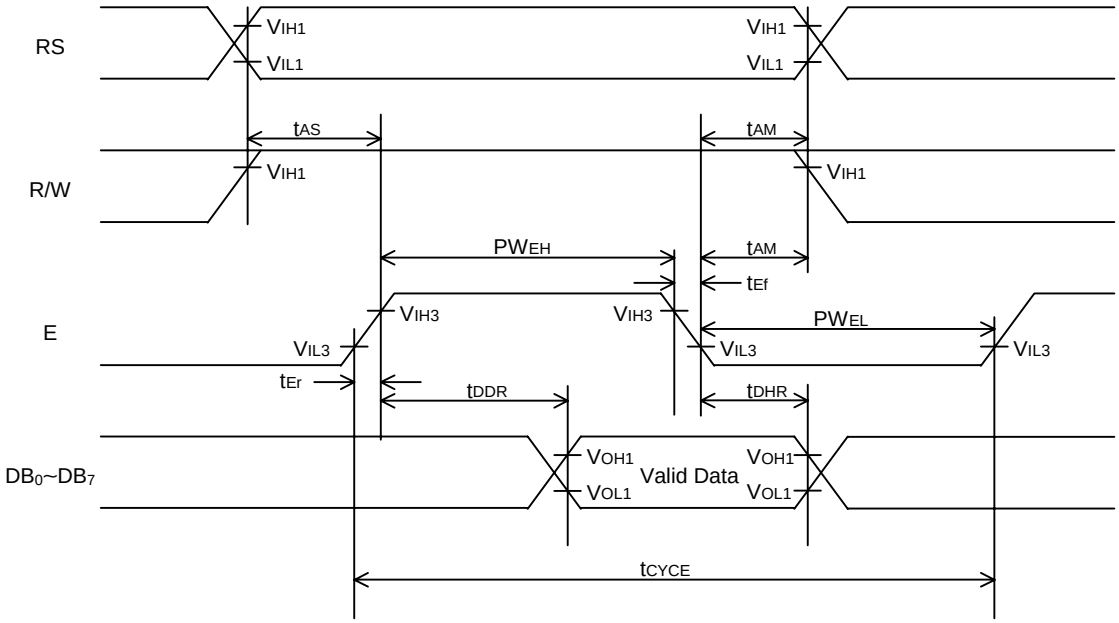


fig. 2 The timing characteristics of the bus read operating sequence.
(Read from NJU6631A to MPU)

-The Input Condition when using the Hardware Reset Circuit

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Reset Input "L" Level Width	t_{RSL}	f_{OSC}=270kHz	1.2	-	-	ms

Input Timing

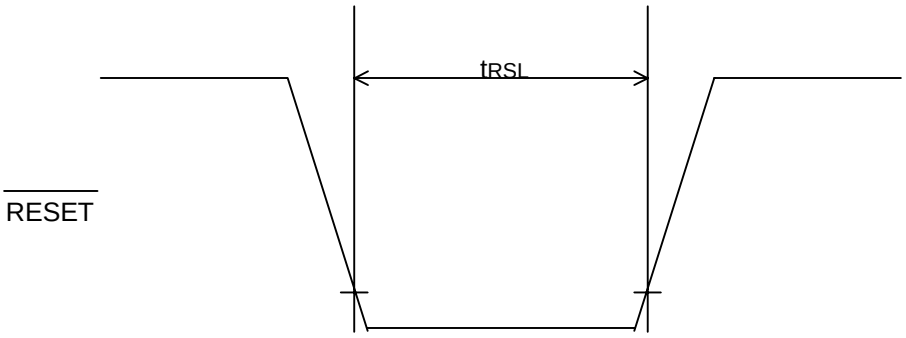
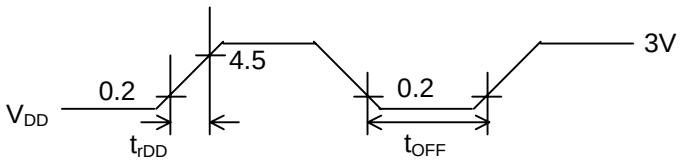


fig. 3 The timing characteristics of the Hardware Reset input

• Power supply condition when using the internal initialization circuit (Ta=-20 to 75°C)

P A R A M E T E R	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power supply rise time	t_{rDD}	–	0.1	–	5	ms
Power supply OFF time	t_{OFF}	–	1	–	–	ms

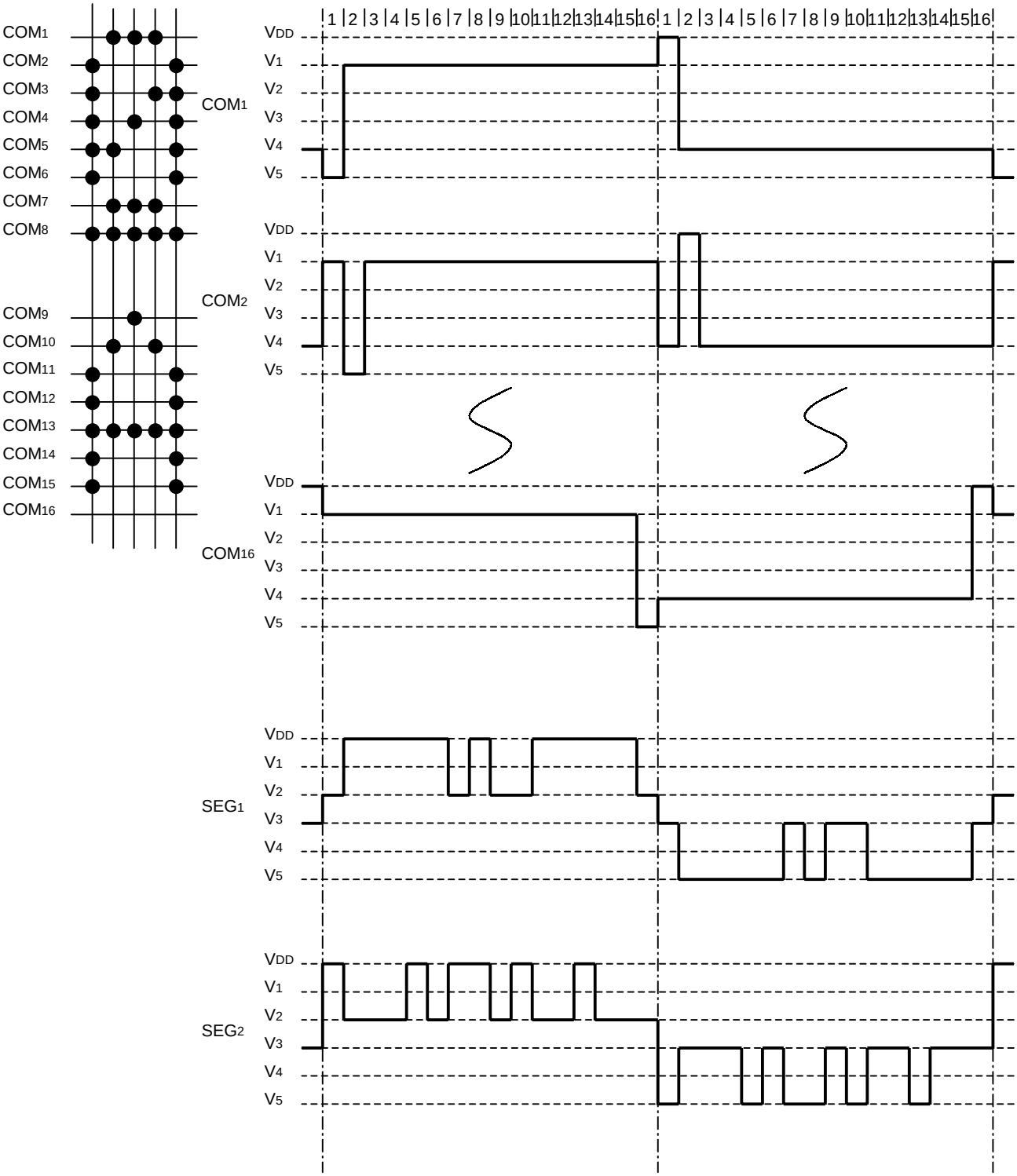


*t_{OFF} specifies the power OFF time in a short period OFF or cyclical ON/OFF

$0.1ms \leq t_{rDD} \leq 10ms$ $t_{OFF} \leq 1ms$

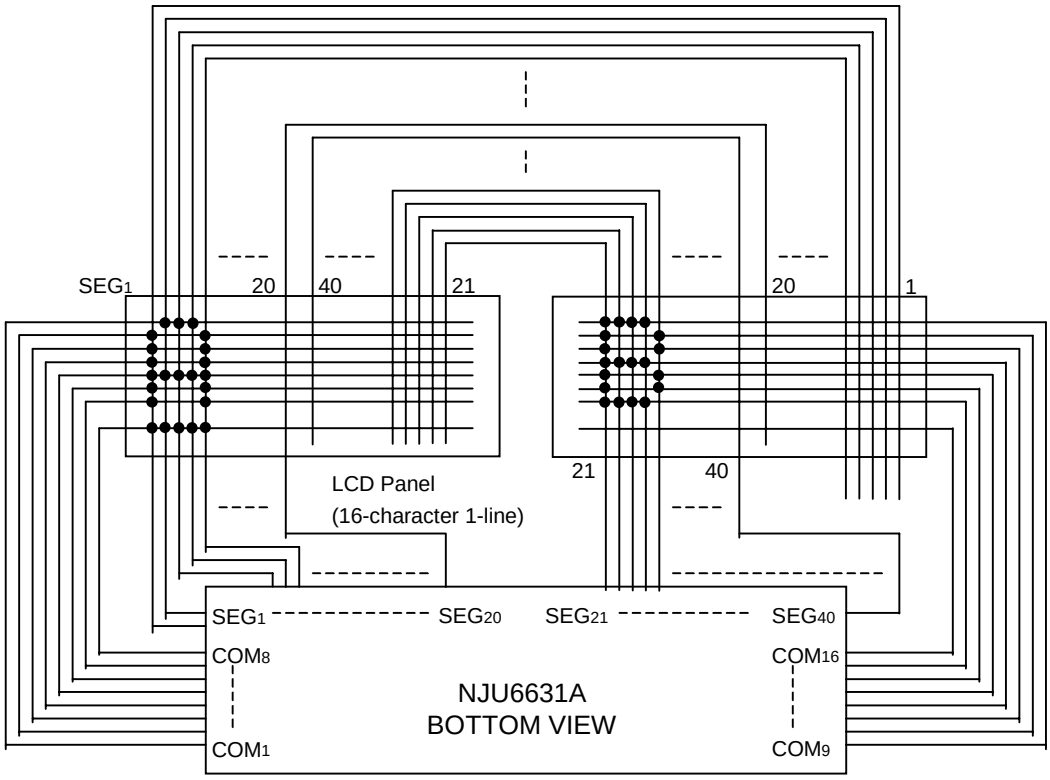
Note.) Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction(Refer to initialization by the instruction).

■ LCD DRIVING WAVEFORM

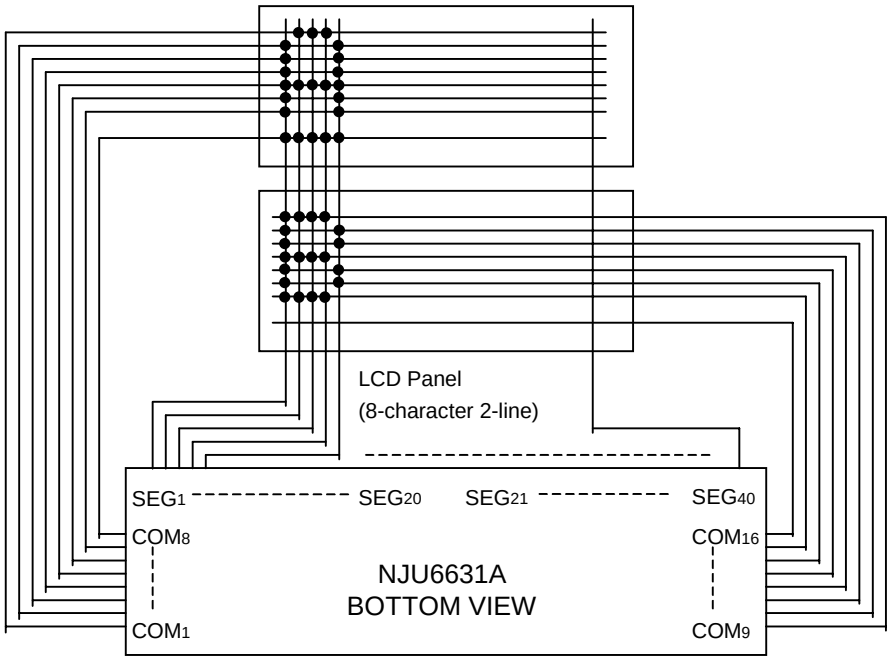


■ APPLICATION CIRCUITS

(1) LCD display interface Pin configuration mode A (BOTTOM VIEW)



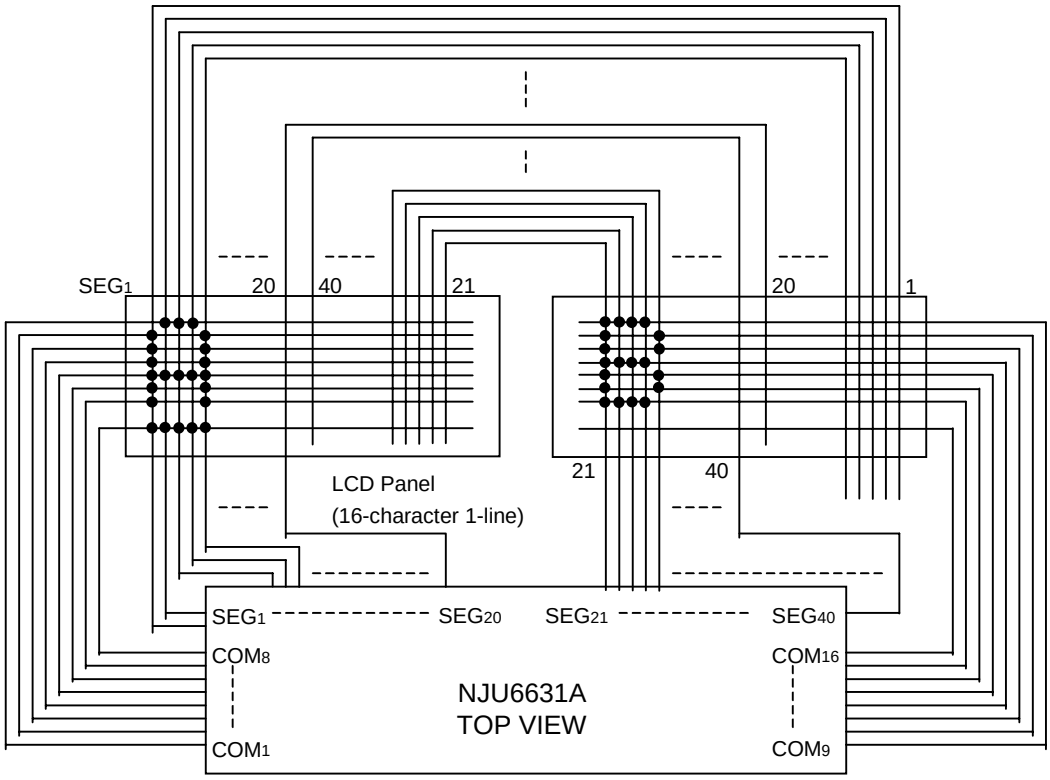
Mode A, 16-character 1-line display example (M0=0, M1=0)



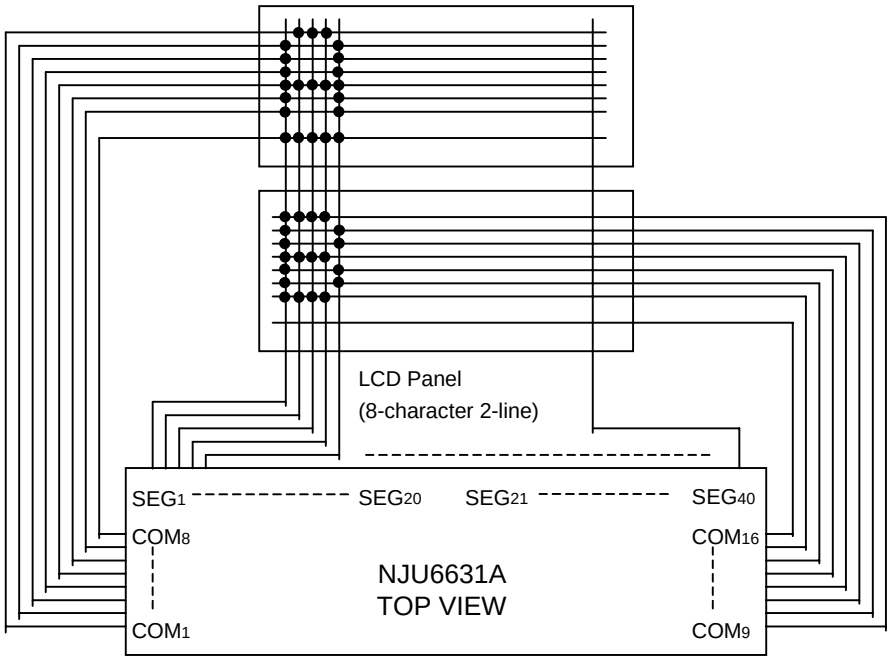
Mode A, 8-character 2-line display example (M0=0, M1=1)

■ APPLICATION CIRCUITS

(2) LCD display interface Pin configuration mode B (TOP VIEW)



Mode B, 16-character 1-line display example (M0=1, M1=0)



Mode B, 8-character 2-line display example (M0=1, M1=1)

MEMO

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