

ESD241-B1-W0201

Protection Devices

TVS (Transient Voltage Suppressor)

Bi-directional, 3.3 V, 6.5 pF, 0201, RoHS and Halogen Free compliant

Features

- ESD / transient protection according to:
 - IEC61000-4-2 (ESD): ± 18 kV (air / contact discharge)
 - IEC61000-4-4 (EFT): ± 2 kV / ± 40 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 4.5 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{RWM} = \pm 3.3$ V
- Line capacitance: $C_L = 6.5$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 6$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.09 \Omega$ (typical)
- Very low reverse current: $I_R < 1$ nA (typical)
- Small form factor SMD Size 0201 and low profile 0.58 mm x 0.28 mm x 0.15 mm
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package



Guidelines for optimized PCB design and assembly process are available in [\[2\]](#).

Potential applications

- IC/ASICs in audio, headset
- Human digital interfaces, buttons, GPIO

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

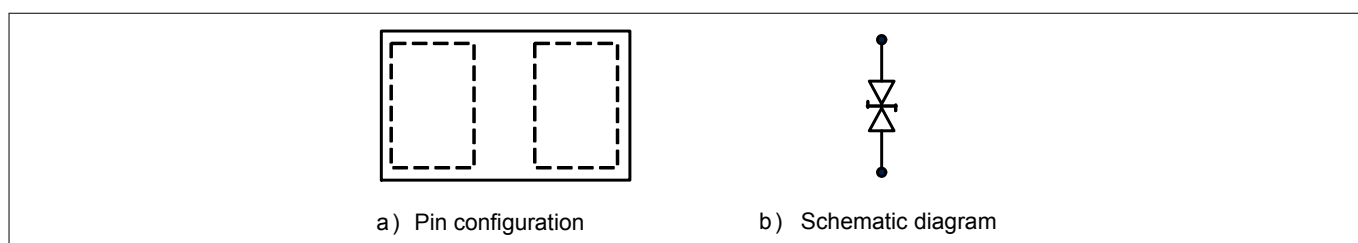


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD241-B1-W0201	WLL-2-3	1 line, bi-directional	AC ¹⁾

¹ The device does not have any marking on the device top. The marking code is on the pads.

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Maximum ratings

1 Maximum ratings

Note: $T_A = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings¹⁾

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	± 3.3	V
ESD discharge ²⁾	V_{ESD} (contact)	± 18	kV
	V_{ESD} (air)	± 18	
Peak pulse power ³⁾	P_{PK}	25	W
Peak pulse current ³⁾	I_{PP}	± 4.5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

¹ Device is electrically symmetrical

² V_{ESD} according to IEC61000-4-2 (R = 330 Ω , C = 150 pF discharge network)

³ Stress pulse: 8/20 μ s current waveform according to IEC61000-4-5

2 Electrical characteristics

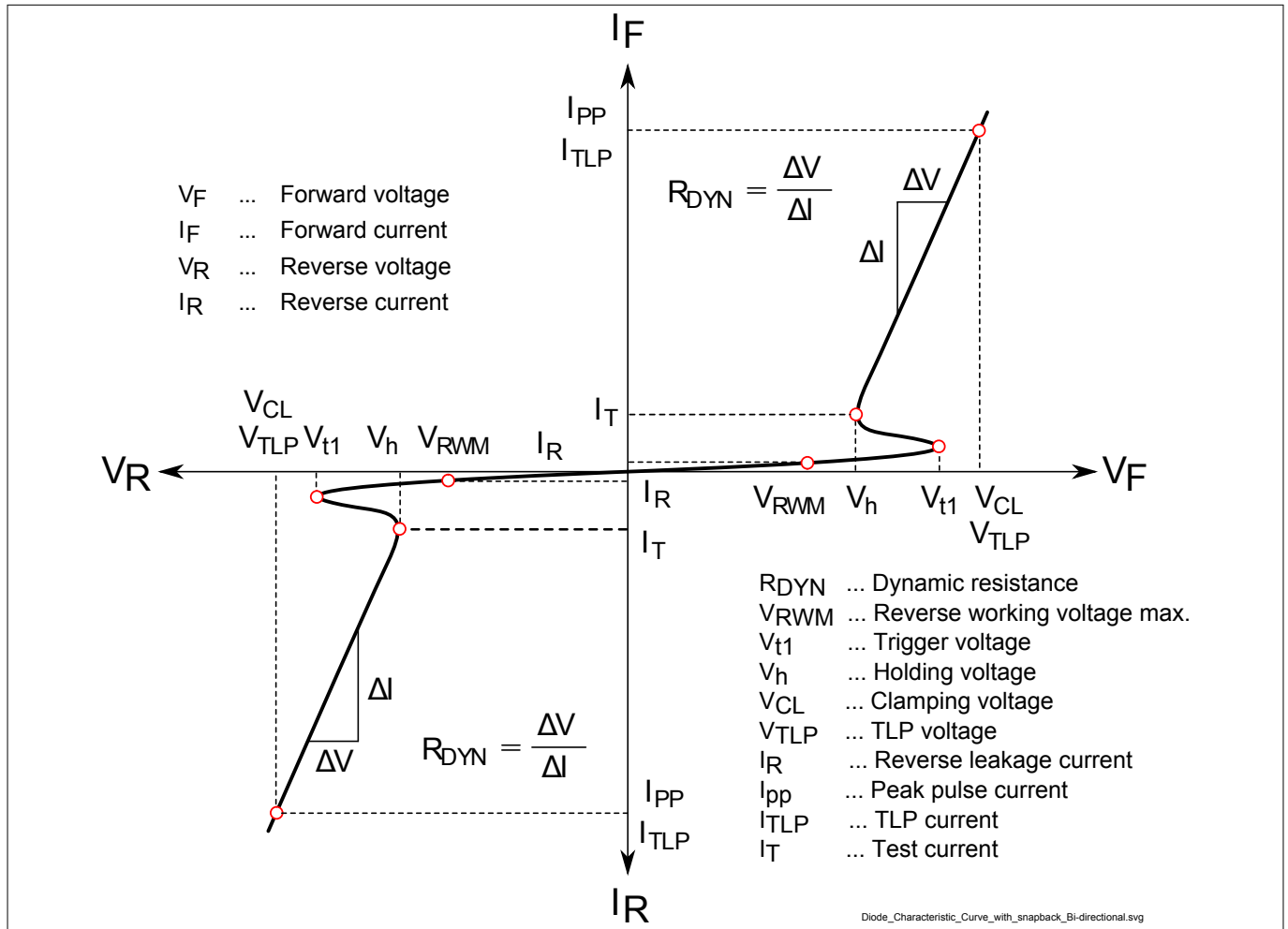


Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics ($T_A = 25\text{ °C}$, unless otherwise specified) ¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Trigger Voltage ²⁾³⁾	V_{t1}	5	6	–	V	–
Holding voltage ⁴⁾	V_h	4	5.7	7.2	V	$I_R = 1\text{ mA}$
Reverse current	I_R	–	1	30	nA	$V_R = 3.3\text{ V}$

Table 4 AC characteristics ($T_A = 25\text{ °C}$, unless otherwise specified) ¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	6.5	–	pF	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$
		–	6.5	–		$V_R = 0\text{ V}$, $f = 1\text{ GHz}$

Table 5 ESD and Surge characteristics ($T_A = 25\text{ °C}$, unless otherwise specified) ¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage ⁵⁾	V _{CL}	–	6	–	V	I _{TLP} = 16 A, t _p = 100 ns
		–	7	–		I _{TLP} = 30 A, t _p = 100 ns
Clamping voltage ⁶⁾		–	5	–		I _{PP} = 1 A, t _p = 8/20 μs
		–	6	–		I _{PP} = 4 A, t _p = 8/20 μs
Dynamic resistance ⁵⁾	R _{DYN}	–	0.09		Ω	t _p = 100 ns

¹⁾ Device is electrically symmetrical

²⁾ Verified by design

³⁾ Voltage forced

⁴⁾ Current forced

⁵⁾ Please refer to Application Note AN210 [\[1\]](#). TLP parameters: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$.

⁶⁾ Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Typical characteristic diagrams

3 Typical characteristic diagrams

Note: $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

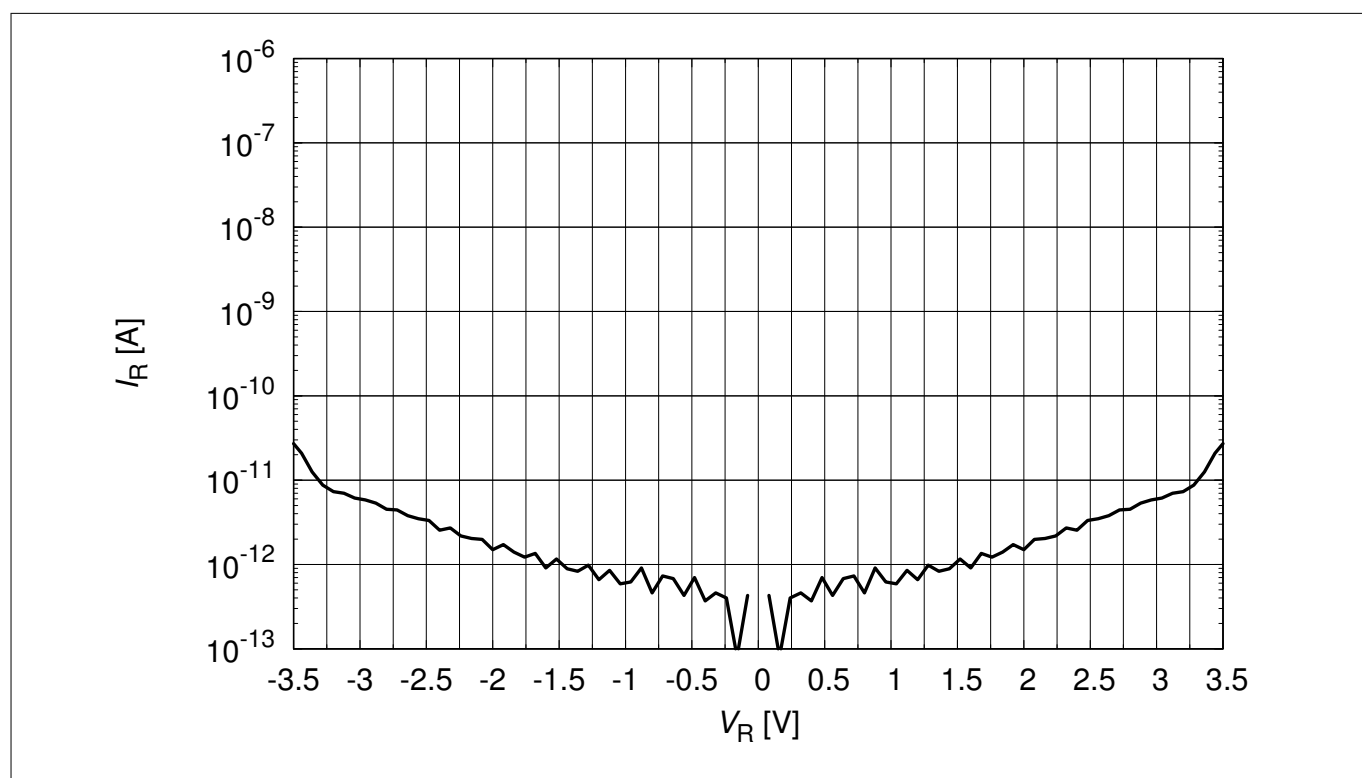


Figure 3 Reverse leakage current: $I_R = f(V_R)$

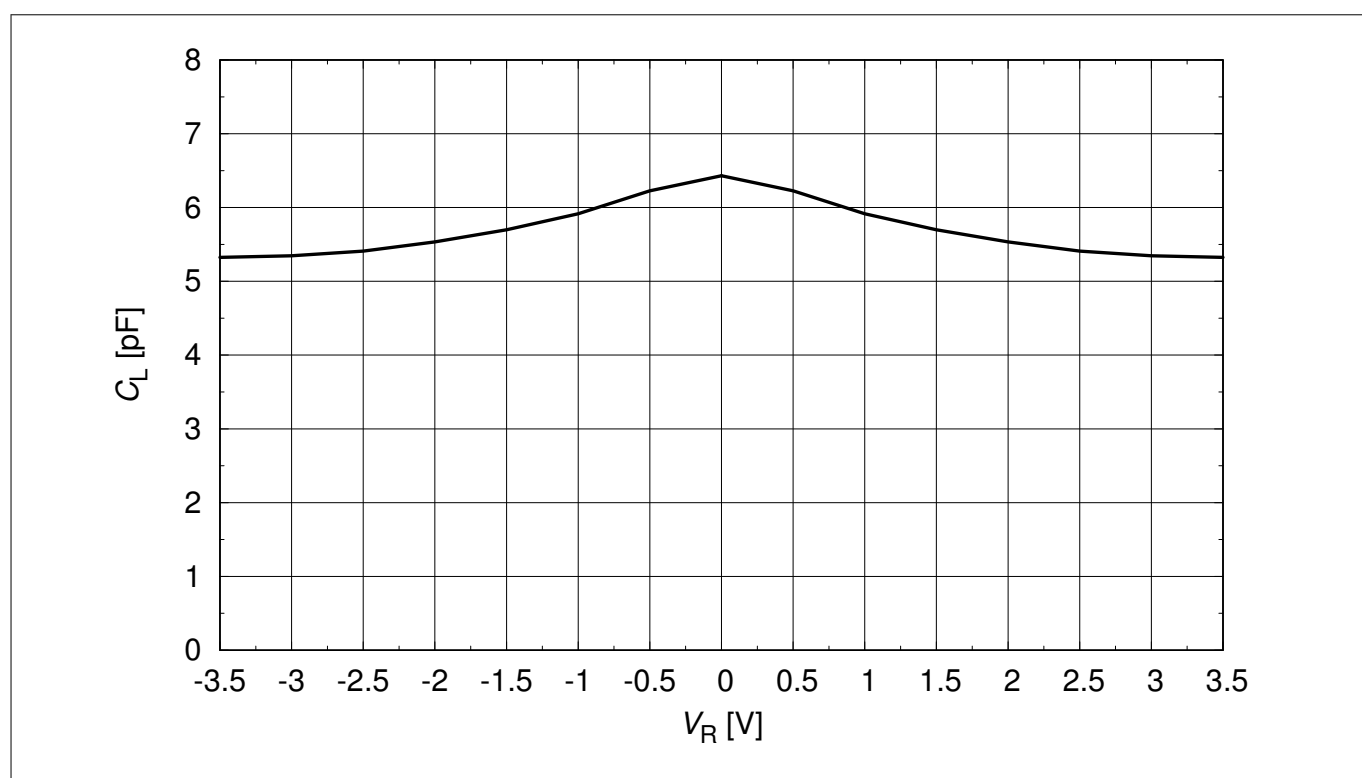


Figure 4 Line capacitance: $C_L = f(V_R)$, $f = 1\text{ MHz}$

Typical characteristic diagrams

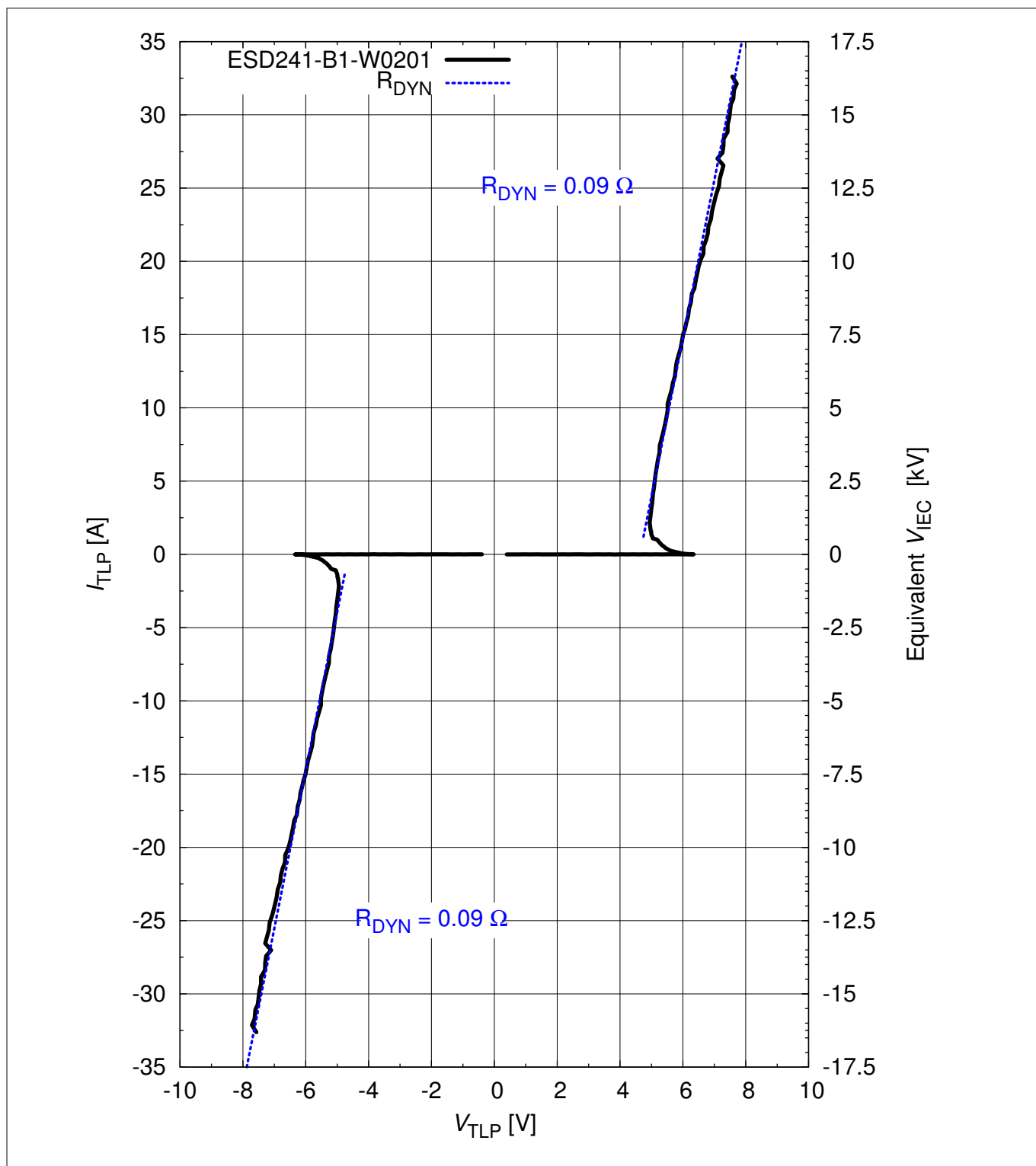


Figure 5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

Typical characteristic diagrams

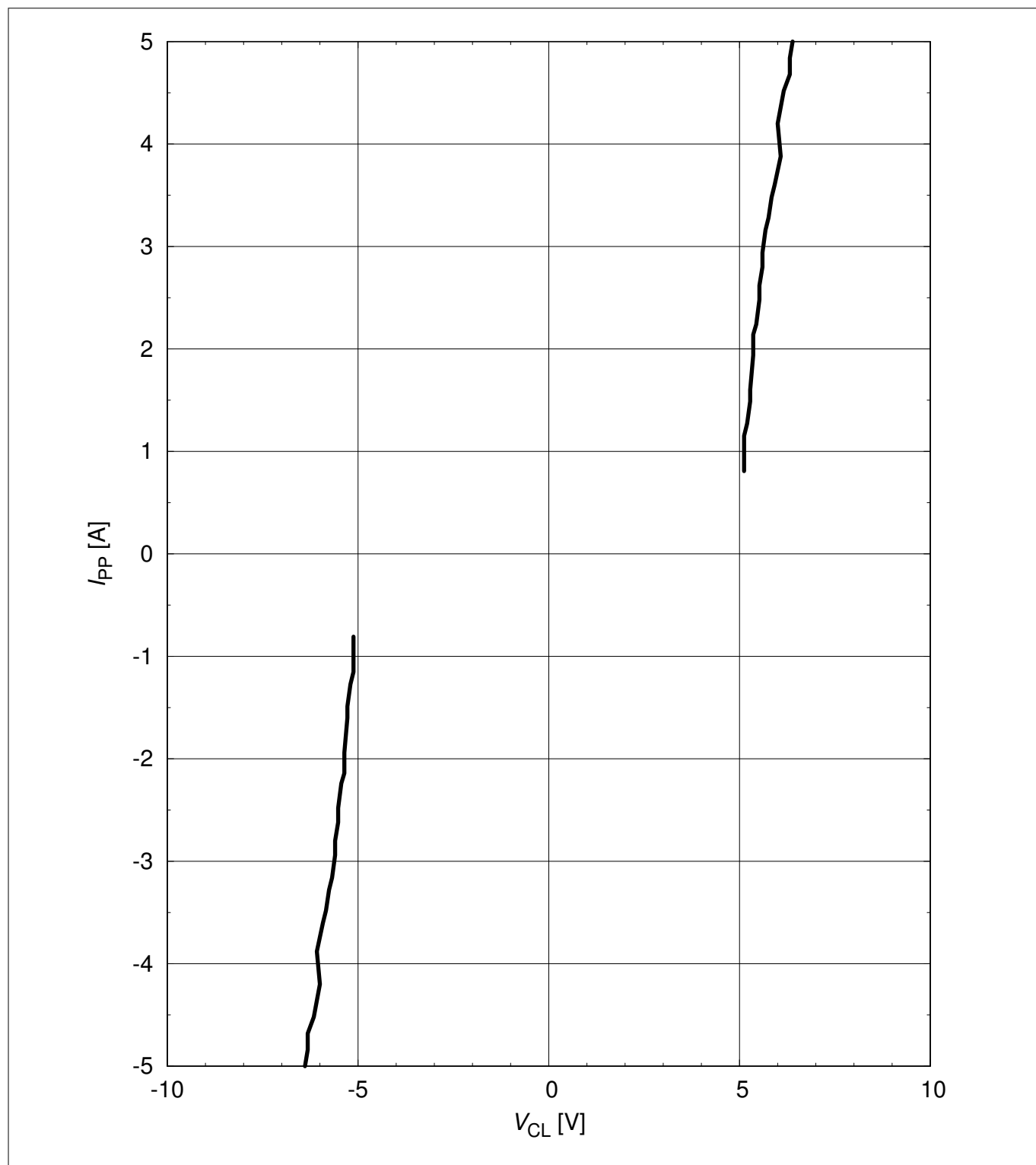


Figure 6 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ [1]

Package information

4 Package information

4.1 WLL-2-3 package

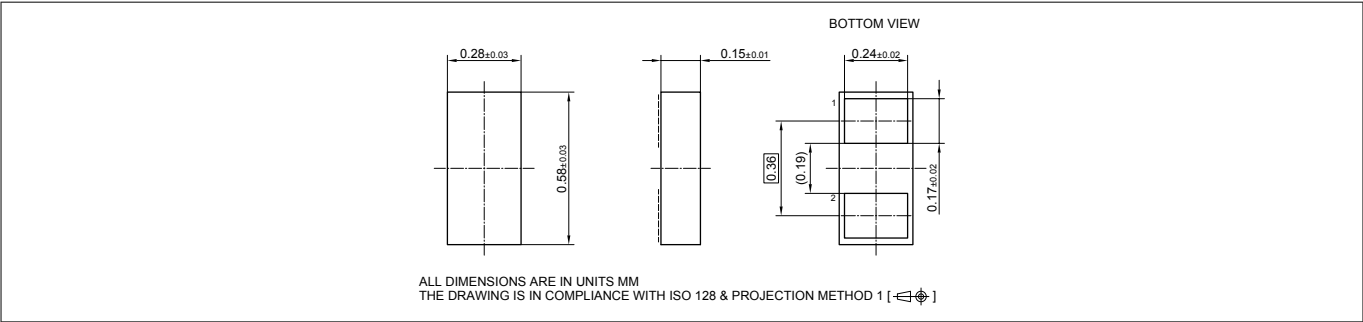


Figure 7 WLL-2-3 package outline (dimension in mm)

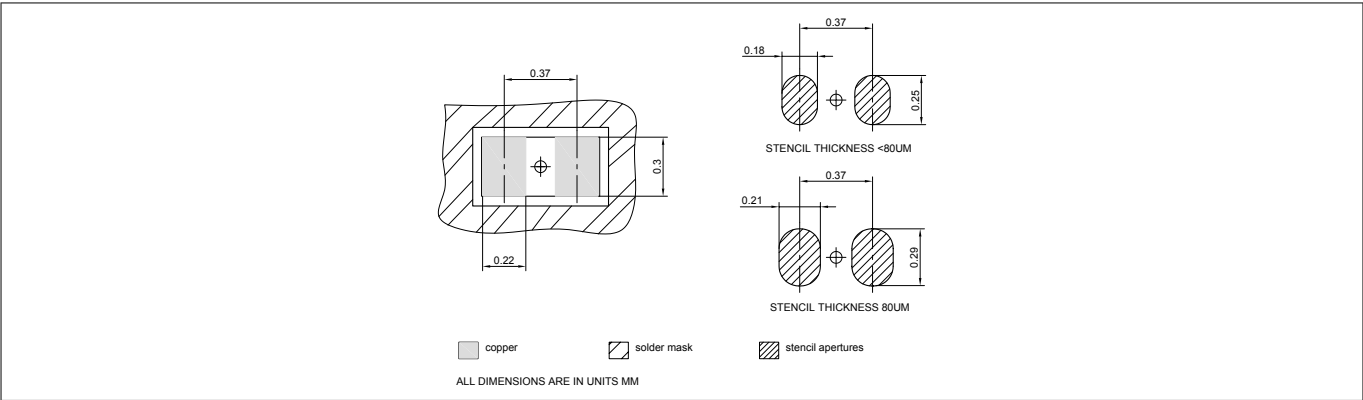


Figure 8 WLL-2-3 footprint (dimension in mm), recommendation for Printed Circuit Board Assembly see [2]

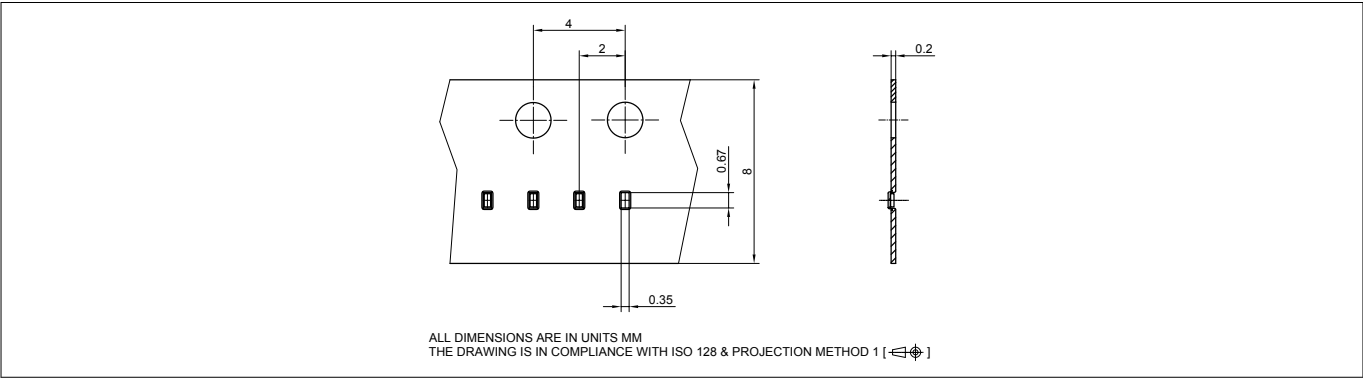


Figure 9 WLL-2-3 packing (dimension in mm)

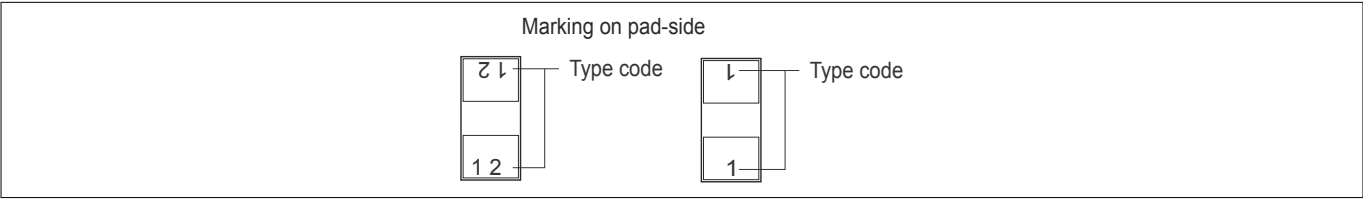


Figure 10 WLL-2-3 marking example (see Table 1)

References

5 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/Packageinformation_WLL
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

Revision history

Revision history: Rev. 0.9.1, 2017-01-25

Page or Item	Subjects (major changes since previous revision)
Revision 1.0 2017-06-26	
All	Final datasheet

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