

SD-SST210/214 N-CHANNEL LATERAL DMOS SWITCH

Product Summary

Part Number	V _{(BR)DS} Min(V)	V _{GS(th)} Max (V)	r _{DS(on)} Max(Ω)	C _{rss} Max (pF)	t _{ON} Max (ns)
SD210DE	30	1.5	45 @ V _{GS} = 10V	0.5	2
SD214DE	20	1.5	45 @ V _{GS} = 10V	0.5	2
SST210	30	1.5	50 @ V _{GS} = 10V	0.5	2
SST214	20	1.5	50 @ V _{GS} = 10V	0.5	2

Features

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

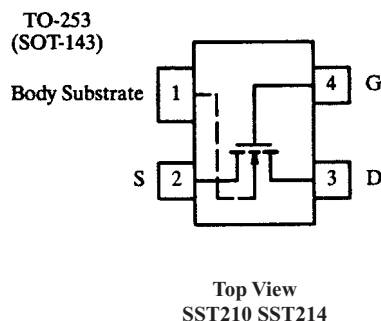
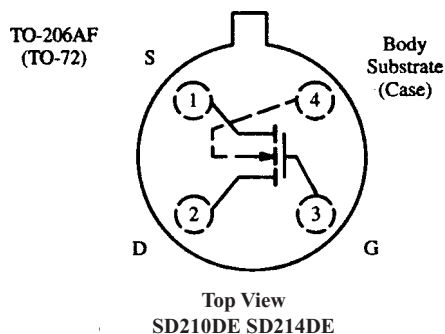
- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

The SD210DE/214DE are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD214DE is normally used for ± 10 -V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not have a gate protection Zener

diode which results in lower gate leakage and $\pm$ voltage capability from gate to substrate. A poly-silicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, and Zener protected—SD211DE/SST211 series.



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage	± 40 V	Source-Substrate Voltage (SD210DE)	15 V
Gate-Substrate Voltage	± 30 V	(SD214DE)	25 V
Drain-Source Voltage (SD210DE)	30 V	Drain Current	50 mA
(SD214DE)	20 V	Lead Temperature (1/16" from case for 10 seconds)	300°C
Source-Drain Voltage (SD210DE)	10 V	Storage Temperature	-65 to 150°C
(SD214DE)	20 V	Operating Junction Temperature	-55 to 125°C
Drain-Substrate Voltage (SD210DE)	30 V	Power Dissipation ^a	300 mW
(SD214DE)	25 V		

Notes:

a. Derate 3 mW/°C above 25°C

Specifications^a

Parameter	Symbol ^b	Test Conditions ^b	Typ ^c	Limits				Unit	
				SD210DE		SD214DE			
				Min	Max	Min	Max		
Static									
Drain-Source Breakdown Voltage	V _{(BR)DS}	V _{GS} = V _{BS} = 0 V, I _D = 10 μA	35	30				V	
		V _{GS} = V _{BS} = -5 V, I _D = 10 nA	30	10		20			
Source-Drain Breakdown Voltage	V _{(BR)SD}	V _{GD} = V _{BD} = -5 V, I _S = 10 nA	22	10		20			
Drain-Substrate Breakdown Voltage	V _{(BR)DBO}	V _{GB} = 0 V, I _D = 10 nA, Source Open	35	15		25			
Source-Substrate Breakdown Voltage	V _{(BR)SBO}	V _{GB} = 0 V, I _S = 10 μA, Drain Open	35	15		25			
Drain-Source Leakage	I _{DS(off)}	V _{GS} = V _{BS} = -5 V	V _{DS} = 10 V	0.4		10		nA	
			V _{DS} = 20 V	0.9			10		
Source-Drain Leakage	I _{SD(off)}	V _{GD} = V _{BD} = -5 V	V _{SD} = 10 V	0.5		10			
			V _{SD} = 20 V	0.8			10		
Gate Leakage	I _{GBS}	V _{DB} = V _{SB} = 0 V, V _{GB} = ±40 V	0.001		0.1		0.1		
Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 μA, V _{SB} = 0 V	0.8	0.5	1.5	0.1	1.5	V	
Drain-Source On-Resistance	r _{DS(on)}	V _{SB} = 0 V I _D = 1 mA	V _{GS} = 5 V	58		70		70	Ω
			V _{GS} = 10 V	38		45		45	
			V _{GS} = 15 V	30					
			V _{GS} = 20 V	26					
			V _{GS} = 25 V	24					
Dynamic									
Forward Transconductance	g _{fs}	V _{DS} = 10 V, V _{SB} = 0 V, I _D = 20 mA f = 1 kHz	11	10		10		mS	
	g _{os}		0.9						
Gate Node Capacitance	C _(GS+GD+GB)	V _{DS} = 10 V, f = 1 MHz V _{GS} = V _{BS} = -15 V	2.5		3.5		3.5	pF	
Drain Node Capacitance	C _(GD+DB)		1.1		1.5		1.5		
Source Node Capacitance	C _(GS+SB)		3.7		5.5		5.5		
Reverse Transfer Capacitance	C _{rss}		0.2		0.5		0.5		
Switching									
Turn-On Time	t _{d(on)}	V _{SB} = 0 V, V _{IN} 0 to 5 V, R _G = 25 Ω V _{DD} = 5 V, R _L = 680 Ω	0.5		1		1	ns	
	t _r		0.6		1		1		
Turn-Off Time	t _{d(off)}		2						
	t _f		6						

Notes:

a. $T_A = 25^\circ\text{C}$ unless otherwise noted.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.