

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC107AP, TC74HC107AF

Dual J-K Flip Flop with Clear

The TC74HC107A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic levels applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

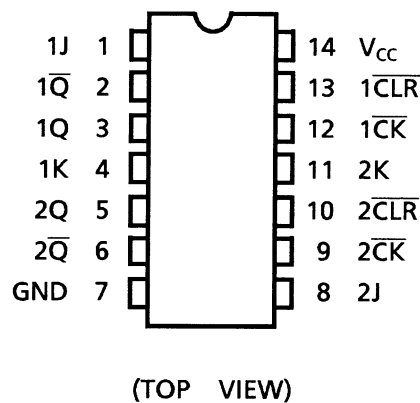
$\overline{\text{CLR}}$ is independent of the clock and is accomplished by a low logic level on the input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

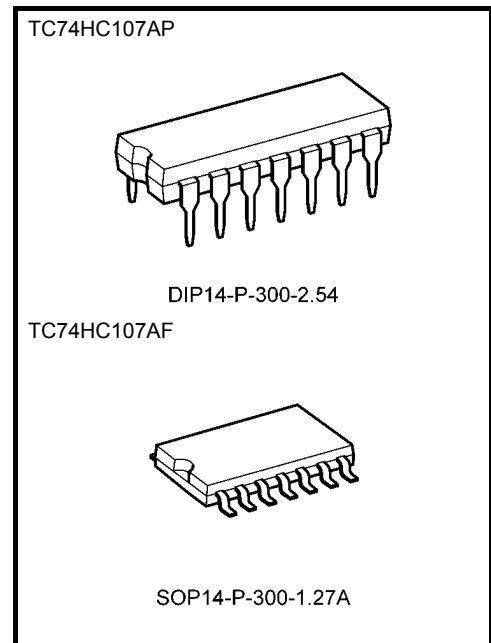
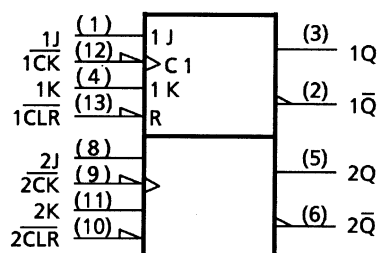
Features

- High speed: $f_{\text{max}} = 75 \text{ MHz}$ (typ.) at $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 2 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$ (min)
- Balanced propagation delays: $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide operating voltage range: $V_{\text{CC}} (\text{opr}) = 2\sim 6 \text{ V}$
- Pin and function compatible with 74LS107

Pin Assignment



IEC Logic Symbol



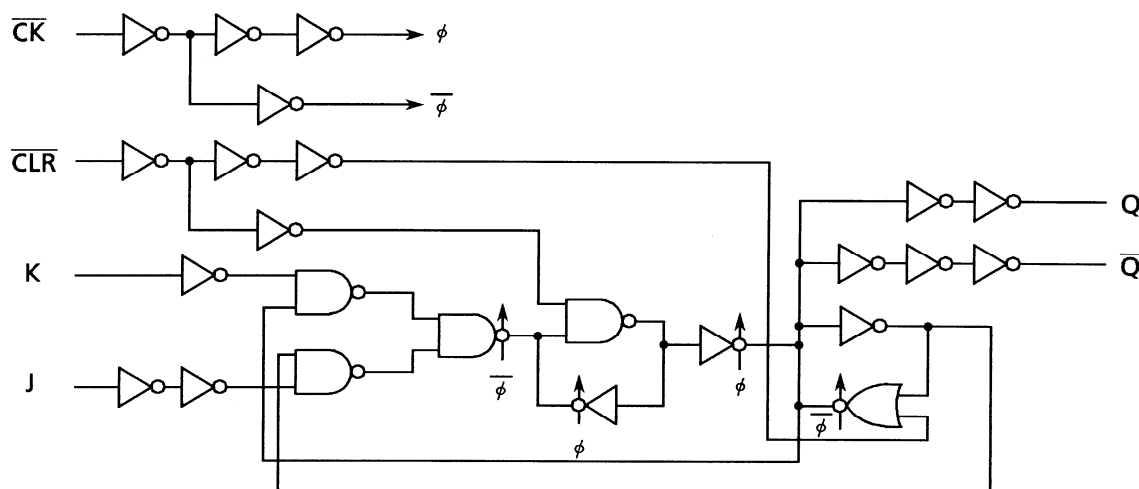
Weight	
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)

Truth Table

Inputs				Outputs		Function
$\overline{\text{CLR}}$	J	K	$\overline{\text{CK}}$	Q	$\overline{\text{Q}}$	
L	X	X	X	L	H	Clear
H	L	L	$\downarrow$	Q_n	$\overline{\text{Q}}_n$	No Change
H	L	H	$\downarrow$	L	H	—
H	H	L	$\downarrow$	H	L	—
H	H	H	$\downarrow$	$\overline{\text{Q}}_n$	Q_n	Toggle
H	X	X	$\uparrow$	Q_n	$\overline{\text{Q}}_n$	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5~7	V
DC input voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10 \text{ mW}/^\circ\text{C}$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2~6	V
Input voltage	V_{IN}	0~ V_{CC}	V
Output voltage	V_{OUT}	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	t_r, t_f	0~1000 ($V_{CC} = 2.0$ V) 0~500 ($V_{CC} = 4.5$ V) 0~400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max
High-level input voltage	V_{IH}	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V
Low-level input voltage	V_{IL}	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	V
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
			$I_{OH} = -4\ \text{mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
			$I_{OH} = -5.2\ \text{mA}$	6.0	5.68	5.80	—	5.63	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 4\ \text{mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	
			$I_{OL} = 5.2\ \text{mA}$	6.0	—	0.18	0.26	—	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND		6.0	—	—	± 0.1	—	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		6.0	—	—	2.0	—	μA

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 ~ 85°C		Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width ($\overline{\text{CK}}$)	t_W (L) t_W (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{CLR}}$)	t_W (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{\text{CLR}}$)	t_{rem}	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	5	5	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	37	30	

AC Characteristics ($C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH}	—	—	4	8	ns
	t_{THL}					
Propagation delay time ($\overline{\text{CK}}$ - Q, $\overline{\text{Q}}$)	t_{pLH}	—	—	11	21	ns
	t_{pHL}					
Propagation delay time ($\overline{\text{CLR}}$ - Q, $\overline{\text{Q}}$)	t_{pLH}	—	—	12	24	ns
	t_{pHL}					
Maximum clock frequency	f_{max}	—	34	75	—	MHz

AC Characteristics ($C_L = 50 \text{ pF}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time ($\overline{CK} \rightarrow Q, \overline{Q}$)	t_{pLH} t_{pHL}	—	2.0	—	48	125	—	155	ns
			4.5	—	14	25	—	31	
			6.0	—	12	21	—	26	
Propagation delay time ($\overline{CLR} \rightarrow Q, \overline{Q}$)	t_{pLH} t_{pHL}	—	2.0	—	52	140	—	175	ns
			4.5	—	15	28	—	35	
			6.0	—	13	24	—	30	
Maximum clock frequency	f_{max}	—	2.0	6	23	—	5	—	MHz
			4.5	31	70	—	25	—	
			6.0	37	80	—	30	—	
Input capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—	—	—	33	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

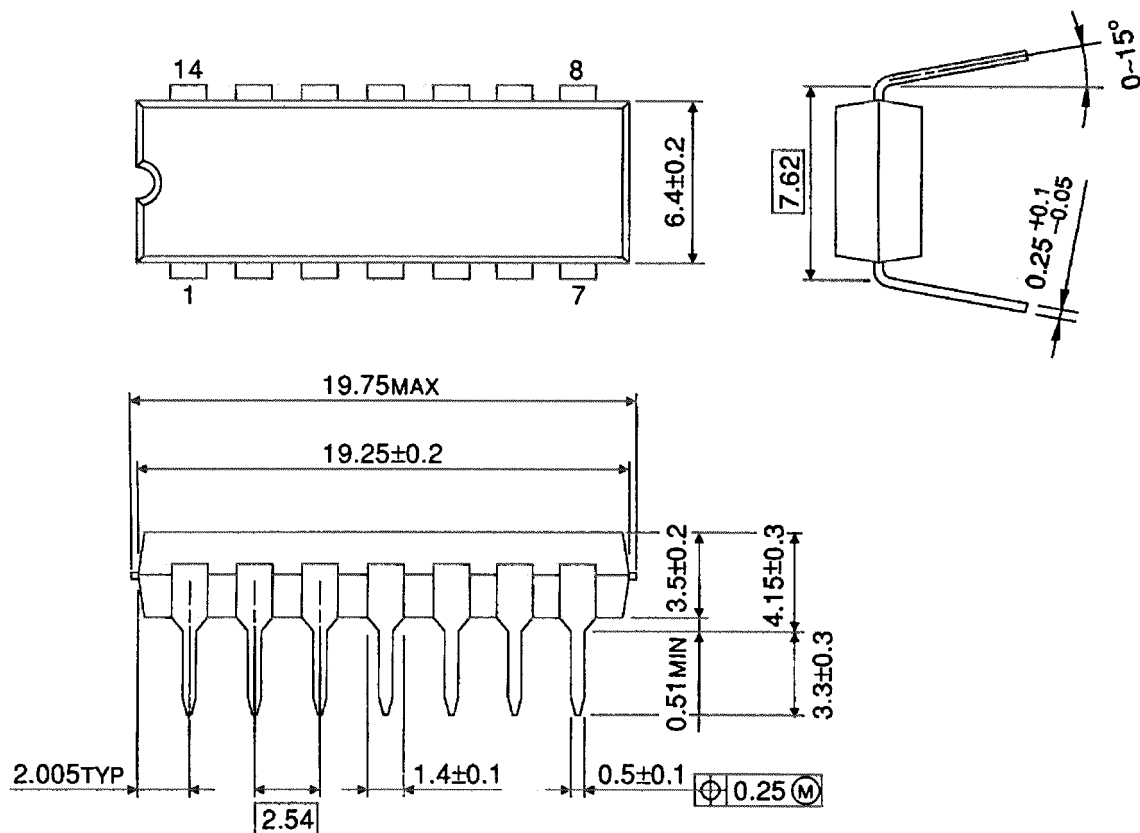
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

Package Dimensions

DIP14-P-300-2.54

Unit : mm

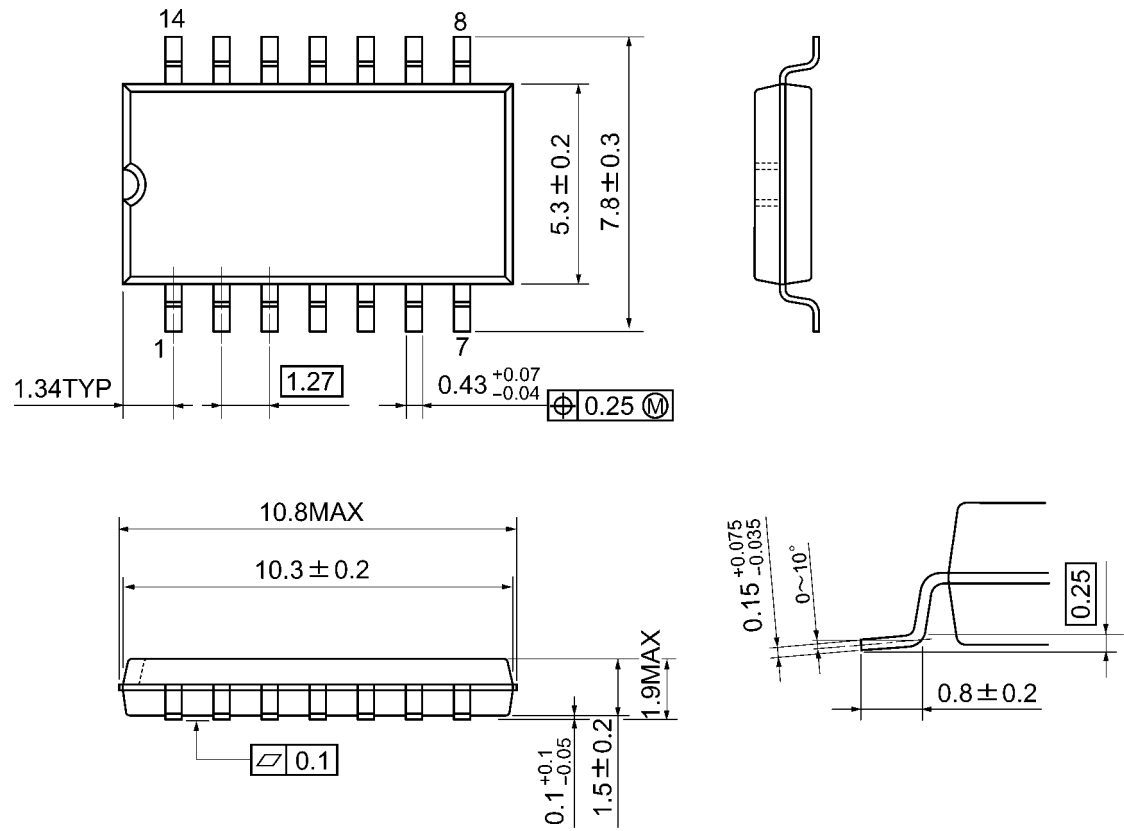


Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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