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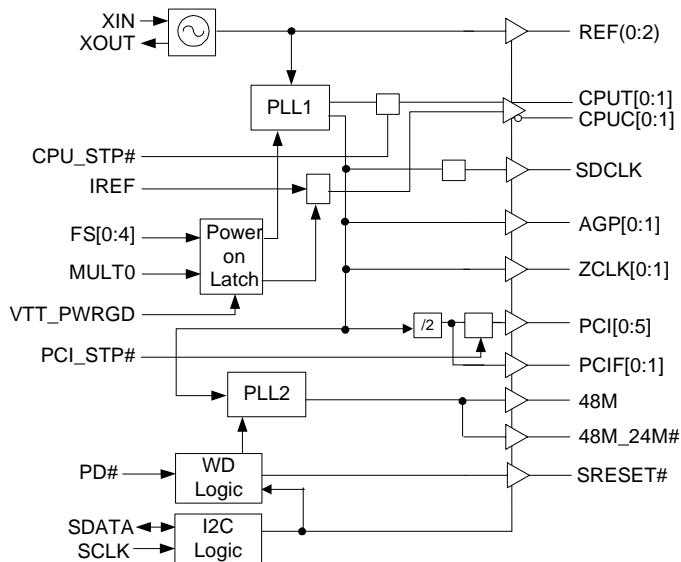
# High-Performance SiS645DX/648DX/650/651 Intel Pentium® 4 Clock Synthesizer

## Features

- Supports Pentium® 4-type CPUs
- 3.3V power supply
- Eight copies of PCI clocks
- One 48-MHz USB clock
- Two copies of ZCLK clocks
- One 48-MHz/24-MHz Programmable SIO clock
- Two differential CPU clock pairs

- SMBus support with readback capabilities
- Spread Spectrum electromagnetic interference (EMI) reduction
- Dial-A-Frequency® features
- Dial-A-Ratio™ features
- Dial-A-dB™ features
- 48-pin SSOP Package
- Watchdog function

## Block Diagram



## Pin Configuration<sup>[1]</sup>

VDDR	1	●	VDDSD
**FS0/REF0	2		SDCLK
**FS1/REF1	3		VSSSD
**FS2/REF2	4		CPU_STP#*
VSSR	5		CPUT1
XIN	6		CPUC1
XOUT	7		VDDC
VSSZ	8		VVSC
ZCLK0	9		CPUT0
ZCLK1	10		CPU0
VDDZ	11		IREF
*SRESET#/PCI_STP#	12		VSSA
VDDP	13		VDDA
**FS3/PCIF0	14		SCLK
**FS4/PCIF1	15		SDATA
PC10	16		PD#/VTT_PWRGD*
PC11	17		VSSAGP
VSSP	18		AGP0
VDDP	19		AGP1
PC12	20		VDDAGP
PC13	21		VDD48M
PC14	22		48M
PC15	23		24.48M/MULT0*
VSSP	24		VSS48M

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### Note:

1. Pins marked with [\*] have internal 150K pull-up resistors. Pins marked with [\*\*] have internal 150K pull-down resistors.

**Pin Description<sup>[2]</sup>**

Pin	Name	PWR	I/O	Description
6	XIN		I	<b>Oscillator Buffer Input.</b> Connect to a crystal or to an external clock.
7	XOUT	VDDR	O	Oscillator Buffer Output. Connect to a crystal. Do not connect when an external clock is applied at XIN.
40,44	CPU[0:1]	VDDC	O	<b>“True” Host Output Clocks.</b> See <i>Table 1</i> for frequencies and functionality.
39,43	CPUC[0:1]	VDDC	O	<b>“Complementary” Host Output Clocks.</b> See <i>Table 1</i> for frequencies and functionality.
16,17,20,23	PCI [0:5]	VDDP	O	<b>PCI Clock Outputs.</b> See <i>Table 1</i> .
14	FS3/PCIF0	VDDP	I/O PD	<b>Power-on Bidirectional Input/Output.</b> At power-up, FS3 is the input. When VTT_PWRGD transitions to a logic high, FS3 state is latched and this pin becomes PCIF0 Clock Output. See <i>Table 1</i> .
15	FS4/PCIF1	VDDP	I/O PD	<b>Power-on Bidirectional Input/Output.</b> At power-up, FS4 is the input. When VTT_PWRGD transitions to a logic high, FS4 state is latched and this pin becomes PCIF1 Clock Output. See <i>Table 1</i> .
2	FS0/REF0	VDDR	I/O PD	<b>Power-on Bidirectional Input/Output.</b> At power-up, FS0 is the input. When VTT_PWRGD transitions to a logic high, FS0 state is latched and this pin becomes REF0, buffered Output copy of the device's XIN clock.
3	FS1/REF1	VDDR	I/O PD	<b>Power-on Bidirectional Input/Output.</b> At power-up, FS1 is the input. When VTT_PWRGD is transited to logic low, FS1 state is latched and this pin becomes REF1, buffered Output copy of the device's XIN clock.
4	FS2/REF2	VDDR	I/O PD	<b>Power-on Bidirectional Input/Output.</b> At power-up, FS2 is the input. When VTT_PWRGD is transited to logic low, FS2 state is latched and this pin becomes REF2, buffered Output copy of the device's XIN clock.
38	IREF		I	<b>Current Reference Programming Input for CPU Buffers.</b> A resistor is connected between this pin and VSS. See <i>Figure 9</i> .
33	PD#/ VTT_PRGD	VDDAGP	I PU	<b>Power-down Input/VTT Power Good Input.</b> At power-up, VTT_PWRGD is the input. When this input is transitions initially from low to high, the FS (0:4) and MULT0 are latched. After the first low to high transition, this pin become a PD# input with an internal pull-up. When PD# is asserted low, the device enters power down mode. See power management function.
27	48M	VDD48M	O	<b>Fixed 48MHz USB Clock Output.</b>
26	24_48M/ MULT0	VDD48M	I/O PU	<b>Power-on Bidirectional Input/Output.</b> At power-up, MULT0 is the input. When VTT_PWRGD is transited to logic low, MULT0 state is latched and this pin becomes 24_48M, SIO programmable clock output.
9,10	ZCLK (0:1)	VDDZ	O	<b>HyperZip Clock Outputs.</b> See <i>Table 1</i> .
34	SDATA	VDDAGP	I/O	<b>Serial Data Input.</b> Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
35	SCLK	VDDAGP	I	<b>Serial Clock Input.</b> Conforms to the SMBus specification.
12	SRESET#	VDDZ	O	<b>PCI Clock Disable Input.</b> If Byte12 Bit7 = 0, this pin becomes an SRESET# open drain output, and the internal pulled up is not active. See system reset description.
	PCI_STP#	VDDZ	I PU	<b>System Reset Control Output.</b> If Byte12 Bit7 = 1 (Default), this pin becomes PCI Clock Disable Input. When PCI_STP# is asserted low, PCI (0:5) clocks are synchronously disabled in a low state. This pin does not affect PCIF (0:1) if they are programmed to be free-running clocks via the device's SMBus interface.
45	CPU_STP#	VDDSD	I PU	<b>CPU Clock Disable Input.</b> When asserted low, CPU (0:1)T clocks are synchronously disabled in a high state and CPU (0:1)C clocks are synchronously disabled in a low state.
47	SDCLK	VDDSD	O	<b>SDRAM Clock Output.</b>
30,31	AGP (0:1)	VDDAGP	O	<b>AGP Clock Outputs.</b> See <i>Table 1</i> for frequencies and functionality.

**Note:**

2. PU = internal pull-up. PD = internal pull-down. T = Tri-level logic input with valid logic voltages of LOW =<0.8V, T = 1.0 -1.8V and HIGH => 2.0V.

**Pin Description<sup>[2]</sup> (continued)**

Pin	Name	PWR	I/O	Description
48	VDDSD		PWR	<b>3.3V Power Supply for SDRAM Clock Output.</b>
29	VDDAGP		PWR	<b>3.3V Power Supply for AGP Clock Outputs.</b>
11	VDDZ		PWR	<b>3.3V Power Supply for HyperZip Clock Outputs.</b>
1	VDDR		PWR	<b>3.3V Power Supply for REF Clock Outputs.</b>
13,19	VDDP		PWR	<b>3.3V Power Supply for PCI Clock Outputs.</b>
42	VDDC		PWR	<b>3.3V Power Supply for CPU Clock Outputs.</b>
28	VDD48M		PWR	<b>3.3V Power Supply for 48-MHz/24-MHz Clock Outputs.</b>
36	VDDA		PWR	<b>3.3V Analog Power Supply.</b>
18,24	VSSP		PWR	<b>GND for PCI Clocks Outputs.</b>
41	VSSC		PWR	<b>GND for CPU Clocks Outputs.</b>
8	VSSZ		PWR	<b>GND for HyperZip Clock Outputs.</b>
25	VSS48M		PWR	<b>GND for 48-MHz/24-MHz Clock Outputs.</b>
5	VSSR		PWR	<b>GND for REF Clock Outputs.</b>
46	VSSSD		PWR	<b>GND for SDRAM Clock Output.</b>
32	VSSAGP		PWR	<b>GND for AGP Clock Outputs.</b>
37	VSSA		PWR	<b>GND for Analog.</b>

**Table 1. Frequency Table**

FS(4:0)	CPU(MHz)	SDRAM(MHz)	ZCLK(MHz)	AGP(MHz)	PCI(MHz)	VCO(MHz)
00000	100.2	100.2	80.2	66.8	33.4	400.8
00001	100.2	133.6	80.2	66.8	33.4	400.8
00010	100.2	200.4	80.2	66.8	33.4	400.8
00011	100.2	167.0	83.5	62.6	31.3	501.0
00100	133.6	100.2	80.2	66.8	33.4	400.8
00101	133.6	133.6	80.2	66.8	33.4	400.8
00110	133.6	200.4	80.2	66.8	33.4	400.8
00111	133.6	167.0	83.5	66.8	33.4	668.0
01000	166.7	100.0	83.4	62.5	31.3	500.1
01001	166.7	133.4	83.4	66.7	33.3	666.8
01010	166.7	222.3	83.4	66.7	33.3	666.8
01011	166.7	166.7	83.4	66.7	33.3	666.8
01100	200.1	100.0	80.0	66.7	33.3	400.1
01101	200.1	133.4	80.0	66.7	33.3	400.1
01110	200.1	200.1	80.0	66.7	33.3	400.1
01111	200.1	150.0	75.0	66.7	33.3	600.2
10000	100.2	100.2	133.6	66.8	33.4	400.8
10001	100.2	133.6	133.6	66.8	33.4	400.8
10010	100.2	200.4	133.6	66.8	33.4	400.8
10011	100.2	167.0	125.3	62.6	31.3	501.0
10100	133.6	100.2	133.6	66.8	33.4	400.8
10101	133.6	133.6	133.6	66.8	33.4	400.8
10110	133.6	200.4	133.6	66.8	33.4	400.8
10111	133.6	167.0	133.6	66.8	33.4	668.0
11000	166.7	100.0	125.0	62.5	31.3	500.1

**Table 1. Frequency Table (continued)**

FS(4:0)	CPU(MHz)	SDRAM(MHz)	ZCLK(MHz)	AGP(MHz)	PCI(MHz)	VCO(MHz)
11001	166.7	133.4	133.4	66.7	33.3	666.8
11010	166.7	222.3	133.4	66.7	33.3	666.8
11011	166.7	166.7	133.4	66.7	33.3	666.8
11100	200.1	100.0	133.4	66.7	33.3	400.1
11101	200.1	133.4	133.4	66.7	33.3	400.1
11110	200.1	200.1	133.4	66.7	33.3	400.1
11111	200.1	150.0	120.0	66.7	33.3	600.2

### Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

### Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 2. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

**Table 3. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N-1) – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	56	Acknowledge
....	Acknowledge from slave	....	Data bytes from slave/Acknowledge

**Table 3. Block Read and Block Write Protocol (continued)**

....	Stop	....	Data byte N from slave – 8 bits
		....	Not Acknowledged
		....	Stop

**Table 4. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

Since SDR and DDR Zero Delay Buffers, will share this same address, this device starts from Byte 4.

**Byte 4: CPU Clock Register**

Bit	@Pup	Name	Description
7	H/W Setting	FS3	For selecting frequencies in <i>Table 1</i>
6	H/W Setting	FS2	For selecting frequencies in <i>Table 1</i>
5	H/W Setting	FS1	For selecting frequencies in <i>Table 1</i>
4	H/W Setting	FS0	For selecting frequencies in <i>Table 1</i>
3	0	SW/HW Frequency Setting Selection	If this bit is programmed to a "1", it enables writes to bits (7:4, 2) for selecting the frequency via software (SMBus) If this bit is programmed to a "0" it enables only reads of bits (7:4, 2), which reflect the hardware setting of FS(0:4).
2	H/W Setting	FS4	For selecting frequencies in <i>Table 1</i>
1	1	SSCG	Spread Spectrum Enable. 0 = Spread Off, 1 = Spread On. This is a Read and Write control bit.
0	0		Master Output Control. 0 = running, 1 = three-state all outputs

**Byte 5: CPU Clock Register**

Bit	@Pup	Name	Description
7	0		Reserved
6	0		Reserved
5	X	MULT0	MULT0 (pin 26) Value. This bit is Read-Only
4	X	FS4	FS4 read back. This bit is Read-Only
3	X	FS3	FS3 read back. This bit is Read-Only.

**Byte 5: CPU Clock Register (continued)**

Bit	@Pup	Name	Description
2	X	FS2	FS2 read back. This bit is Read-Only.
1	X	FS1	FS1 read back. This bit is Read-Only.
0	X	FS0	FS0 read back. This bit is Read-Only.

**Byte 6: CPU Clock Register**

Bit	@Pup	Name	Description
7	0		Function Test Bit, always program to 0.
6	0		Reserved
5	0	PCIF0	PCI_STP# control of PCIF0. 0 = Free-Running, 1 = Stopped when PCI_STP# is LOW.
4	0	PCIF1	PCI_STP# control of PCIF1. 0 = Free-Running, 1 = Stopped when PCI_STP# is LOW.
3	1	CPU[T/C]0	Controls CPUT0 and CPUC0 functionality when CPU_STP# is asserted LOW 0 = Free-Running, 1 + Stopped with CPU_STP# asserted LOW This is a Read and Write Control bit.
2	0	CPU[T/C]1	Controls CPUT1 and CPUC1 functionality when CPU_STP# is asserted LOW 0 = Free-Running, 1 Stopped with CPU_STP# asserted to LOW This is a Read and Write Control Bit.
1	1	CPU0T/C	CPUT0, CPUC0 Output Control, 1 = enabled, 0 = disabled. This is a Read and Write Control bit.
0	1	CPU1T/C	CPUT1, CPUC1 Output Control, 1 = enabled, 0 = disabled. This is a Read and Write Control bit.

**Byte 7: PCI Clock Register**

Bit	@Pup	Name	Description
7	1	PCIF0	PCIF0 Output Control 1 = enabled, 0 = forced LOW
6	1	PCIF1	PCIF1 Output Control 1 = enabled, 0 = forced LOW
5	1	PCI5	PCI5 Output Control 1 = enabled, 0 = forced LOW
4	1	PCI4	PCI4 Output Control 1 = enabled, 0 = forced LOW
3	1	PCI3	PCI3 Output Control 1 = enabled, 0 = forced LOW
2	1	PCI2	PCI2 Output Control 1 = enabled, 0 = forced LOW
1	1	PCI1	PCI1 Output Control 1 = enabled, 0 = forced LOW
0	1	PCI0	PCI0 Output Control 1 = enabled, 0 = forced LOW

**Byte 8: Silicon Signature Register**

Bit	@Pup	Description
7	1	Vendor ID 1000 = Cypress
6	0	
5	0	
4	0	
3	0	Revision ID
2	0	
1	0	
0	0	

**Byte 9: Peripheral Control Register**

Bit	@Pup	Name	Description
7	1	PD#	PD# Enable. 0 = enable, 1 = disable
6	0	PD# output control	0 = when PD# is asserted LOW, CPU(0:1) stop in a high state, CPUC[0:1] stop in a low state. 1 = when PD# is asserted LOW, CPUT[0:1] and CPUC[0:1] stop in H-Z.
5	1	48M	48M Output Control 1 = enabled, 0 = forced LOW
4	1	48M_24M	48M_24M Output Control 1 = enabled, 0 = forced LOW
3	0	48M_24M	48M_24M, 0 = pin28 output is 24 MHz, 1 = pin26 output is 48 MHz.
2	0	SS2	SS2 Spread Spectrum control bit (0 = down spread, 1 = center spread)
1	0	SS1	SS1 Spread Spectrum control bit. See Table 5.
0	0	SS0	SS0 Spread Spectrum control bit. See Table 5.

**Table 5. Spread Spectrum**

SS2	SS1	SS0	Spread Mode	Spread%
0	0	0	Down	-0.50
0	0	1	Down	-0.75
0	1	0	Down	-1.00
0	1	1	Down	-1.50
1	0	0	Center	+0.25, -0.25
1	0	1	Center	+0.37, -0.37
1	1	0	Center	+0.50, -0.50
1	1	1	Center	+0.75, -0.75

**Byte 10: Peripheral Control Register**

Bit	@Pup	Name	Description
7	1	SDCLK	SDCLK Output Enable 1 = enabled, 0 = disabled
6	1	REF2	REF2 Output Control 1 = enabled, 0 = forced LOW
5	1	REF1	REF1 Output Control 1 = enabled, 0 = forced LOW
4	1	REF0	REF0 Output Control 1 = enabled, 0 = forced LOW
3	1	ZCLK1	ZCLK1 Output Enable 1 = enabled, 0 = disabled
2	1	ZCLK0	ZCLK0 Output Enabled 1 = enabled, 0 = disabled
1	1	AGP1	AGP1 Output Enabled 1 = enabled, 0 = disabled
0	1	AGP0	AGP0 Output Enabled 1 = enabled, 0 = disabled

**Byte 11: Dial-a-Skew™ and Dial-a-Ratio Control Register**

Bit	@Pup	Name	Description
7	0	DARZCK2	Programming these bits allow modifying the frequency ratio of the ZCLK clock relative to the VCO. See Table 6.
6	0	DARZCK1	
5	0	DARZCK0	
4	0	DARAG2	Programming these bits allow modifying the frequency ratio of the AGP(1:0), PCI(5:0) and PCIF(0:1) clocks relative to the VCO. See Table 7
3	0	DARAG1	
2	0	DARAG0	
1	0	DASSD1	Programming these bits allow shifting skew between CPU and SDCLK signals. See Table 8.
0	0	DASSD0	

**Table 6. Dial-a-Ratio for ZCLK**

DARZCK(2:0)	VC0/ZCLK Ratio
000	Frequency Selection Default

**Table 6. Dial-a-Ratio for ZCLK (continued)**

001	2
010	3
011	4
100	5
101	6
110	8
111	9

**Table 7. Dial-a-Ratio for AGP(0:1)<sup>[3]</sup>**

DARAG(2:0)	VC0/AGP Ratio
000	Frequency Selection Default
001	6
010	7
011	8
100	9
101	10
110	10
111	10

**Table 8. Dial-a-Skew SDCLK CPU**

DASSD(1:0)	SDCLK-CPU Skew
00	0ps (Default) <sup>[4]</sup>
01	+150ps (CPU lag)*
10	+300ps (CPU lag)*
11	+450ps (CPU lag)*

**Byte 12: Watchdog Time Stamp Register**

Bit	@Pup	Name	Description
7	1	SRESET#/PCI_STP#/ PCI_STP# Selection	SRESET#/PCI_STP#. 1 = Pin 12 is the input pin as PCI_STP# signal. 0 = Pin 12 is the output pin as SRESET# signal.
6	0		Frequency Revert. This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only. 0 = selects frequency of existing H/W setting1 = selects frequency of the second to last S/W setting. (the software setting prior to the one that caused a system reboot).
5	0		WDTEST. For WD-Test, ALWAYS program to '0'
4	0		WD Alarm. This bit is set to "1" when the Watchdog times out. It is reset to "0" when the system clears the WD time stamps (WD3:0).
3	0	WD3	This bits selects the Watchdog Time Stamp Value. See Table 9
2	0	WD2	
1	0	WD1	
0	0	WD0	

**Notes:**

3. The ratio of AGP to PCI is retained at 2:1.
4. See *Figure 9* for CPU test measurement point. See *Figure 10* for SDCLK test measurement point.

**Table 9. Watchdog Time Stamp Table**

WD(3:0)	FUNCTION
0000	Off
0001	1 second
0010	2 seconds
0011	3 seconds
0100	4 seconds
0101	5 seconds
0110	6 seconds
0111	7 seconds
1000	8 seconds
1001	9 seconds
1010	10 seconds
1011	11 seconds
1100	12 seconds
1101	13 seconds
1110	14 seconds
1111	15 seconds

**Byte 13: Dial-a-Frequency Control Register N (all bits are read- and write-functional)<sup>[5]</sup>**

Bit	@Pup	Description
7	0	Reserved
6	0	N6, MSB
5	0	N5
4	0	N4
3	0	N3
2	0	N2
1	0	N3
0	0	N0, LSB

**Byte 14: Dial-a-Frequency Control Register R (all bits are read- and write-functional)<sup>[5, 6]</sup>**

Bit	@Pup	Description
7	0	Reserved
6	0	R5 MSB
5	0	R4
4	0	R3
3	0	R2
2	0	R1
1	0	R0, LSB
0	0	R and N register mux selection. 0 = R and N values come from the ROM. 1 = data is loaded from the Dial-a-Frequency registers into R and N.

**Notes:**

5. Byte 13 and Byte 14 should be written together in every case.
6. The range of R = (20...60), The range of N = (21...125) and N > R > N/2.

## Dial-A-Frequency Feature

SMBus Dial-A-frequency feature is available in this device via Byte13 and Byte14. P is a large value PLL constant that depends on the frequency selection achieved through the hardware selectors (FS4, FS0). P value may be determined from the following table.

**Table 10.**

FS(4:0)	P
00100, 00101, 00110, 01000, 01111, 10100, 10101, 10110, 11000, 11111	127994666.7
00000, 00001, 00010, 01001, 01010, 01011, 10000, 10001, 10010, 11001, 11010, 11011	95996000
00011, 00111, 10011, 10111	76796800
01100, 01101, 01110, 11100, 11101, 11110	191992000

### Dial-A-Frequency Formula

$F_{CPU} = (P * N) / R$  and Range of R = (20..60), Range of N = (21..125) where N > R > N/2.

For a more detail programming guide, please refer to Cypress "genapp.pfd" file AN-0025.

### Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing EMI radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control Bytes. See the SMBus register section of this data sheet for the exact bit and byte functionally. The following table is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

### PD# (Power-down) Clarification

The PD# (Power-down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is low, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low 'stopped' state.

### PD# – Assertion

When PD# is sampled low by two consecutive rising edges of CPUC clock then all clock outputs (except CPUT) clocks must be held low on their next high to low transition. CPUT clocks must be held with CPUT clock pin driven high with a value of 2x Iref and CPUC undriven.

Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete

### PD# Deassertion

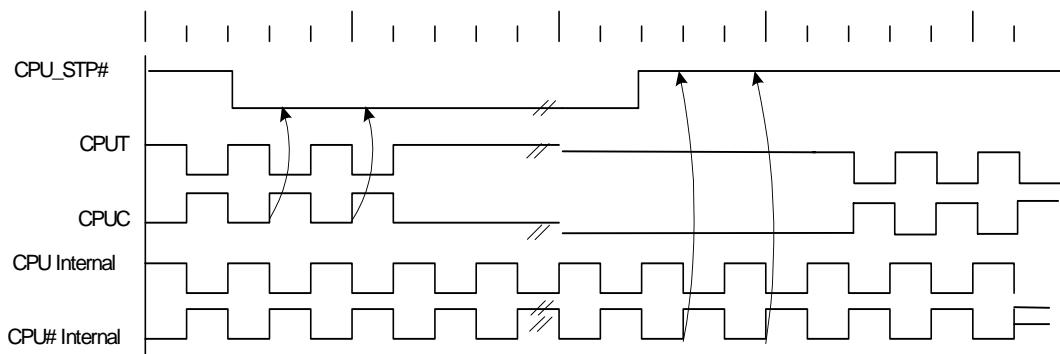
The power-up latency between PD# rising to a valid logic '1' level and the starting of all clocks is less than 3.0 ms.

### CPU\_STP# Clarification

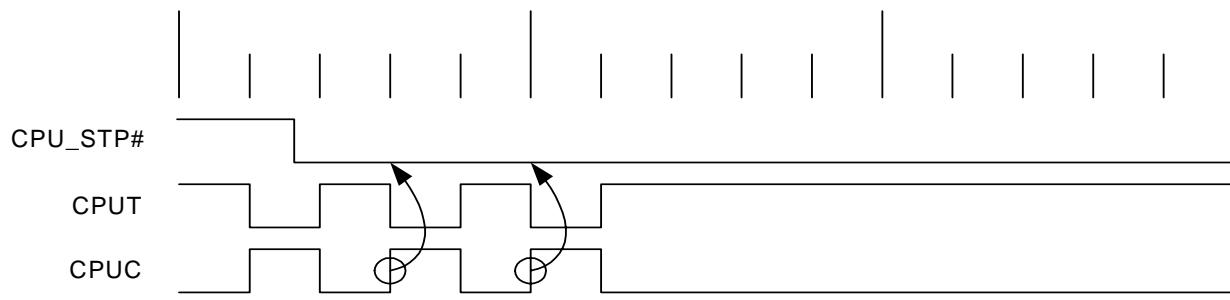
The CPU\_STP# signal is an active low input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function.

### CPU\_STP# Assertion

When CPU\_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU\_STP# will be stopped after being sampled by two falling CPU clock edges. The final state of the stopped CPU signals is CPU = HIGH and CPUC0 = LOW. There is no change to the output drive current values during the stopped state. The CPU is driven HIGH with a current value equal to (Mult 0 'select') x (Iref), and the CPUC signal will not be driven. Due to external pull-down circuitry CPUC will be LOW during this stopped state.



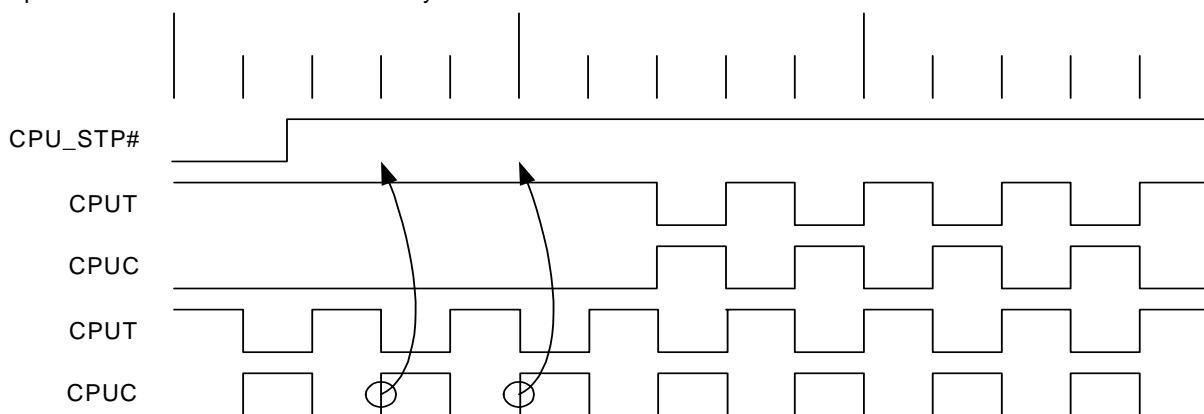
**Figure 1. Power-down Assertion/Deassertion Timing Waveforms – Nonbuffered Mode**



**Figure 2. Assertion CPU\_STP# Waveforms**

#### **CPU\_STP# Deassertion**

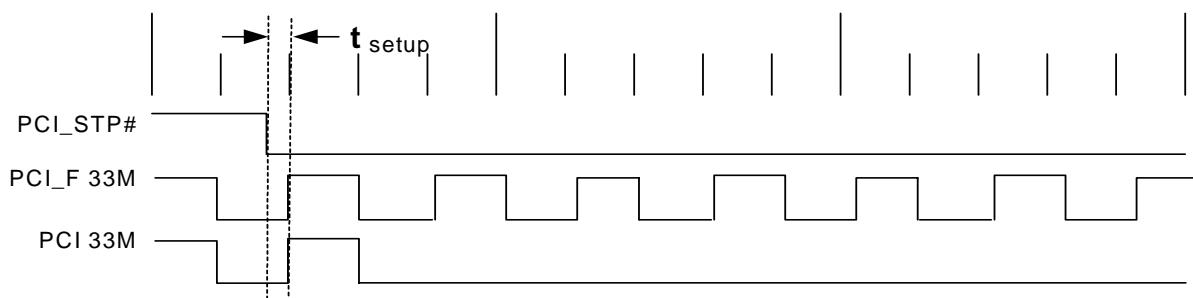
The de-assertion of the CPU\_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produced when the clock resumes. The maximum latency from the Deassertion to active outputs is no more than two CPU clock cycles.



**Figure 3. Deassertion CPU\_STP# Waveforms**

#### **PCI\_STP# Assertion**

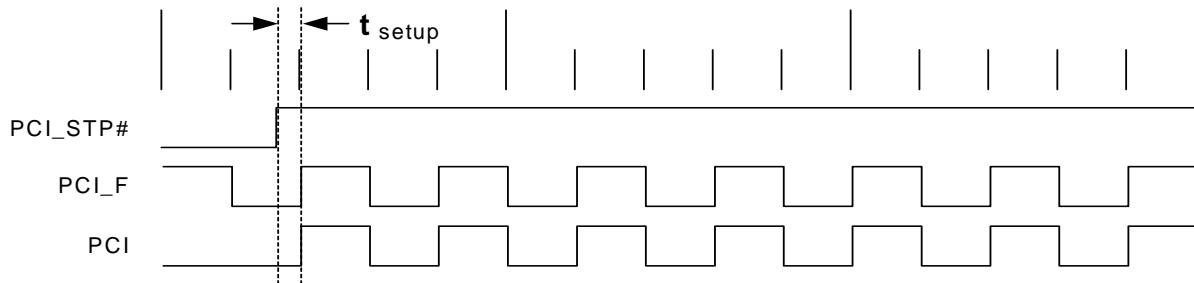
The PCI\_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI\_STP# going LOW is 10 ns ( $t_{setup}$ ). (See Figure 4.) The PCIF (clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free running.



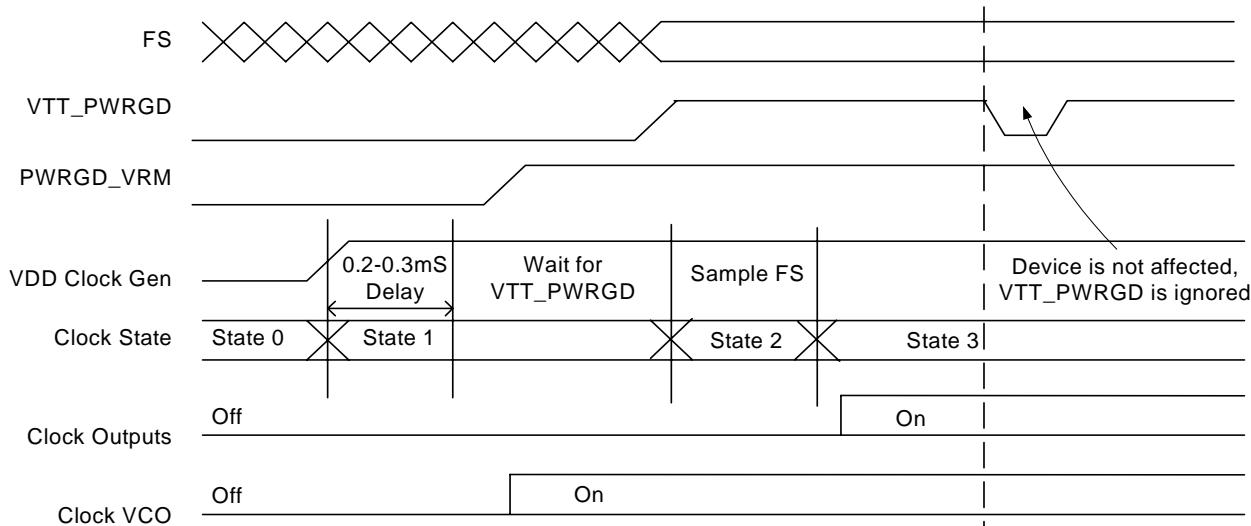
**Figure 4. Assertion PCI\_STP# Waveforms**

### PCI\_STP# Deassertion

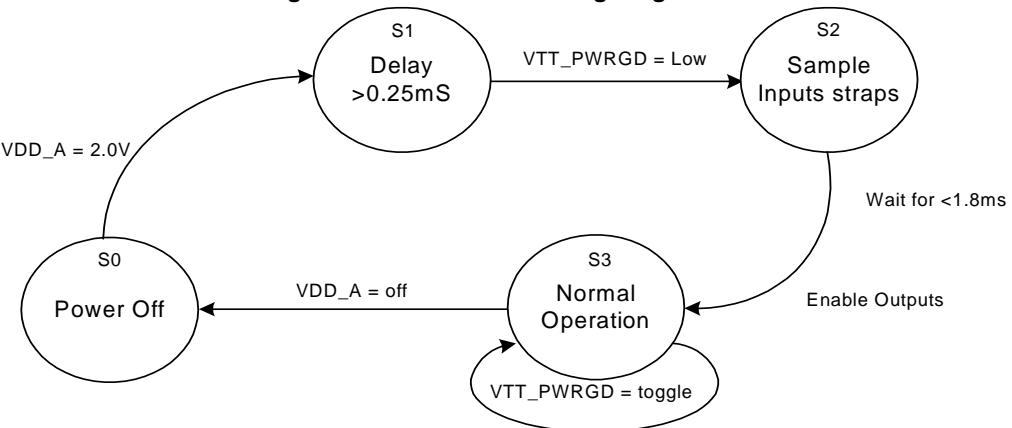
The deassertion of the PCI\_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI\_STP# transitions to a high level.



**Figure 5. Deassertion PCI\_STP# Waveforms<sup>[7]</sup>**



**Figure 6. VTT\_PWRGD Timing Diagram**



**Figure 7. Clock Generator Power-up/Run State Diagram**

#### Note:

7. The PCI STOP function is controlled by two inputs. One is the device PCI\_STP# pin number 34 and the other is SMBus byte 0 bit 3. These two inputs are logically ANDed. If either the external pin or the internal SMBus register bit is set low then the stoppable PCI clocks will be stopped in a logic low state. Reading SMBus Byte 0 Bit 3 will return a 0 value if either of these control bits are set LOW thereby indicating the device's stoppable PCI clocks are not running.

## Watchdog Self-Recovery Sequence

This feature is designed to allow the system designer to change frequency while the system is running and reboot the operation of the system in case of a hang up due to the frequency change.

When the system sends an SMBus command requesting a frequency change through the Dial-a-Frequency Control Registers, it must have previously sent a command to the Watchdog Timer to select which time out stamp the Watchdog must perform, otherwise the System Self-recovery feature will not be applicable. Consequently, this device will change frequency and then the Watchdog timer starts timing.

Meanwhile, the system BIOS is running its operation with the new frequency. If this device receives a new SMBus command to clear the bits originally programmed in the Watchdog Timer bits (reprogram to 0000) before the Watchdog times out, then this device will keep operating in its normal condition with the new selected frequency.

The Watchdog timer will also be triggered if you program the software frequency select bits (FSEL) to a new frequency selection. If the Watchdog times out before the new SMBus reprograms the Watchdog Timer bits to (0000), then this device will send a low system reset pulse, on SRESET# and changes WD Time-out bit to "1."

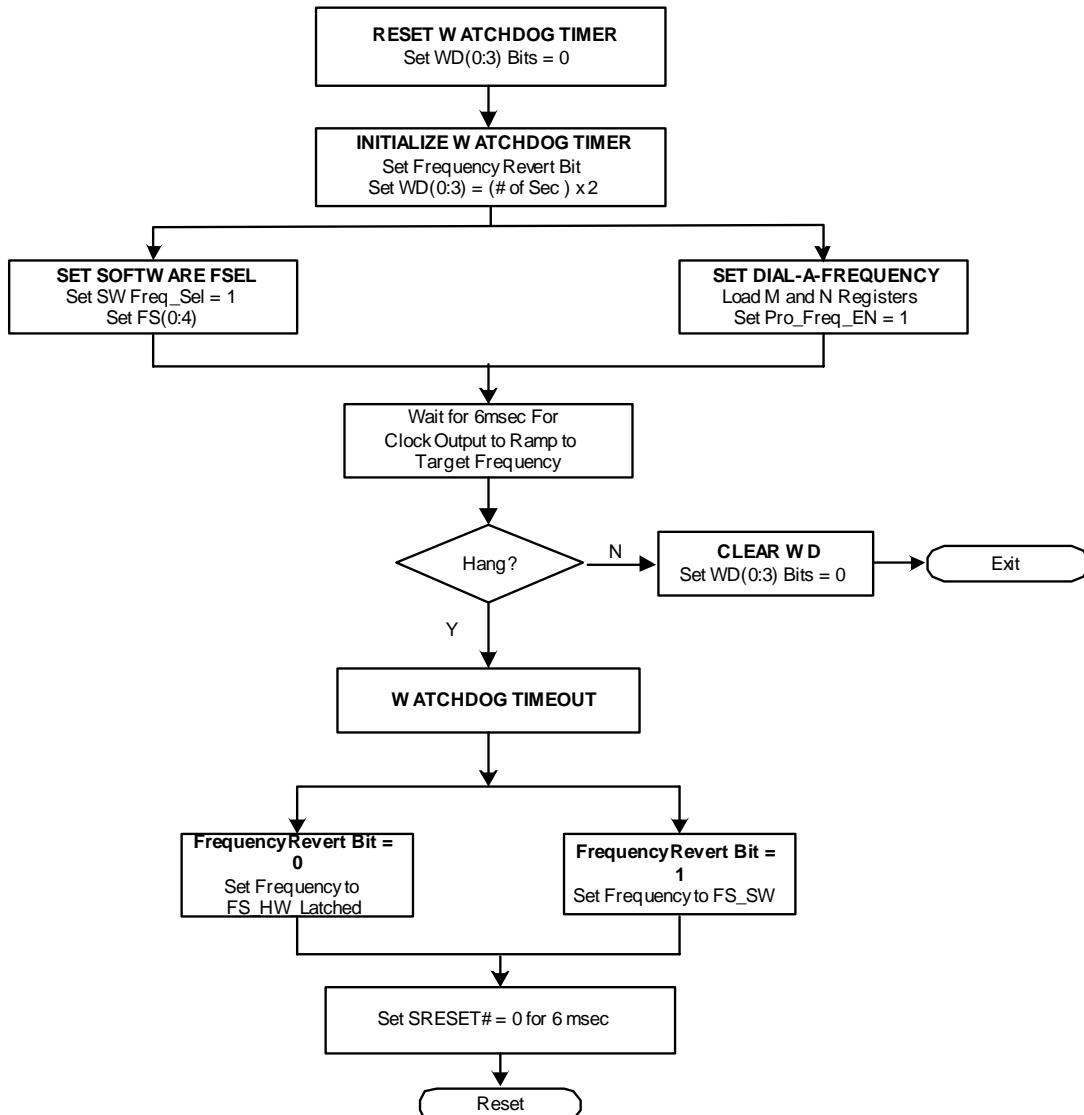


Figure 8. Watchdog Self-recovery Sequence Flowchart

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD}$	Core Supply Voltage		-0.5	4.6	V
$V_{DDA}$	Analog Supply Voltage		-0.5	4.6	V
$V_{IN}$	Input Voltage	Relative to $V_{SS}$	-0.5	$V_{DD} + 0.5$	VDC
$T_S$	Temperature, Storage	Non Functional	-65	+150	°C
$T_A$	Temperature, Operating Ambient	Functional	0	70	°C
$T_J$	Temperature, Junction	Functional	-	150	°C
$ESD_{HBM}$	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	-	V
$\emptyset_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	15		°C/W
$\emptyset_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	45		°C/W
UL-94	Flammability Rating	At 1/8 in.		V-0	
MSL	Moisture Sensitivity Level		1		

**Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DDSD}$ , $V_{DDAGP}$ , $V_{DDZ}$ , $V_{DDR}$ , $V_{DDP}$ , $V_{DDC}$ , $V_{DD48M}$ , $V_{DDA}$	3.3V Operating Voltage	$3.3V \pm 5\%$	3.135	3.465	V
$V_{ILI2C}$	Input Low Voltage	SDATA, SCLK	-	-	1.0
$V_{IHI2C}$	Input High Voltage	SDATA, SCLK	2.2	-	-
$V_{IL}$	Input Low Voltage		$V_{SS} - 0.5$	0.8	V
$V_{IH}$	Input High Voltage		2.0	$V_{DD} + 0.5$	V
$I_{IL}$	Input Leakage Current	except Pull-ups or Pull downs $0 < V_{IN} < V_{DD}$	-5	5	µA
$V_{OL}$	Output Low Voltage	$I_{OL} = 1 \text{ mA}$	-	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -1 \text{ mA}$	2.4	-	V
$I_{OZ}$	High-Impedance Output Current		-10	10	µA
$C_{IN}$	Input Pin Capacitance		2	5	pF
$C_{OUT}$	Output Pin Capacitance		3	6	pF
$L_{IN}$	Pin Inductance		-	7	nH
$V_{XIH}$	Xin High Voltage		$0.7V_{DD}$	$V_{DD}$	V
$V_{XIL}$	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD}$	Dynamic Supply Current	At 200 MHz and all outputs loaded per <i>Table 11</i> and <i>Figure 7</i>	-	300	mA
$I_{PD}$	Power-down Supply Current	PD# Asserted	-	1	mA
$C_{XTAL}$	Crystal Pin Capacitance	Nominal = 36 pF	30	42	pF

**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
<b>Crystal</b>					
T <sub>DC</sub>	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T <sub>PERIOD</sub>	XIN period	When Xin is driven from an external clock source	69.841	71.000	ns
V <sub>XIH</sub>	Xin High Voltage		0.7V <sub>DD</sub>	V <sub>DD</sub>	V
V <sub>XIL</sub>	Xin Low Voltage		0	0.3V <sub>DD</sub>	V
T <sub>R</sub> / T <sub>F</sub>	XIN Rise and Fall Times	Measured between 0.3V <sub>DD</sub> and 0.7V <sub>DD</sub>	—	10.0	ns
T <sub>CCJ</sub>	XIN Cycle to Cycle Jitter	As an average over 1μs duration	—	500	ps
<b>CPU at 0.7V</b>					
T <sub>DC</sub>	CPUT and CPUC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD100</sub>	100-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	9.8	10.2	ns
T <sub>PERIOD133</sub>	133-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	7.35	7.65	ns
T <sub>SKEW</sub>	Any CPUT/C to CPUT/C Clock Skew	Measured at crossing point V <sub>OX</sub>	—	150	ps
T <sub>CCJ</sub>	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	—	200	ps
T <sub>R</sub> / T <sub>F</sub>	CPUT and CPUC Rise and Fall Times	Measured from Vol = 0.175 to Voh = 0.525V	175	900	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of 2*(T <sub>R</sub> -T <sub>F</sub> )/(T <sub>R</sub> +T <sub>F</sub> )	—	20	%
ΔT <sub>R</sub>	Rise Time Variation		—	125	ps
ΔT <sub>F</sub>	Fall Time Variation		—	125	ps
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		280	430	mv
<b>AGP</b>					
T <sub>DC</sub>	AGP Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	AGP Period	Measured at crossing point V <sub>OX</sub>	15.0	15.3	ns
T <sub>SKEWUN-BUFFERED</sub>	Any AGP to Any AGP Clock Skew	Measurement at 1.5V	—	175	ps
T <sub>R</sub> / T <sub>F</sub>	AGP Rise and Fall Times	Measured from Vol= 0.175 to Voh = 0.525V	0.5	1.6	ns
T <sub>HIGH</sub>	AGP High Time		5.25	—	ns
T <sub>LOW</sub>	AGP Low Time		5.05	—	ns
T <sub>CCJ</sub>	AGP Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	—	500	ps
<b>ZCLK</b>					
T <sub>DC</sub>	ZCLK Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>R</sub> / T <sub>F</sub>	ZCLK Rise and Fall Times	Measured between 0.4V and 2.4V	0.5	1.6	ns
T <sub>SKEW</sub>	Any ZCLK to Any ZCLK Clock Skew	Measurement at 1.5V	—	175	ps
T <sub>CCJ</sub>	ZCLK Cycle to Cycle Jitter	Measurement at 1.5V	—	500	ps
<b>PCI/PCIF</b>					
T <sub>DC</sub>	PCI/PCIF Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	PCIF/PCI Period	Measurement at 1.5V	30.0	30.0	ns
T <sub>HIGH</sub>	PCIF and PCI High Time	Measurement at 2.4V	12.0	—	ns
T <sub>LOW</sub>	PCIF and PCI Low Time	Measurement at 0.4V	12.0	—	ns
T <sub>R</sub> / T <sub>F</sub>	PCIF and PCI Rise and Fall Times	Measured between 0.4V and 2.4V	0.5	2.0	ns
T <sub>SKEW</sub>	Any PCI clock to Any PCI Clock Skew	Measurement at 1.5V	—	500	ps
T <sub>CCJ</sub>	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	—	500	ps
<b>SDCLK</b>					
T <sub>DC</sub>	SDCLK Duty Cycle	Measurement at 1.5V	45	55	%

**AC Electrical Specifications (continued)**

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIOD}$	SDCLK Period	Measurement at 1.5V	7.4	15.0	ns
$T_{HIGH100}$	SDCLK High Time	Measurement at 2.4V	3.0		ns
$T_{HIGH133}$	SDCLK High Time	Measurement at 2.4V	1.87		ns
$T_{LOW100}$	SDCLK Low Time	Measurement at 0.4V	2.8		ns
$T_{LOW133}$	SDCLK Low Time	Measurement at 0.4V	1.67		ns
$T_R / T_F$	SDCLK Rise and Fall Times	Measured between 0.4V and 2.4V	0.4	1.6	ns
$T_{CCJ}$	SDCLK Cycle to Cycle Jitter	Measurement at 1.5V	–	800	ps
<b>48M</b>					
$T_{DC}$	48M Duty Cycle	Measurement at 1.5V	45	55	%
$T_{PERIOD}$	48M Period	Measurement at 1.5V	20.829	20.834	ns
$T_R / T_F$	48M Rise and Fall Times	Measured between 0.4V and 2.4V	1.0	2.0	ns
$T_{CCJ}$	48M Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
<b>24M</b>					
$T_{DC}$	24M Duty Cycle	Measurement at 1.5V	45	55	%
$T_{PERIOD}$	24M Period	Measurement at 1.5V	41.66	41.67	ns
$T_R / T_F$	24M Rise and Fall Times	Measured between 0.4V and 2.4V	1.0	4.0	ns
$T_{CCJ}$	24M Cycle to Cycle Jitter	Measurement at 1.5V	–	800	ps
<b>REF</b>					
$T_{DC}$	REF Duty Cycle	Measurement at 1.5V	45	55	%
$T_{PERIOD}$	REF Period	Measurement at 1.5V	69.841	71.00	ns
$T_R / T_F$	REF Rise and Fall Times	Measured between 0.4V and 2.4V	1.0	4.0	V/ns
$T_{CCJ}$	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
<b>ENABLE/DISABLE and SET-UP</b>					
tpZL, tpZH	Output Enable Delay(all outputs)		1.0	10.0	ns
tpLZ, tpZH	Output Disable Delay (all outputs)		1.0	10.0	ns
$T_{STABLE}$	Clock Stabilization from Power-up		–	1.5	ms
$T_{SS}$	Stopclock Set-up Time		10.0	–	ns
$T_{SH}$	Stopclock Hold Time		0	–	ns

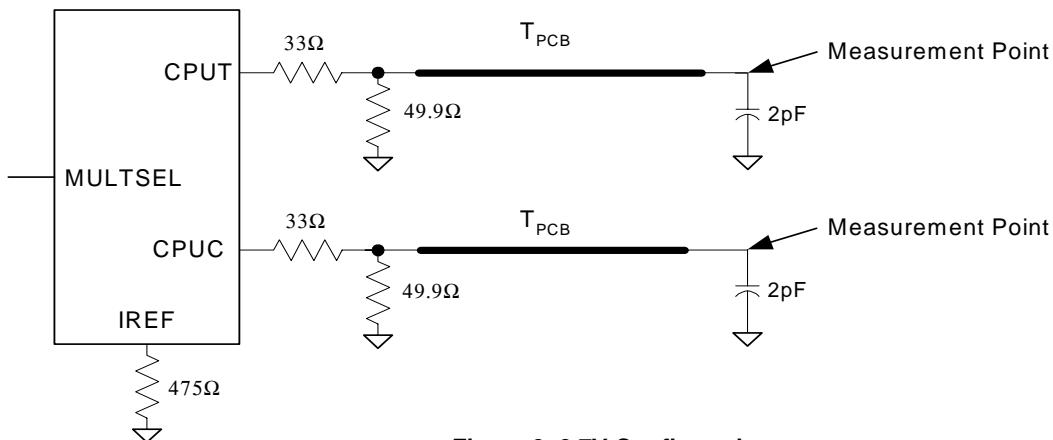
**Table 11. Maximum Lumped Capacitive Output Loads**

Clock	Max Load	Units
PCI, PCIF	30	pF
AGP, SDCLK	30	pF
ZCLK	10	pF
48M_24, 48M Clock	20	pF
REF	30	pF
CPUT,CPUC	2	pF

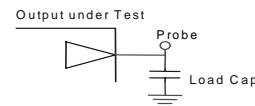
## Test and Measurement Set-up

### For Differential CPU Output Signals

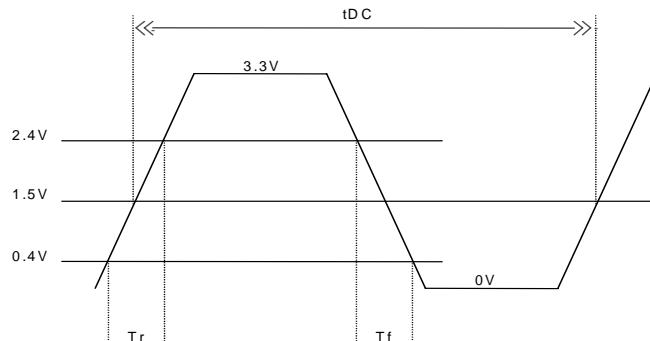
The following diagram shows lumped test load configurations for the differential Host Clock Outputs.



**Figure 9. 0.7V Configuration**



**3.3V signals**



**Figure 10. Lumped Load for Single-Ended Output Signals (for AC Parameters Measurement)**

**Table 12. CPU Clock Current Select Function**

Mult0	Board Target Trace/Term Z	Reference R, Iref – Vdd (3*Rr)	Output Current	Voh @ Z
0	50 Ohms (not used)	Rr = 221 1%, Iref = 5.00mA	Ioh = 4*Iref	1.0V @ 50
1	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6*Iref	0.7V @ 50

**Table 13. Group Timing Relationship and Tolerances**

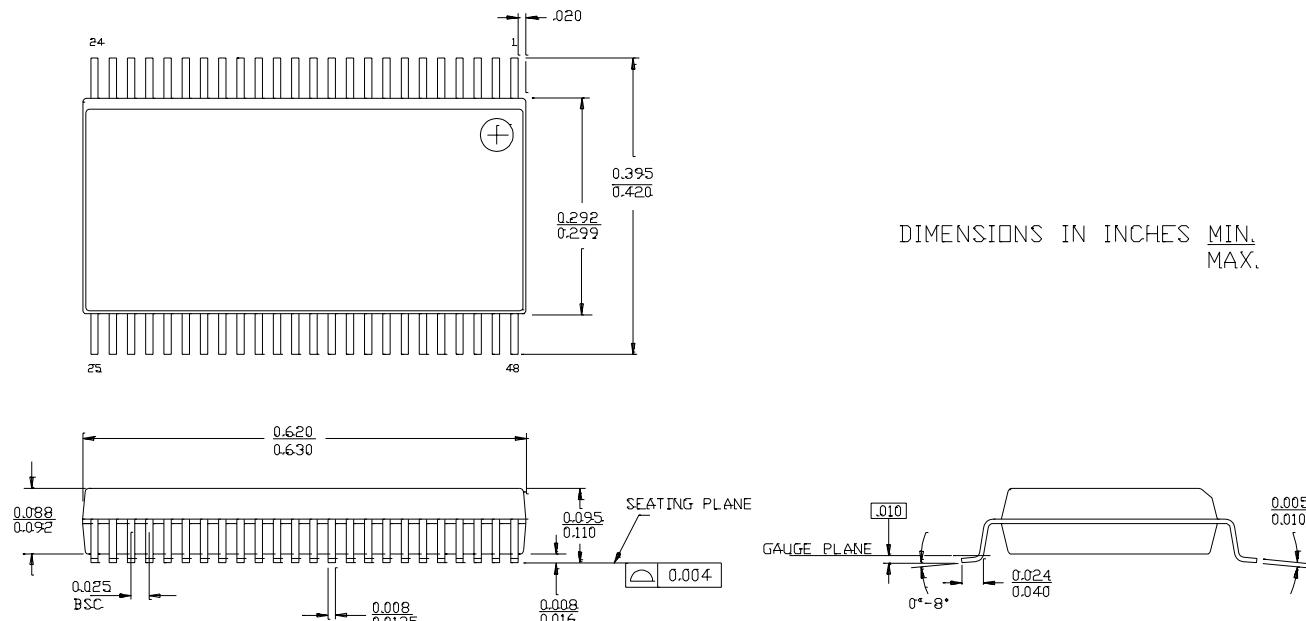
	Offset	Tolerance (or Range)	Conditions	Notes
CPU to SDCLK	Typical 0 ns	±2 ns	CPU leads	See Note 8
CPU to AGP	Typical 2 ns	1–4 ns	CPU leads	See Note 8
CPU to ZCLK	Typical 2 ns	1–4 ns	CPU leads	See Note 8
CPU to PCI	Typical 2 ns	1–4 ns	CPU leads	See Note 8

**Note:**

8. See Figure 9 for CPU clocks measurement point. See Figure 10 for SDCLK, AGP, ZCLK and PCI Outputs measurement point.

**Ordering Information**

Part Number	Package Type	Product Flow
CY28381OC	48-pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
CY28381OCT	48-pin Shrunk Small Outline package (SSOP) – Tape and Reel	Commercial, 0° to 70°C

**Package Drawing and Dimensions**
**48-lead Shrunk Small Outline Package O48**


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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126496	05/23/03	RGL	New Data Sheet