

EV31C3A3A1-74.250M

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REGULATORY COMPLIANCE (Data Sheet downloaded on Feb 18, 2019)


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ITEM DESCRIPTION

Voltage Controlled Quartz Crystal Clock Oscillators VCXO HCMOS/TTL (CMOS) 5.0Vdc 6 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 74.250MHz ± 50 ppm Maximum 0°C to +70°C ± 50 ppm Minimum 10% Typical, 20% Maximum

ELECTRICAL SPECIFICATIONS

Nominal Frequency	74.250MHz
Frequency Tolerance/Stability	± 50 ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, and Vibration.)
Aging at 40°C	± 2 ppm/First year typical, ± 10 ppm/10 Years Maximum
Operating Temperature Range	0°C to +70°C
Supply Voltage	5.0Vdc $\pm 10\%$
Input Current	35mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	5nSec Maximum (Measured at 0.4Vdc to 2.4Vdc with TTL Load; Measured at 20% to 80% of waveform with HCMOS Load)
Duty Cycle	50 ± 10 (%) (Measured at 1.4Vdc with TTL Load; Measured at 50% of waveform with HCMOS Load)
Load Drive Capability	10TTL Load or 30pF HCMOS Load Maximum
Output Logic Type	CMOS
Absolute Pull Range	± 50 ppm Minimum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, Shock, Vibration, and Aging over the Control Voltage (Vc).)
Control Voltage	0.5Vdc to 4.5Vdc (Test condition for Absolute Pull Range)
Control Voltage Range	0.0Vdc to Vdd
Linearity	10% Typical, 20% Maximum
Transfer Function	Positive Transfer Characteristic
Modulation Bandwidth	10kHz Minimum (Measured at -3dB, Vc = 2.5Vdc)
Input Impedance	50kOhms Minimum
Input Leakage Current	10 μ A Maximum
Phase Noise	-70dBc/Hz at offset of 10Hz, -100dBc/Hz at offset of 100Hz, -130dBc/Hz at offset of 1kHz, -147dBc/Hz at offset of 10kHz, -152dBc/Hz at offset of 100kHz, and -155dBc/Hz at offset of 1MHz (Typical Values at Fo = 27MHz)
Tri-State Input Voltage (Vih and Vil)	+0.9Vdd Minimum to Enable Output; +0.1Vdd Maximum to Disable Output (High Impedance); No Connect to Enable Output.
RMS Phase Jitter	1pSec Maximum (Fj = 12kHz to 20MHz)
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A
Gross Leak Test	MIL-STD-883, Method 1014 Condition C
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010



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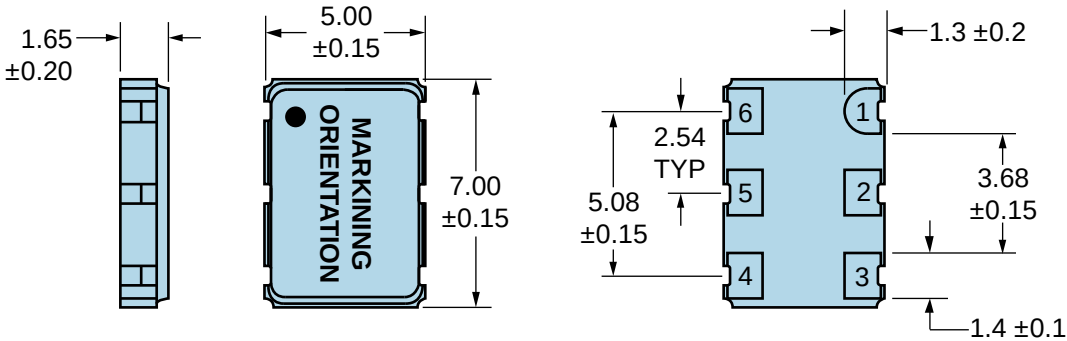
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS CONTINUED

Vibration	MIL-STD-883, Method 2007 Condition A
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MECHANICAL DIMENSIONS (all dimensions in millimeters)

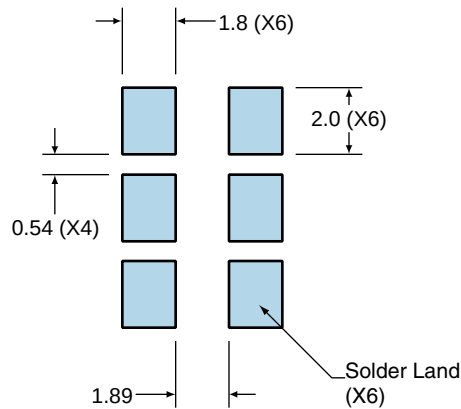


PIN	CONNECTION
1	Voltage Control
2	No Connect
3	Case Ground
4	Output
5	Tri-State
6	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	74.250M
3	XXYYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of Year ZZ=Week of Year

Suggested Solder Pad Layout

All Dimensions in Millimeters

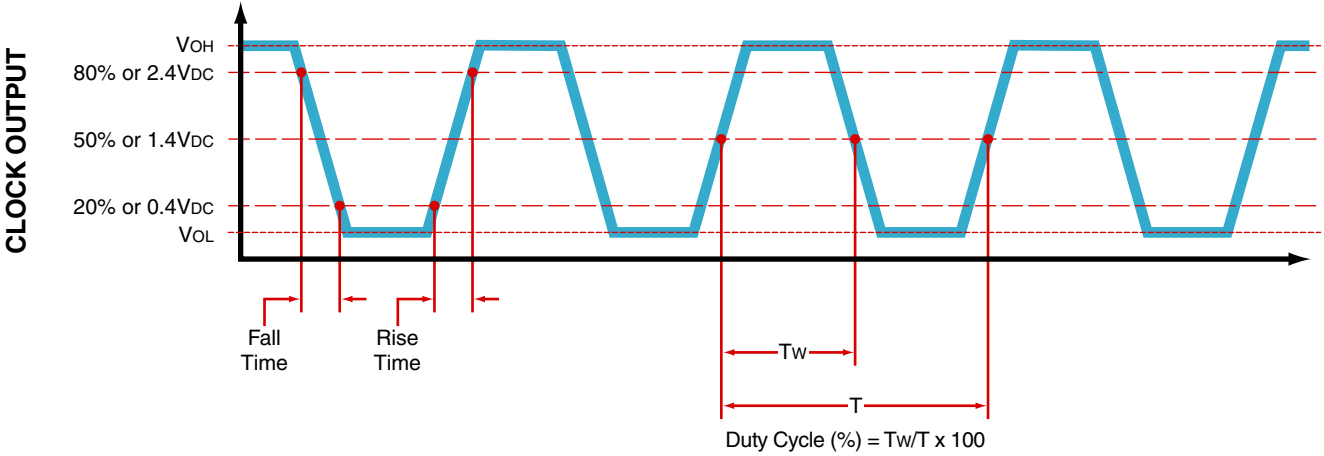


All Tolerances are ±0.1

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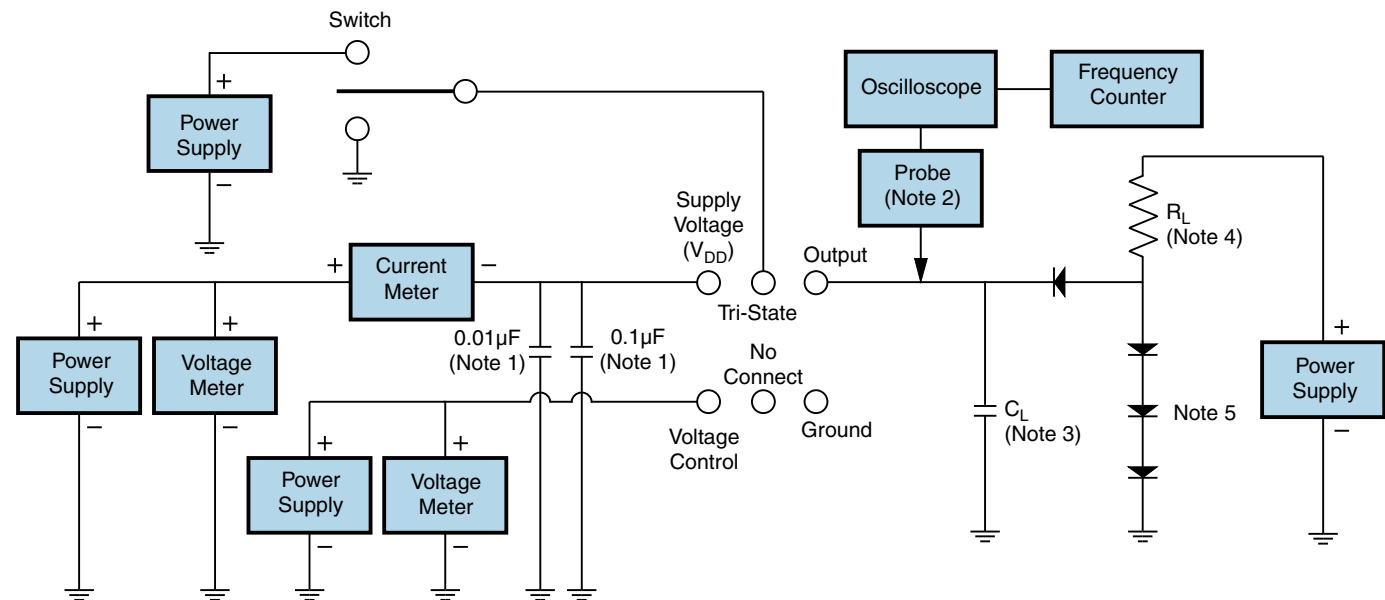
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OUTPUT WAVEFORM



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Test Circuit for TTL Output



- Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.
- Note 4: Resistance value R_L is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.
- Note 5: All diodes are MMBD7000, MMBD914, or equivalent.

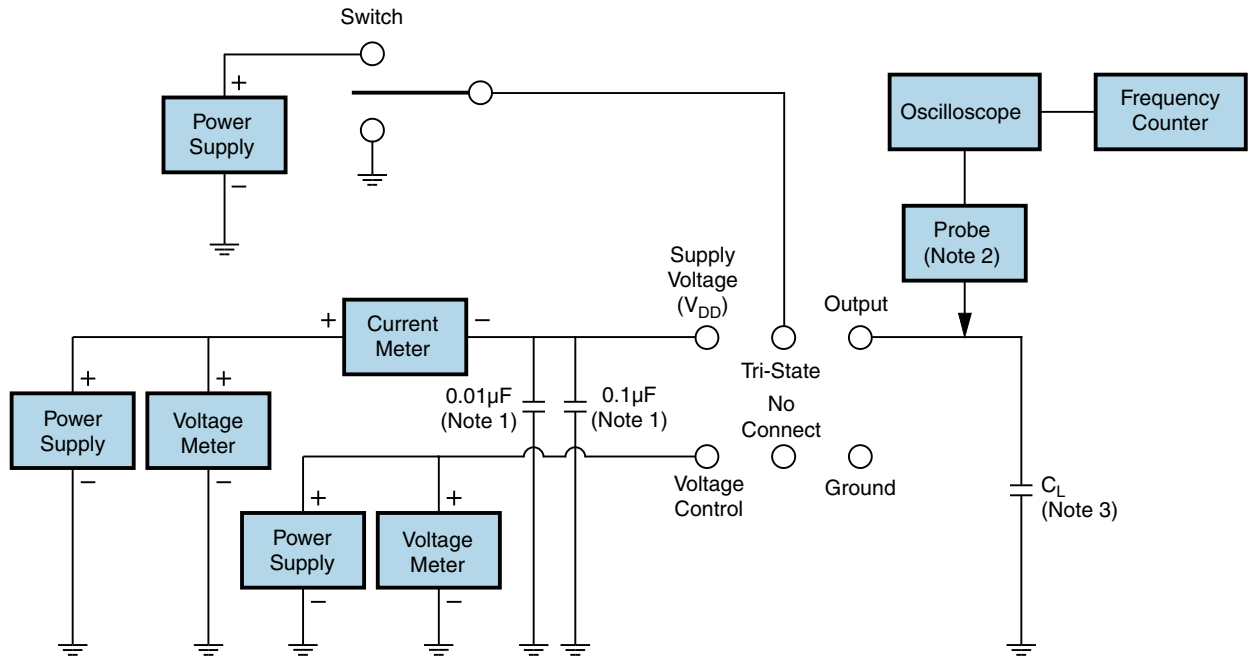
Output Load Drive Capability	R_L Value (Ohms)	C_L Value (pF)
10TTL	390	15

Table 1: R_L Resistance Value and C_L Capacitance Value Vs. Output Load Drive Capability

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Test Circuit for CMOS Output



Note 1: An external $0.01\mu F$ ceramic bypass capacitor in parallel with a $0.1\mu F$ high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

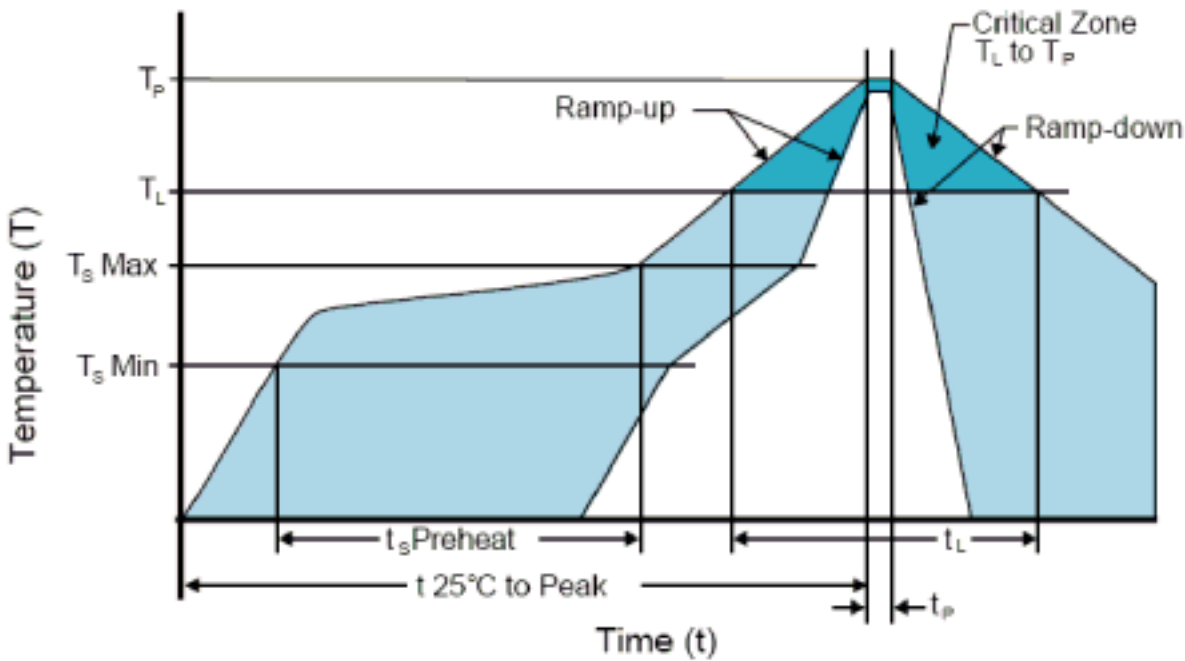
Note 2: A low capacitance ($<12pF$), 10X attenuation factor, high impedance ($>10M\Omega$), and high bandwidth ($>300MHz$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

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Recommended Solder Reflow Methods



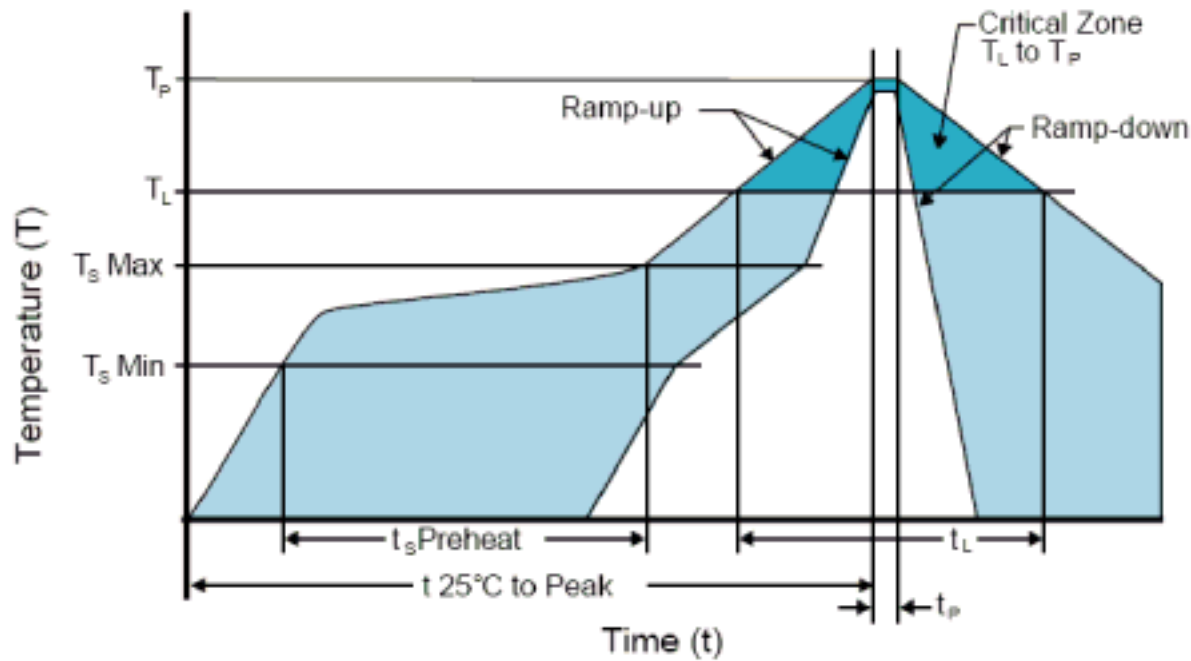
High Temperature Infrared/Convection

Ts MAX to TL (Ramp-up Rate)	3°C/Second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	150°C
- Temperature Typical (Ts TYP)	175°C
- Temperature Maximum (Ts MAX)	200°C
- Time (ts MIN)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/Second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (tL)	60 - 150 Seconds
Peak Temperature (TP)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (TP Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 Seconds
Ramp-down Rate	6°C/Second Maximum
Time 25°C to Peak Temperature (t)	8 Minutes Maximum
Moisture Sensitivity Level	Level 1

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Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

TS MAX to TL (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum (TS MIN)	N/A
- Temperature Typical (TS TYP)	150°C
- Temperature Maximum (TS MAX)	N/A
- Time (ts MIN)	60 - 120 Seconds
Ramp-up Rate (TL to TP)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (TL)	150°C
- Time (tL)	200 Seconds Maximum
Peak Temperature (TP)	240°C Maximum
Target Peak Temperature (TP Target)	240°C Maximum 2 Times / 230°C Maximum 1 Time
Time within 5°C of actual peak (tp)	10 Seconds Maximum 2 Times / 80 Seconds Maximum 1 Time
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.