



74AC16541

16-BIT BUS BUFFER WITH 3-STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:
 $t_{PD} = 4.5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 8 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH
74 SERIES 16541
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74AC16541 is an advanced high-speed CMOS 16-BIT BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

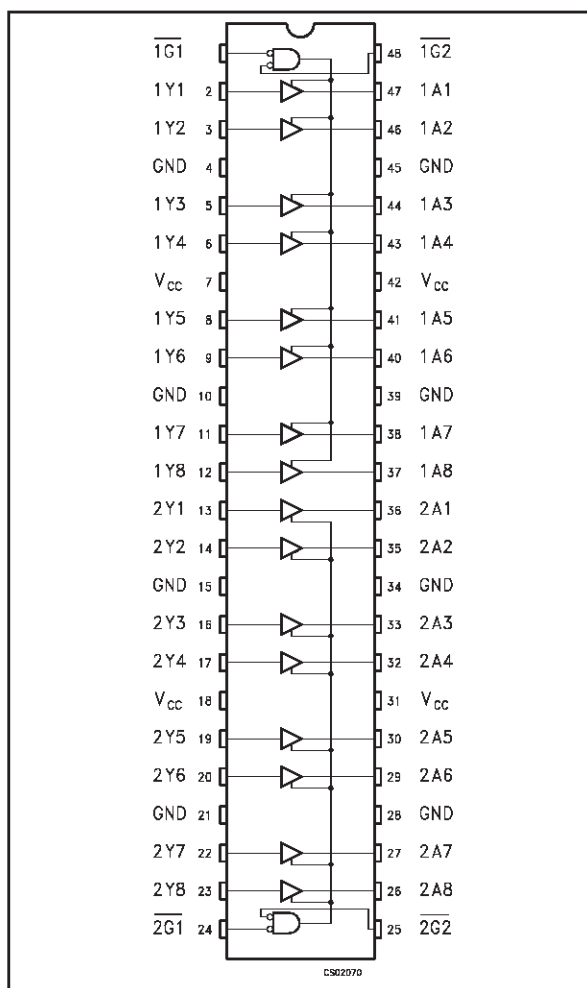
This is composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffers section, the 3 STATE control gate operates as a two input AND such that if either nG1 and nG2 are high, all outputs are in the high impedance state.



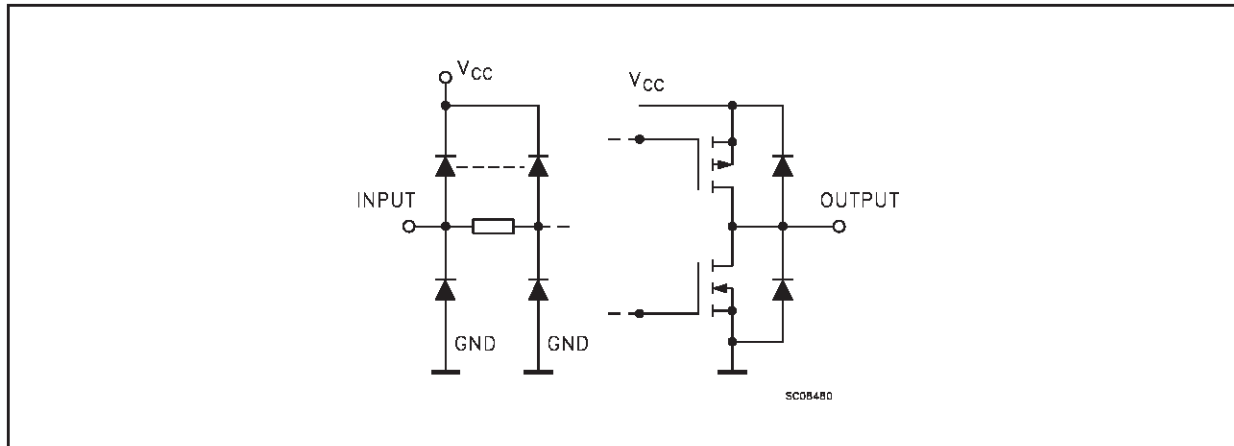
ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74AC16541TTR

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

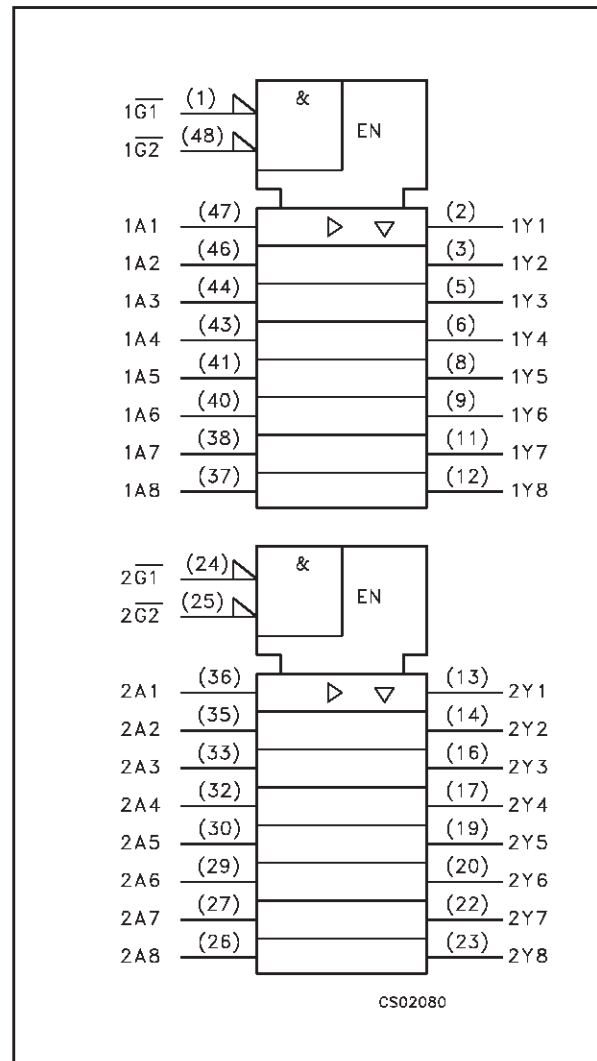
PIN No	SYMBOL	NAME AND FUNCTION
1, 48	1G1, 1G2	Output Enable Inputs
2, 3, 5, 6, 8, 9, 11, 12	1Y1 to 1Y8	Data Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Y1 to 2Y8	Data Outputs
24, 25	2G1, 2G2	Output Enable Inputs
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data Outputs
47, 46, 44, 43, 41, 40, 38, 37	1A1 to 1A8	Data Outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT
G1	G2	A _n	Y _n
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 50	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) $V_{CC} = 3.0, 4.5$ or 5.5	0 to 8	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} -0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V _{IL}	Low Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} -0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V _{OH}	High Level Output Voltage	3.0	I _O =-50 μA	2.9	2.99		2.9		2.9		V
		4.5	I _O =-50 μA	4.4	4.49		4.4		4.4		
		5.5	I _O =-50 μA	5.4	5.49		5.4		5.4		
		3.0	I _O =-12 mA	2.56			2.46		2.46		
		4.5	I _O =-24 mA	3.86			3.76		3.76		
		5.5	I _O =-24 mA	4.86			4.76		4.76		
V _{OL}	Low Level Output Voltage	3.0	I _O =50 μA		0.002	0.1		0.1		0.1	V
		4.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		5.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		3.0	I _O =12 mA			0.36		0.44		0.44	
		4.5	I _O =24 mA			0.36		0.44		0.44	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5		± 5	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			8		80		80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time A to Y	3.3 ^(*)				6.3	7.5		9.5		9.5	ns
		5.0 ^(**)				4.5	7.0		9.0		9.0	
t _{PZL} t _{PZH}	Output Enable Time	3.3 ^(*)				8.5	10.0		12.0		12.0	ns
		5.0 ^(**)				5.5	7.0		9.0		9.0	
t _{PLZ} t _{PHZ}	Output Disable Time	3.3 ^(*)				7.5	9.0		11.5		11.5	ns
		5.0 ^(**)				6.0	8.0		11.0		11.0	

(*) Voltage range is 3.3V ± 0.3V

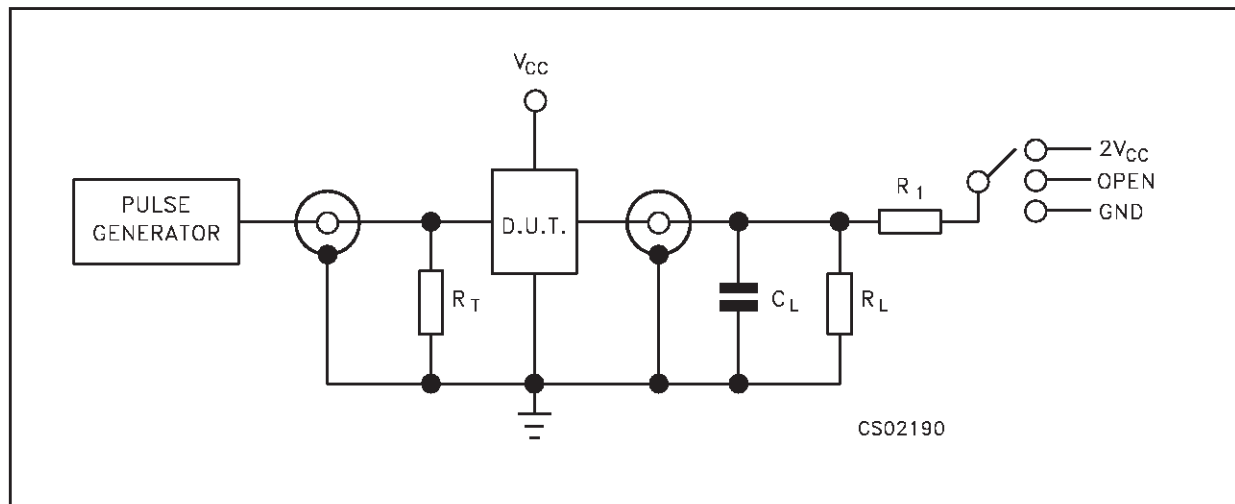
(**) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance				7	10		10		10	pF
C _{OUT}	Output Capacitance				14						pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0	f _{IN} = 10MHz		25						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$

TEST CIRCUIT

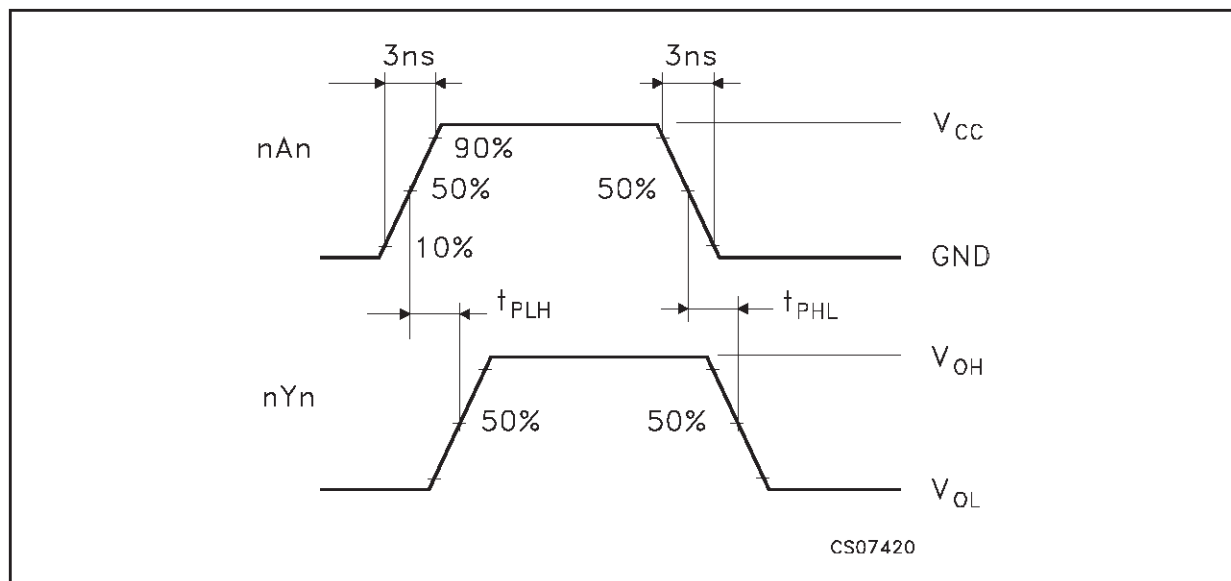
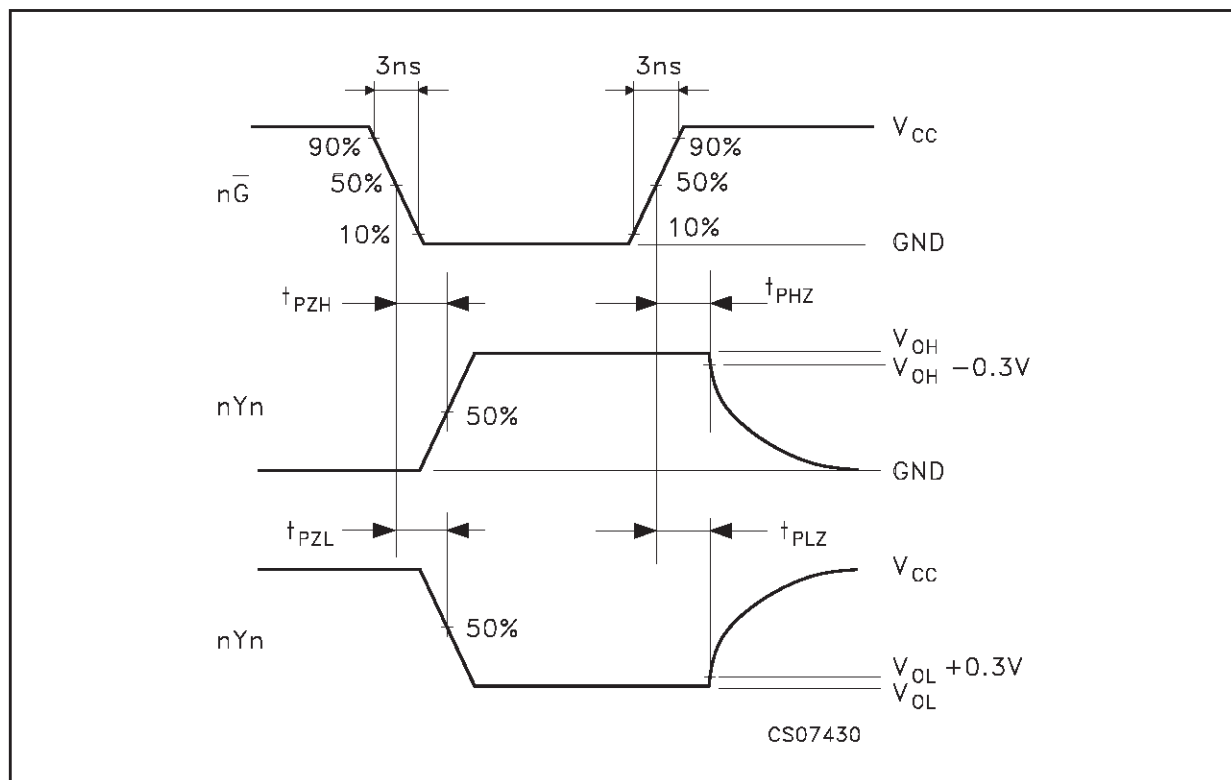


TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

$C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance)

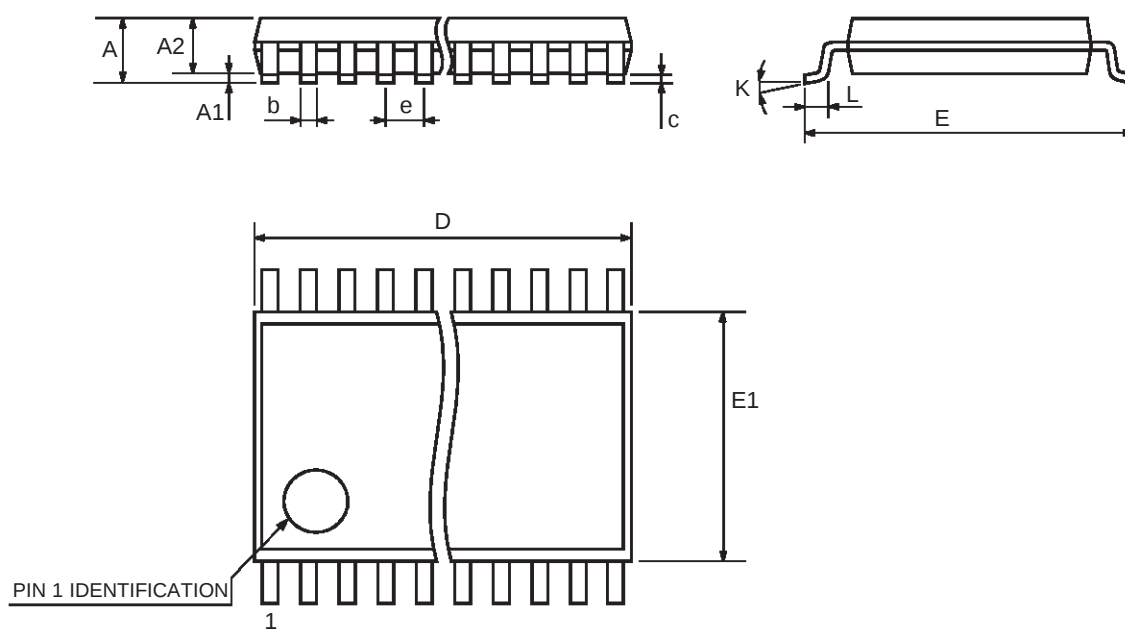
$R_L = R_1 = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ($f=1\text{MHz}$; 50% duty cycle)

TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.408		0.496
E	7.95		8.25	0.313		0.325
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



7065588A

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>