Amp'ed RF
Wireless Technology

Fast Track Your Wireless Project
自由无线 放飞梦想

WF43 Datasheet

Amp'ed RF Technology, Inc.

WF43 Product Specification

14.6mm x 13.5mm x 2.8 mm

Description

Amp'ed RF Tech presents the WF43 Wi-Fi Stand-alone module: 802.11bgn + Host MCU with Wi-Fi protocol stack. The WF43 is a small footprint low cost RF module including chip antenna, 7 general purpose and ADC/DAC IO lines, several serial interface options, and up to 12M bps data throughput using the SPI interface.

The complete stack, TCP/IP with WLAN, is hosted on the integrated MCU. A simple AT command interface, artSerial, allows users to easily configure and operate the WF43.

WLAN features

- 802.11b/g/n, 802.11d Regulatory Domain, 802.11r
- Output Power, +23dBm
- Power savings mode
- Transmit power back-off
- Wi-Fi Direct (concurrent)
- Wi-Fi Display
- Wi-Fi Protected Setup
- Soft Access Point
- Hotspot 2.0
- Security: WPAI/WPA2, AES, WEP

Hardware configuration

- Cortex-M3 microprocessor up to 72MHz
- 256K bytes Flash memory
- 48K bytes RAM memory
- UART, up to 2.25M baud
- SPI and I2C interfaces
- 7 general purpose I/O
- 5x12-bit A/D inputs
- 1 DAC output
- 1 LPO input
- Standby current, 40 µA
- RoHS conformance
- FCC/IC certified (pending)

Embedded software

- Amp'edUP WiFi stack
- artSerial, AT command set, SDK, Software Development Kit (Optional)
- Mobile application software (Optional)

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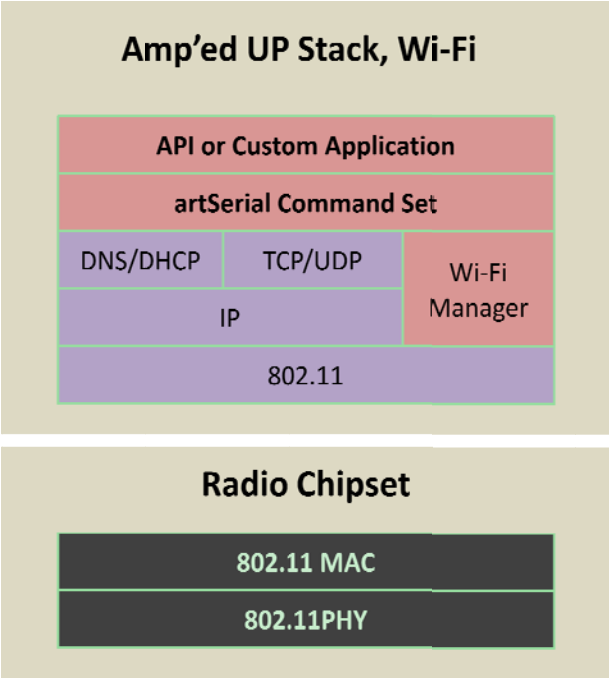
1 Software Architecture

1.1 Protocol stack diagram



1.2 Wi-Fi features

- 802.11b/g/n, 802.11d Regulatory Domain, 802.11r
- Output Power, +23dBm
- Interface, SDIO 2.0, SPI
- Wi-Fi Direct (concurrent)
- Wi-Fi Display
- Wi-Fi Protected Setup
- Soft Access Point
- Hotspot 2.0
- Security: WPAI/WPA2, AES, WEP, TKIP

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2 Hardware Specifications

General Conditions (V_{IN}= 3.6V and 25°C)

2.1 Recommended Operating Conditions

Rating	Min	Typical	Max	Unit
Operating Temperature Range	-40	-	85	°C
Supply Voltage V_{IN}	2.3	3.6	4.8	Volts
Signal Pin Voltage	-	2.0	-	Volts
RF Frequency	2400	-	2483.5	MHz

2.2 Absolute Maximum Ratings

Rating	Min	Typical	Max	Unit
Storage temperature range	-55	-	+150	°C
Supply voltage V_{IN}	-0.3	-	+5.0	Volts
I/O pin voltage V_{IO}	-0.3	-	+2.5	Volts
RF input power	-	-	-5	dBm

2.3 I/O Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low-Level Input Voltage	-	0.6	Volts
V_{IH}	High-Level Input Voltage	1.3	-	Volts
V_{OL}	Low-Level Output Voltage	-	0.4	Volts
V_{OH}	High-Level Output Voltage	2.0	-	Volts
I_{OL}	Low –Level Output Current	-	4.0	mA
I_{OH}	High-Level Output Current	-	4.0	mA
R_{PU}	Pull-up Resistor	80	120	KΩ
R_{PD}	Pull-down Resistor	80	120	KΩ

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2.4 Current Consumption

Modes (WLANMax Power Consumption) V_{BAT}=3.6v	**Avg**	**Unit**
Complete Power Down	17	µA
Sleep	101	µA
Power save (beacon period (including DTIM) 100ms, beacon length 1ms) -proprietary power saving features enabled	0.77	mA
RX (idle, 2.4GHz)	62.07	mA
RX (active, 2.4GHz, OFDM)	65.87	mA
TX (active, 2.4GHz, OFDM), 15.5dBm @RF port	257.67	mA
TX (active, 2.4GHz, OFDM), 20.5dBm @RF port	279.67	mA
A VoIP call using a standard codec G.711 (64Kb/s, 320 byte packets) and U-APSD (WMM power save) power-saving mode.	4.65	mA
Video streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example, MPEG-4@2Mbps)	13.31	mA
I_{peak}: system maximum peak current draw	378	mA
Modes (WLAN ReducedPower Consumption) VBAT=2.7v	**Avg**	**Unit**
Complete Power Down	TBD	µA
Sleep	TBD	µA
Power save (beacon period (including DTIM) 100ms, beacon length 1ms) -proprietary power saving features enabled	TBD	mA
RX (idle, 2.4GHz)	TBD	mA
RX (active, 2.4GHz, OFDM)	TBD	mA
TX (active, 2.4GHz, OFDM), 15.5dBm @RF port	TBD	mA
TX (active, 2.4GHz, OFDM), 20.5dBm @RF port	TBD	mA
A VoIP call using a standard codec G.711 (64Kb/s, 320 byte packets) and U-APSD (WMM power save) power-saving mode.	TBD	mA
Video streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example, MPEG-4@2Mbps)	TBD	mA
Ipeak: system maximum peak current draw	TBD	mA
Modes (WLAN Min Power Consumption) VBAT=2.3v	**Avg**	**Unit**
Complete Power Down	TBD	µA
Sleep	TBD	µA
Power save (beacon period (including DTIM) 100ms, beacon length 1ms) -proprietary power saving features enabled	TBD	mA
RX (idle, 2.4GHz)	TBD	mA
RX (active, 2.4GHz, OFDM)	TBD	mA
TX (active, 2.4GHz, OFDM), 15.5dBm @RF port	TBD	mA
TX (active, 2.4GHz, OFDM), 20.5dBm @RF port	TBD	mA
A VoIP call using a standard codec G.711 (64Kb/s, 320 byte packets) and U-APSD (WMM power save) power-saving mode.	TBD	mA
Video streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example, MPEG-4@2Mbps)	TBD	mA
Ipeak: system maximum peak current draw	TBD	mA

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2.5 Selected RF Characteristics

Parameters	Conditions	Typical	Unit
Antenna load		50	ohm
Wi-Fi Receiver			
Sensitivity	DSSS 1Mbps@FER<8%	-98.5	dBm
Sensitivity	DSSS 2Mbps@FER<8%	-96	dBm
Sensitivity	CCK 5.5Mbps@FER<8%	-94	dBm
Sensitivity	CCK 11Mbps@FER<8%	-89	dBm
Sensitivity	BPSK 6Mbps@PER<10%	-94.5	dBm
Sensitivity	BPSK 9Mbps@PER<10%	-92.5	dBm
Sensitivity	QPSK 12Mbps@PER<10%	-91.5	dBm
Sensitivity	QPSK 18Mbps@PER<10%	-89	dBm
Sensitivity	16QAM 24Mbps@PER<10%	-86	dBm
Sensitivity	16QAM 36Mbps@PER<10%	-83	dBm
Sensitivity	64QAM 48Mbps@PER<10%	-78.5	dBm
Sensitivity	64QAM 54Mbps@PER<10%	-77	dBm
Sensitivity	BPSK 6.5Mbps@PER<10%	-92.5	dBm
Sensitivity	QPSK 13Mbps@PER<10%	-89.5	dBm
Sensitivity	QPSK 19.5Mbps@PER<10%	-87	dBm
Sensitivity	16QAM 26Mbps@PER<10%	-84.5	dBm
Sensitivity	16 QAM 39Mbps@PER<10%	-81	dBm
Sensitivity	64QAM 52Mbps@PER<10%	-77	dBm
Sensitivity	64QAM 58.5Mbps@PER<10%	-75.5	dBm
Sensitivity	64QAM 65Mbps@PER<10%	-73.5	dBm
Wi-Fi Transmitter			
Output Power	802.11b/g BPSK 1/2	20	dBm
Output Power	802.11b/g BPSK 3/4	20	dBm
Output Power	802.11b/g QPSK 1/2	20	dBm
Output Power	802.11b/g QPSK 3/4	20	dBm
Output Power	802.11b/g 16QAM 1/2	19.5	dBm
Output Power	802.11b/g 16QAM 3/4	18.5	dBm
Output Power	802.11b/g 64QAM 2/3	17.5	dBm
Output Power	802.11b/g 64QAM 3/4	16.5	dBm
Output Power	802.11n MCS-0	20	dBm
Output Power	802.11n MCS-1	20	dBm
Output Power	802.11n MCS-2	20	dBm
Output Power	802.11n MCS-3	19.5	dBm
Output Power	802.11n MCS-4	18.5	dBm
Output Power	802.11n MCS-5	17.5	dBm
Output Power	802.11n MCS-6	16.5	dBm
Output Power	802.11n MCS-7	15.5	dBm

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2.6 Transmit Power Back-off

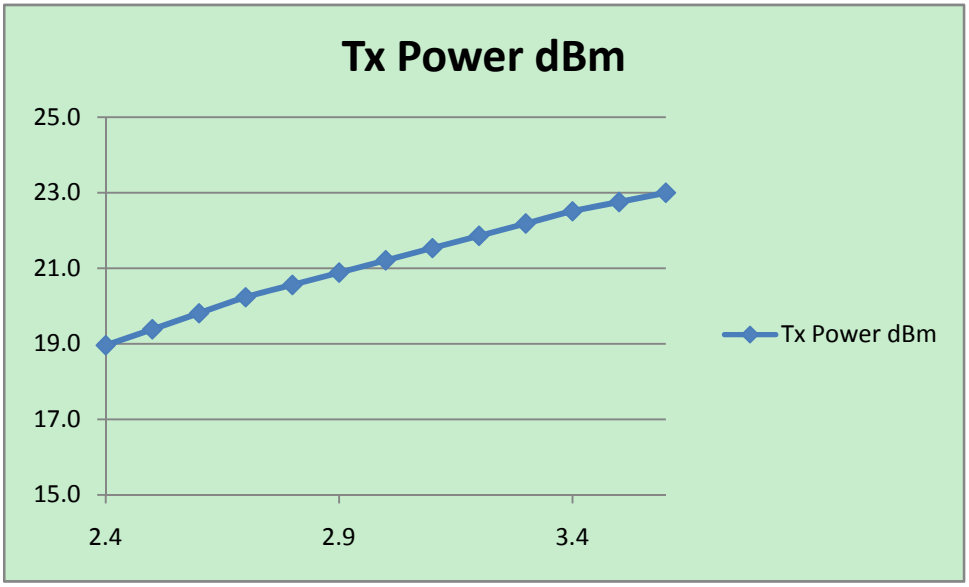
When 2.7 V < VBAT < 3.6 V, the output power shall be backed off by 0.8 dB per300 mV drop of Vbat below 3.6 V to guarantee meeting spectral mask, EVM, harmoniclevels, spurious emissions and regulatory requirements in general.

When 2.3 V < VBAT < 2.7 V, an additional back-off of the output power is needed to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general.

When the load is not 50Ω, the output power is backed off to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general. The device is able to withstand a VSWR of up to 12:1 without any damage.

When the temperature increases from +25°C to +85°C, the output power shall be backed off by 0.25 dB per 10°C increase to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions and regulatory requirements in general.

Tx Power vs Vin



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2.7 Pin Assignment

WF43H

Name	Type	Pin #	Description	ALT Function	5V Tolerant	Initial State
UART Interface						
RXD	I	13	Receive data		Y	
TXD	O	14	Transmit data		Y	
RTS	O	12	Request to send (active low)	I2C Data/Aux Uart Rx	Y	
CTS	I	11	Clear to send (active low)	I2C Clock/Aux Uart Tx	Y	
Reserved						
BOOT 0	I	9	Boot 0			
Power and Ground						
V_{in}		8	V_{in}			
GND		7	GND			
Reset						
RESETN	I	10	Reset input (active low for 5 ms)		2.5V max	
LPO						
SYSCLK	I	15	Sysclk input			
GPIO – General Purpose Input/Output						
GPIO [1]	I/O	1	General Purpose Input/Output	SPI MISO	Y	Input pull down
GPIO [2]	I/O	2	General Purpose Input/Output	SPI MOSI/I2S SD	Y	Floating
GPIO [3]	I/O	3	General Purpose Input/Output	SPI SCLK/ I2S CK	Y	Input pull down
GPIO [4]	I/O	4	General Purpose Input/Output	SPI SS/I2S WS	Y	Input pull down
GPIO [5]	I/O	5	General Purpose Input/Output	ADC 0	2.5V max	Input pull down
GPIO [6]	I/O	6	General Purpose Input/Output	ADC 1/DAC 0	2.5V max	Input pull down

WF43S

Name	Type	Pin #	Description	ALT Function	5V Tolerant	Initial State
UART Interface						
RXD	I	13	Receive data		Y	
TXD	O	14	Transmit data		Y	
RTS	O	12	Request to send (active low)	I2C Data/Aux Uart Rx	Y	
CTS	I	11	Clear to send (active low)	I2C Clock/Aux Uart Tx	Y	
Reserved						
BOOT 0	I	9	Boot 0			
Power and Ground						
V_{in}		8	V_{in}			
GND		7	GND			
Reset						
RESETN	I	10	Reset input (active low for 5 ms)		2.5V max	
LPO						
LPO	I	15	LPO input			
GPIO – General Purpose Input/Output						
GPIO [1]	I/O	1	General Purpose Input/Output	SPI MISO/I2SextSD	Y	Input pull down
GPIO [2]	I/O	2	General Purpose Input/Output	SPI MOSI/I2S SD	Y	Floating
GPIO [3]	I/O	3	General Purpose Input/Output	SPI SCLK/ I2S CK	Y	Input pull down
GPIO [4]	I/O	4	General Purpose Input/Output	SPI SS/I2S WS	Y	Input pull down
GPIO [5]	I/O	5	General Purpose Input/Output	ADC 0	Y	Input pull down
GPIO [6]	I/O	6	General Purpose Input/Output	ADC 1	Y	Input pull down

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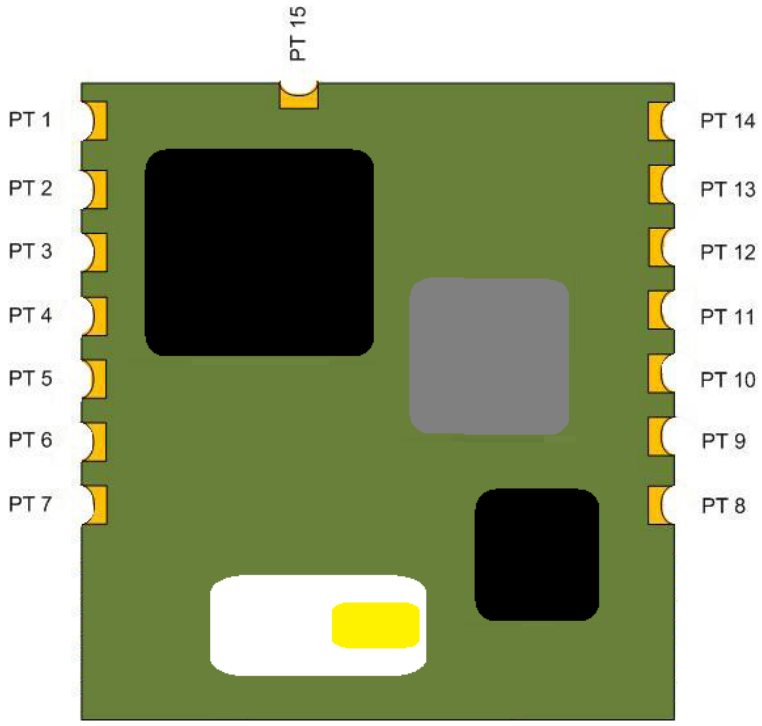
2.8 Pin Placement Diagram (Top View)



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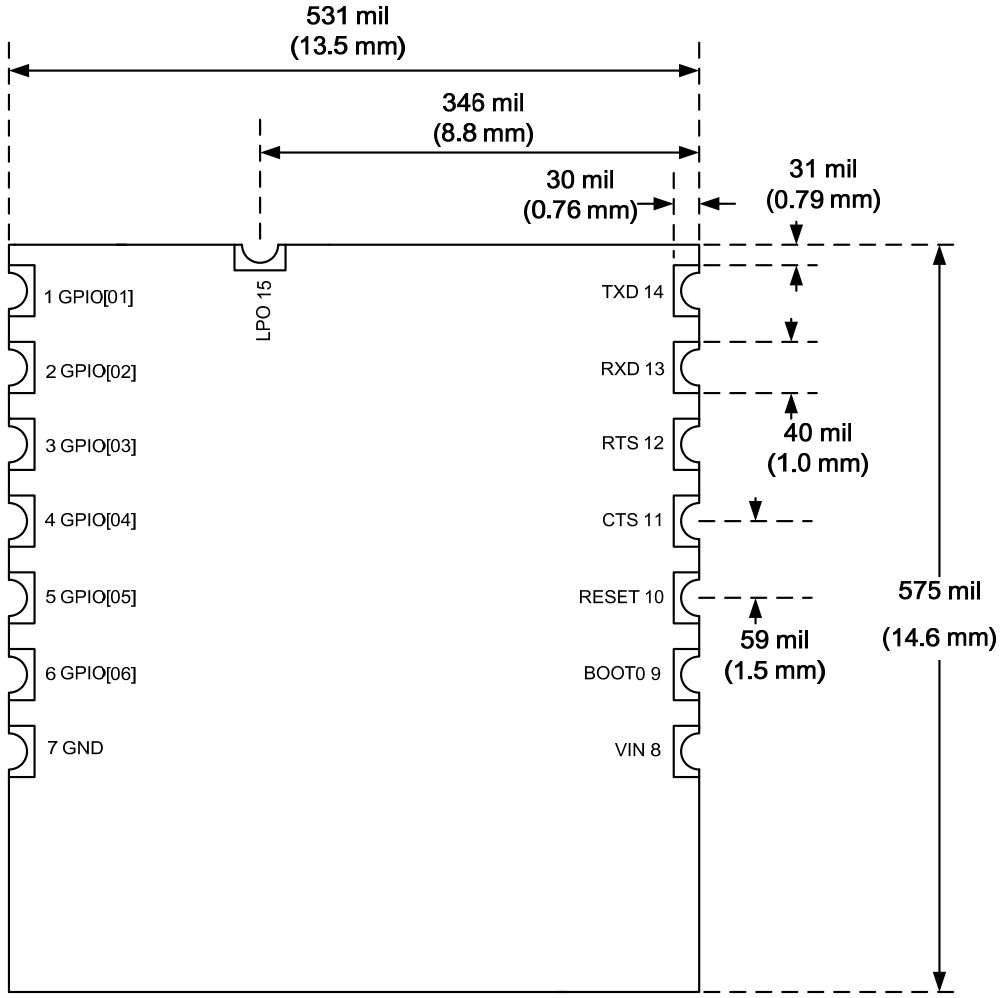
2.9 Layout Drawing

Size: 14.6 mm x 13.5 mm x 2.8 mm



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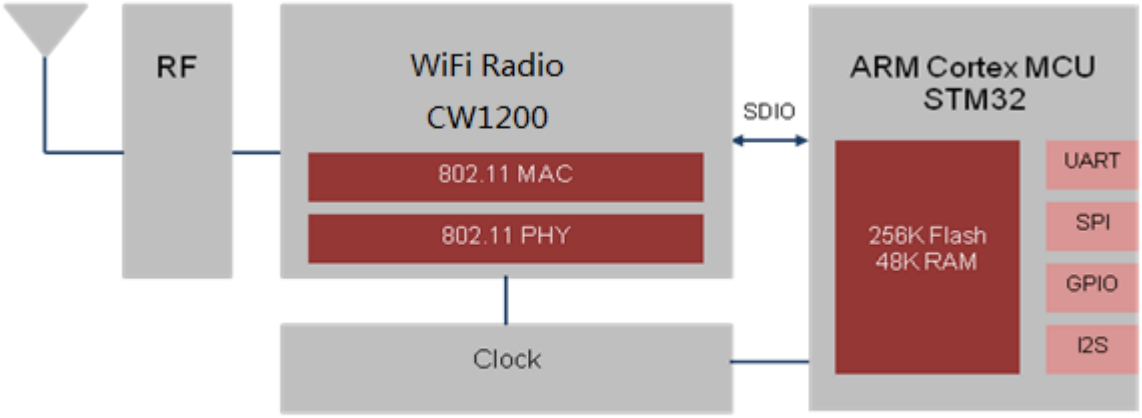
3 Hardware Design

3.1 Block Diagram



3.2 Layout

- All unused pins should be left floating; do not ground.
- All GND pins must be well grounded.
- The area around the antenna should be free of any ground planes, power planes, trace routings, or metal for at least 6.5 mm in all directions.
- Traces should not be routed underneath the module.

3.3 Module Reflow

The WF43 is a surface mount module supplied on a 15 pin, 6-layer PCB. The final assembly recommended reflow profiles are:

For RoHS/Pb-free applications, Sn96.5/Ag3.0/Cu0.5 solder is recommended.

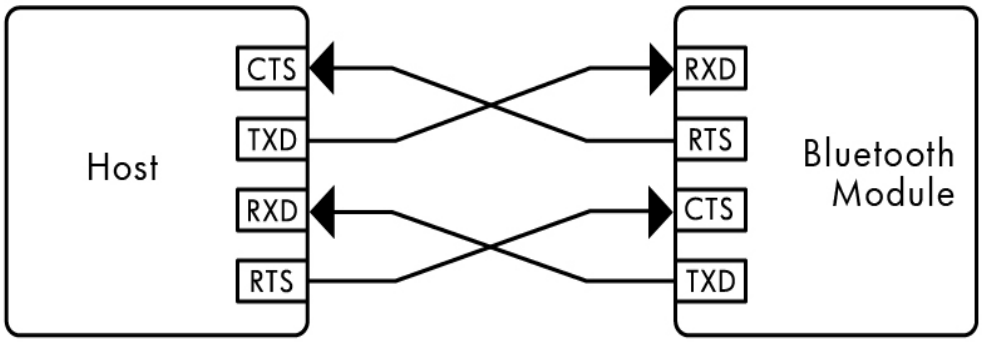
- Maximum peak temperature of 230° - 240°C (below 250°C).
- Maximum rise and fall slope after liquidous of < 2°C/second.
- Maximum rise and fall slope after liquidous of < 3°C/second.
- Maximum time at liquidous of 40 – 80 seconds.

3.4 GPIO Interface

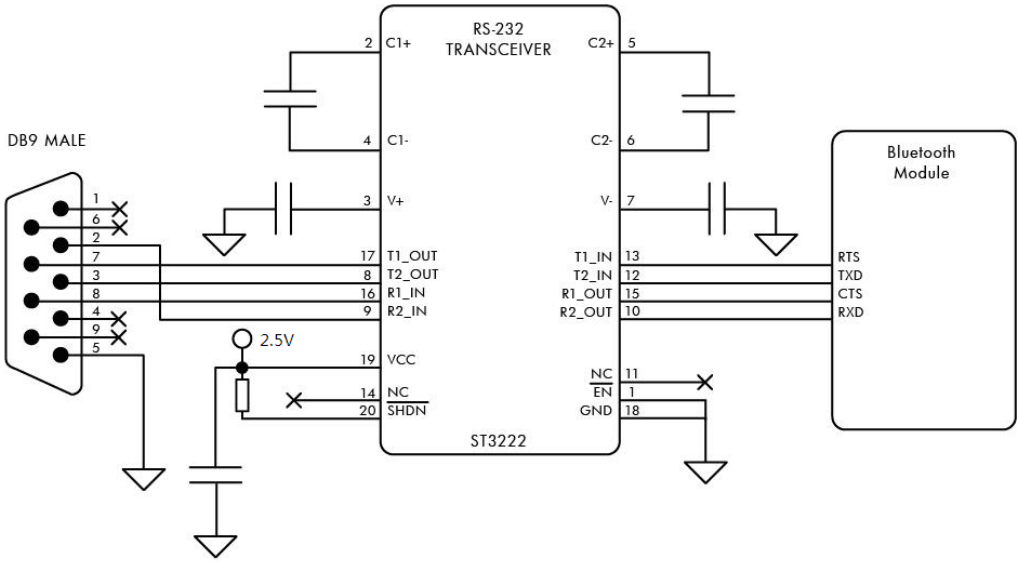
All GPIOs are capable of sinking and sourcing 4mA of I/O current.

3.5 UART Interface

The UART is compatible with the 16550 industry standard. Four signals are provided with the UART interface. The TXD and RXD pins are used for data while the CTS and RTS pins are used for flow control.

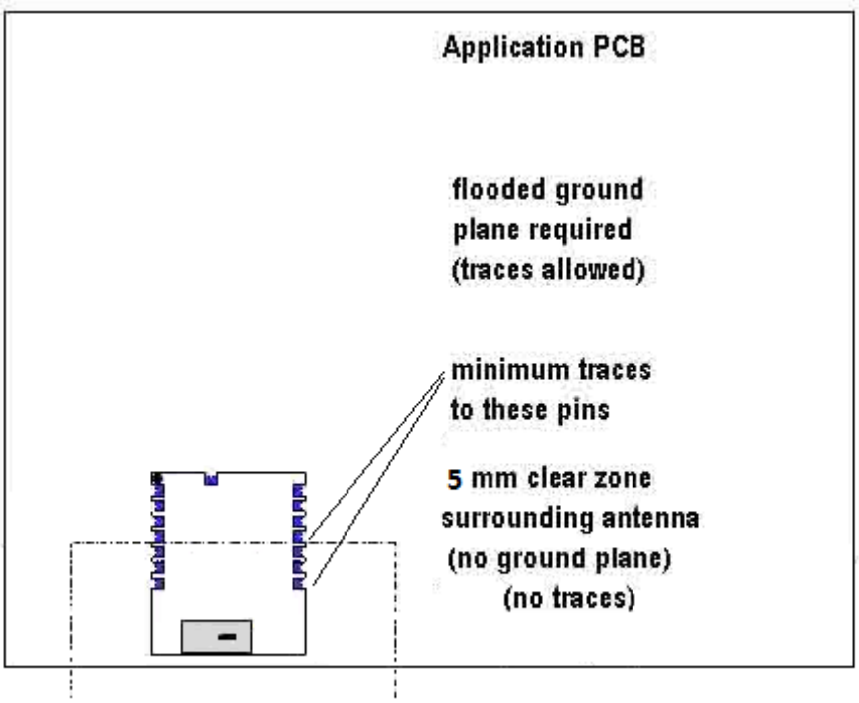


Connection to Host Device



Typical RS232 Circuit

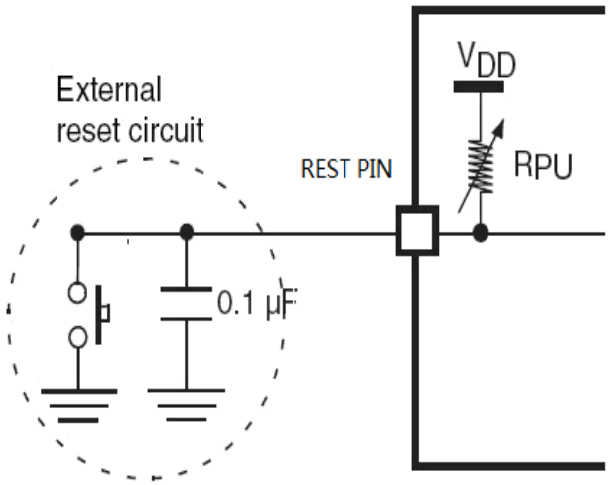
3.6 PCB Layout Guidelines



3.7 Reset Circuit

Two types of system reset circuits are detailed below.

3.7.1 External Reset Circuit



Note: R_{PU} ranges from 30K ohm to 50K ohm internally.

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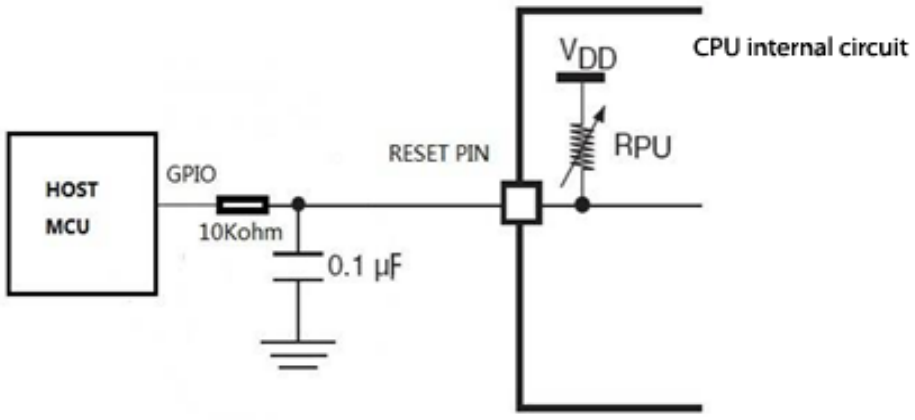
3.7.2 Internal Reset Circuit



Notes:

- R_{PU} ranges from 30K ohm to 50K ohm internally.
- R_{RST} should be from 1K ohm to 10K ohm

4 Regulatory Compliance

This module has been tested and found to comply with the FCC Part15 and IC RSS-210 rules. These limits are designed to provide reasonable protection against harmful interference in approved installations. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications or changes to this equipment not expressly approved by Amp'ed RF Technology may void the user's authority to operate this equipment.

4.1 Modular Approval, FCC and IC

FCC ID: TBD

IC: TBD

In accordance with FCC Part 15, the WF41 is listed above as a Limited Modular Transmitter device.

4.2 FCC Label Instructions

The outside of final products that contain a WF41 device must display a label referring to the enclosed module. This exterior label can use wording such as the following:

Contains Transmitter Module

FCC ID: TBD

IC: TBD

Any similar wording that expresses the same meaning may be used.

4.3 CE Label Instructions

CE Certification

CE ID: TBD

5 Ordering Information

Part Name	Description
WF43H	High performance version
WF43S	Extended memory version

6 Revision History

Data	Revision	Description
17-February-2014	1.2	Added WF43LT option
20-June-2014	1.3	Update the picture of WF43
16-Sep-2014	1.4	Update the ordering information

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