TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

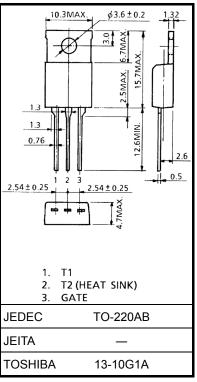
SM6G45, SM6J45, SM6G45A, SM6J45A

AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage: VDRM = 400V, 600V
- R.M.S On-State Current: IT (RMS) = 6A
- High Commutating (dv / dt)

ABSOLUTE MAXIMUM RATINGS

CHARACTERI	STIC	SYMBOL	RATING	UNIT	
Repetitive Peak Off-	SM6G45 SM6G45A	V _{DRM}	400	>	
State Voltage	SM6J45 SM6J45A	V DRM	600		
R.M.S On-State Curren (Full Sine Waveform Tc	•	I _{T (RMS)}	6	А	
Peak One Cycle Surge On-State Current (Non-Repetitive)		I _{TSM}	60 (50Hz)	Α	
			66 (60Hz)		
I ² t Limit Value		I ² t	18	A ² s	
Critical Rate of Rise of C Current	n-State	di / dt 50		A / μs	
Peak Gate Power Dissip	ation	P _{GM}	5	W	
Average Gate Power Dis	ssipation	P _G (AV)	0.5	W	
Peak Gate Voltage		V_{GM}	10	V	
Peak Gate Current		I _{GM}	2	Α	
Junction Temperature		Tj	-40~125	°C	
Storage Temperature Ra	ange	T _{stg} -40~125		°C	



Unit: mm

Weight: 2.0 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

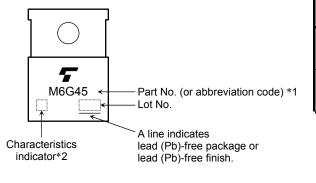
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



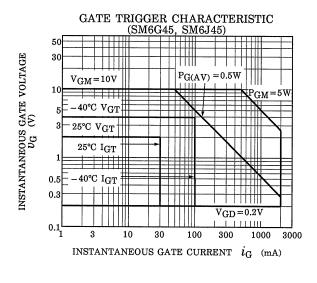
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

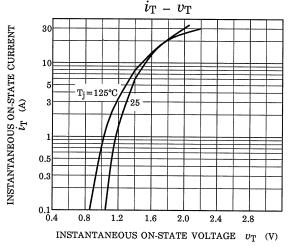
CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT		
Repetitive Peak Current	COff-State			I _{DRM}	V _{DRM} = Rated, T _j = 125°C		_	_	2	mA
Gate Trigger Voltage			I	V _{GT}	V _D = 12V R _L = 20Ω	T2 (+), Gate (+)	_	_	2	V
	SM6G4	5	II			T2 (+), Gate (-)	_	_	2	
	SM6J45	i	III			T2 (-), Gate (-)	_	_	2	
		-	IV			T2 (-), Gate (+)	_	_	_	
			I			T2 (+), Gate (+)	_	_	1.5	
	SM6G4	5A	II			T2 (+), Gate (-)	_	_	1.5	
	SM6J45		III			T2 (-), Gate (-)	_	_	1.5	
		•	IV			T2 (-), Gate (+)	_	_	_	
Gate Trigger Current			I	- lgī	$V_D = 12V$ $R_L = 20\Omega$	T2 (+), Gate (+)	_	_	30	- mA
	SM6G4	5	II			T2 (+), Gate (-)	_	_	30	
	SM6J45		III			T2 (-), Gate (-)	_	_	30	
		•	IV			T2 (-), Gate (+)	_	_	_	
			I			T2 (+), Gate (+)	_	_	20	
	SM6G4	5A	II			T2 (+), Gate (-)	_	_	20	
	SM6J45	A	III			T2 (-), Gate (-)	_	_	20	
		•	IV			T2 (-), Gate (+)	_	_	_	
Peak On-State Voltage		V _{TM}	I _{TM} = 9A		_	_	1.5	V		
Gate Non-Trigger Voltage		V_{GD}	V _D = Rated, Tc = 125°C		0.2	_	_	V		
Holding Current		I _H	V _D = 12V, I _{TM} = 1A		_	_	50	mA		
Thermal Resistance		R _{th (j-c)}	Junction to Case, AC		_	_	2.5	°C / W		
Critical Rate of SM6G45 Rise of Off-SM6J45 State Voltage at SM6G45A Commutation				V _{DRM} = 400V,		10	_	_	V/us	
				(dv / dt) c	(di / dt) c = -3.3A / ms $T_j = 125°C$		4	_	_	V / µs

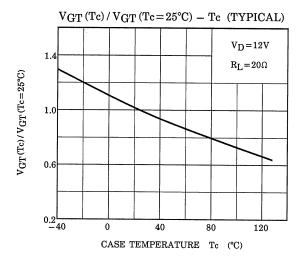
MARKING

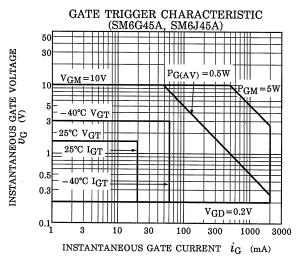


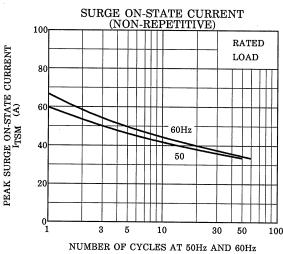
	Part No. (or abbreviation code)	Part No.
*1	M6G45	SM6G45, SM6G45A
	M6J45	SM6J45, SM6J45A
*2	Nothing	SM6G45, SM6J45
	A	SM6G45A, SM6J45A

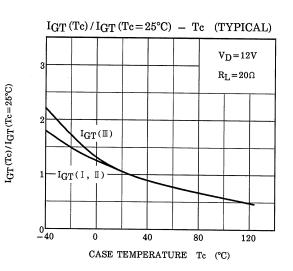




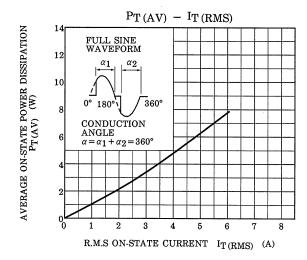


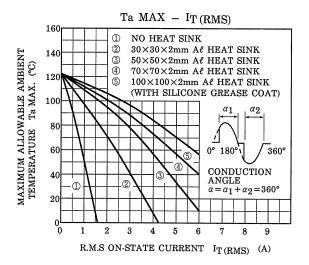


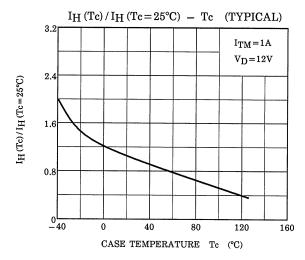


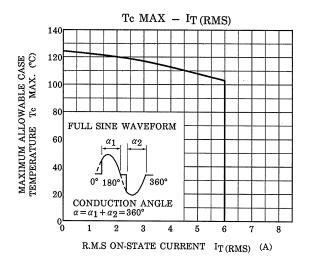


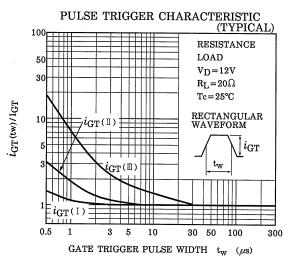
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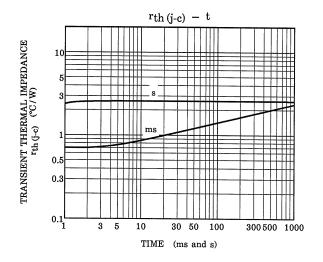












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20070701-EN

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